# P4C1258
# ULTRA HIGH SPEED 64K x 4
# STATIC CMOS RAM

## FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  **– 15/20/25/35 ns (Commercial/Industrial)**
- **Low Power**
- **Single 5V±10% Power Supply**
- **Data Retention with 2.0V Supply**
- **Three-State Outputs**
- **TTL/CMOS Compatible Outputs**
- **Fully TTL Compatible Inputs**
- **Standard Pinout (JEDEC Approved)**
  **– 24-Pin 300 mil DIP, SOJ**

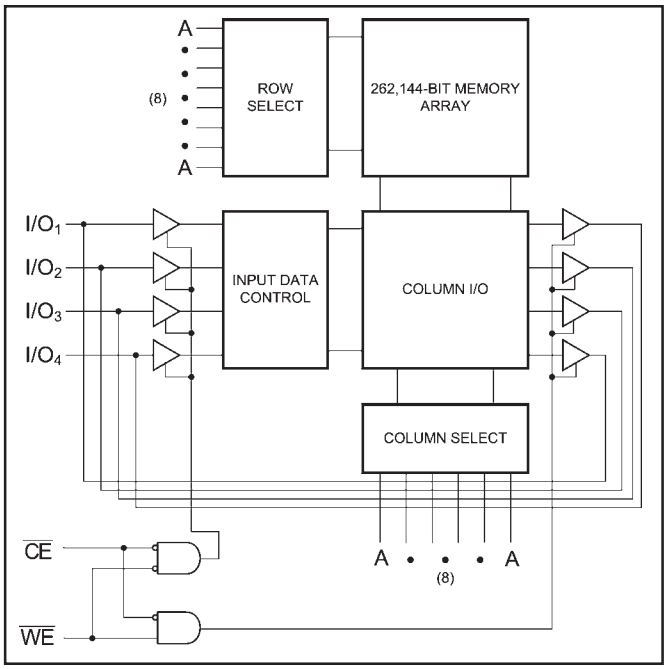
## DESCRIPTION

The P4C1258 is a 262,144-bit ultra high speed static RAM organized as 64K x 4. The CMOS memory requires no clock or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 10 µA from a 2.0V supply.

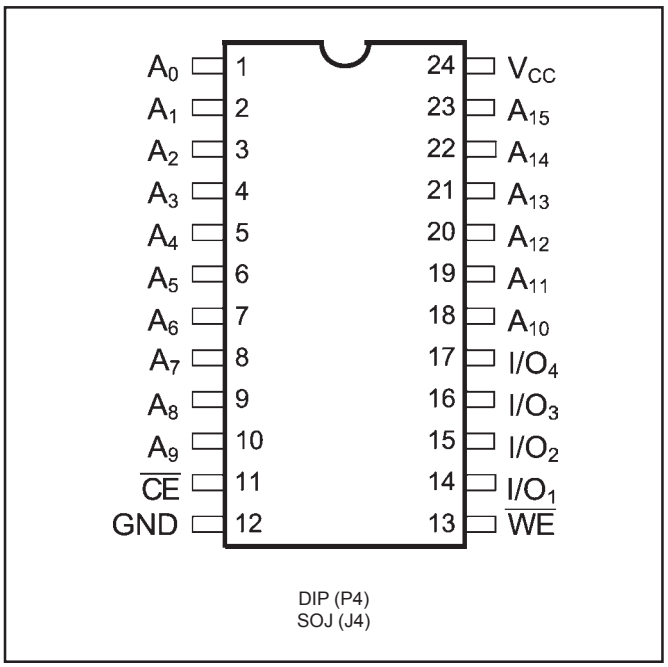
Access times as fast as 15 nanoseconds are available, permitting greatly enhanced system speeds. CMOS is utilized to reduce power consumption.

The P4C1258 is available in a 24-pin 300 mil DIP or SOJ packages providing excellent board level densities.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATION




DIP (P4)
SOJ (J4)

## MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Pin with Respect to GND | –0.5 to +7 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | –55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade(2) | Ambient Temperature | GND | $V_{CC}$ |
|---|---|---|---|
| Industrial | –40°C to +85°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

## CAPACITANCES[4]

$V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz

| Symbol | Parameter | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

| Symbol | Parameter | Test Conditions | P4C1258 | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{CC}$ +0.5 | V |
| $V_{IL}$ | Input Low Voltage | | –0.5[3] | 0.8 | V |
| $V_{HC}$ | CMOS Input High Voltage | | $V_{CC}$ –0.2 | $V_{CC}$ +0.5 | V |
| $V_{LC}$ | CMOS Input Low Voltage | | –0.5[3] | 0.2 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = 18 mA | | –1.2 | V |
| $V_{OL}$ | Output Low Voltage (TTL Load) | $I_{OL}$ = +8 mA, $V_{CC}$ = Min. | | 0.4 | V |
| $V_{OH}$ | Output High Voltage (TTL Load) | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | 2.4 | | V |
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max.<br>$V_{IN}$ = GND to $V_{CC}$ | –5 | +5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CE}$ = $V_{IH}$<br>$V_{OUT}$ = GND to $V_{CC}$ | –5 | +5 | µA |
| $I_{SB}$ | Standby Power Supply Current (TTL Input Levels) | $\overline{CE} \geq V_{IH}$<br>$V_{CC}$ = Max ., f = Max., Outputs Open | —— | 35 | mA |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE} \geq V_{HC}$<br>$V_{CC}$ = Max., f = 0, Outputs Open<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | —— | 10 | mA |

**Notes:**

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with $V_{IL}$ and $I_{IL}$ not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

## POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | –15 | –20 | –25 | –35 | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current* | Commercial | 160 | 125 | 115 | 110 | mA |
| | | Industrial | 170 | 135 | 120 | 115 | mA |

*$V_{CC}$ = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = $V_{IL}$

## DATA RETENTION CHARACTERISTICS

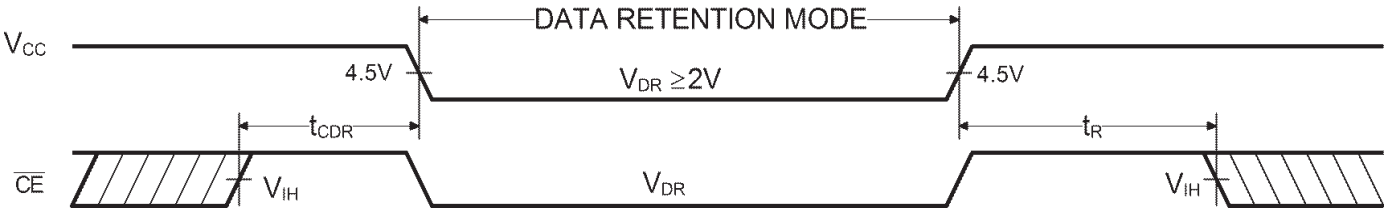
| Symbol | Parameter | Test Conditions | Min | Typ.* $V_{cc}$ = 2.0V | Typ.* $V_{cc}$ = 3.0V | Max $V_{cc}$ = 2.0V | Max $V_{cc}$ = 3.0V | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2.0 | | | | | V |
| $I_{CCDR}$ | Data Retention Current | $\overline{CE} \geq V_{CC}$ –0.2V, $V_{IN} \geq V_{CC}$ –0.2V or $V_{IN} \leq 0.2V$ | | 10 | 15 | 1500 | 2000 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | | | | | ns |
| $t_R$† | Operation Recovery Time | | $t_{RC}$§ | | | | | ns |

*$T_A$ = +125°C

§$t_{RC}$ = Read Cycle Time

† This parameter is guaranteed but not tested.

## DATA RETENTION WAVEFORM

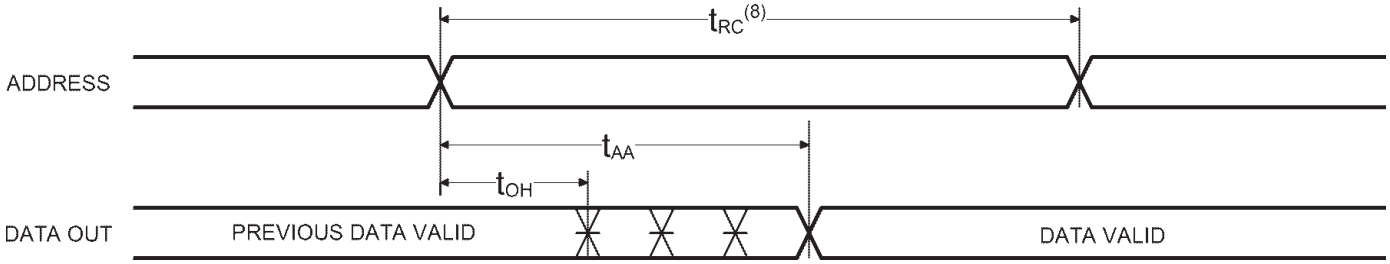


## AC CHARACTERISTICS—READ CYCLE

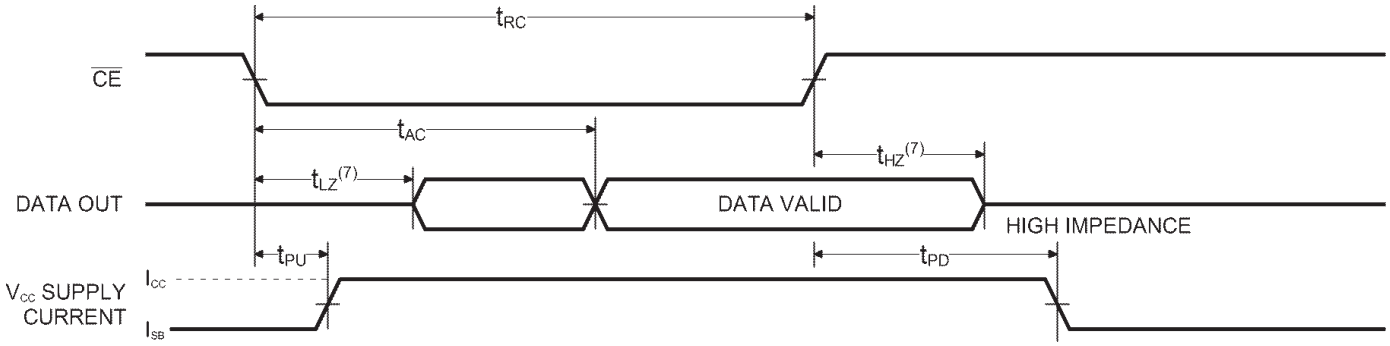
($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | -15 | | -20 | | -25 | | -35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{AA}$ | Address Access Time | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{AC}$ | Chip Enable Access Time | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{OH}$ | Output Hold from Address Change | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{LZ}$ | Chip Enable to Output in Low Z | 2 | | 3 | | 3 | | 3 | | ns |
| $t_{HZ}$ | Chip Disable to Output in High Z | | 8 | | 9 | | 10 | | 11 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | Chip Disable to Power Down Time | | 15 | | 20 | | 25 | | 35 | ns |

## TIMING WAVEFORM OF READ CYCLE NO. 1[5]




## TIMING WAVEFORM OF READ CYCLE NO. 2[6]




**Notes:**

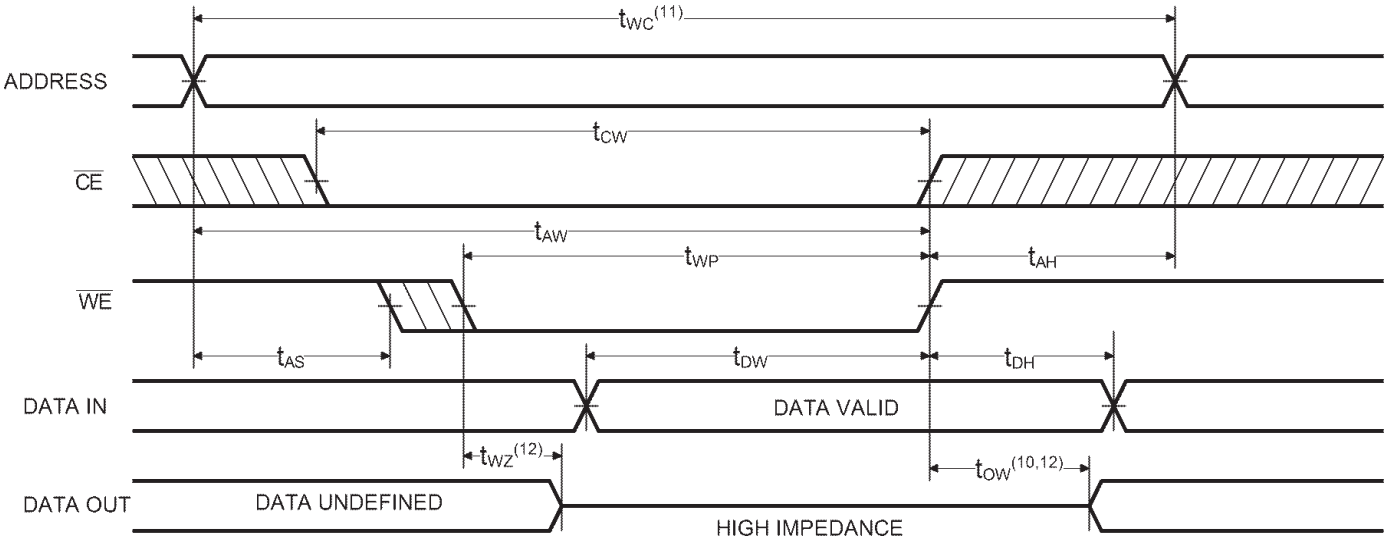
5. $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{WE}$ is HIGH, and address must be valid prior to or coincident with $\overline{CE}$ transition LOW.
7. Transition is measured ±200mV from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.
8. Read Cycle Time is measured from the last valid address to the first transitioning address.

## AC CHARACTERISTICS - WRITE CYCLE

($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | -15 | | -20 | | -25 | | -35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write Cycle Time | 13 | | 20 | | 25 | | 35 | | ns |
| $t_{CW}$ | Chip Enable Time to End of Write | 12 | | 15 | | 18 | | 25 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 12 | | 15 | | 18 | | 25 | | ns |
| $t_{AS}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 12 | | 15 | | 18 | | 25 | | ns |
| $t_{AH}$ | Address Hold Time from End of Write | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Data Valid to End of Write | 7 | | 8 | | 10 | | 15 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WZ}$ | Write Enable to Output in High Z | | 6 | | 8 | | 10 | | 15 | ns |
| $t_{DW}$ | Output Active from End of Write | 2 | | 2 | | 2 | | 3 | | ns |

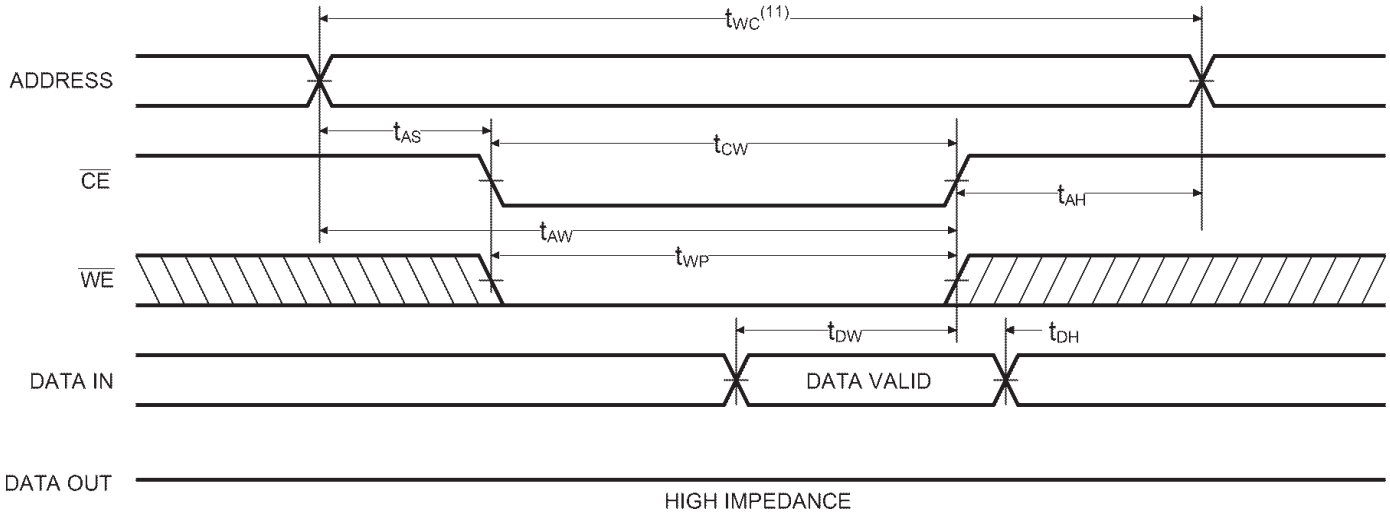
## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) [9]




**Notes:**

9. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
10. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.
12. Transition is measured ±200mV from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.

## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[9]




## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

## TRUTH TABLE

| Mode | $\overline{CE}$ | $\overline{WE}$ | Output | Power |
|---|---|---|---|---|
| Standby | H | X | High Z | Standby |
| Read | L | H | $D_{OUT}$ | Active |
| Write | L | L | $D_{IN}$ | Active |

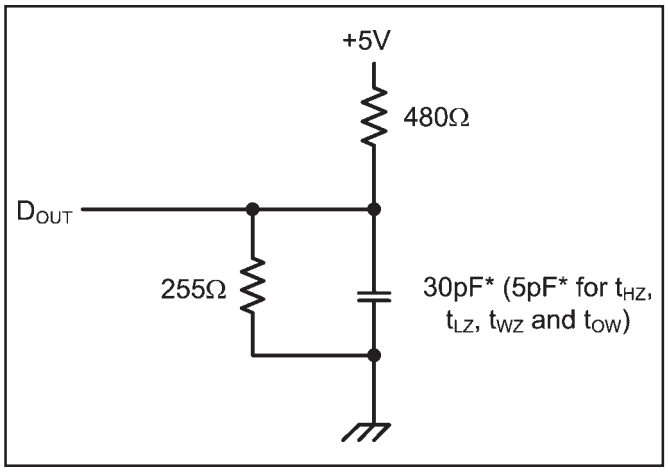



**Figure 1. Output Load**

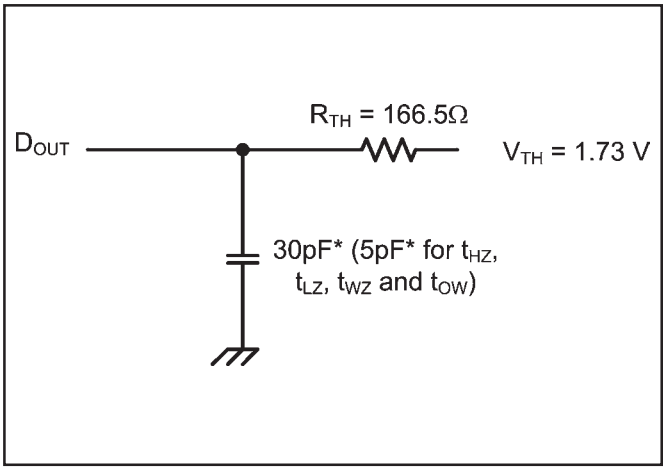
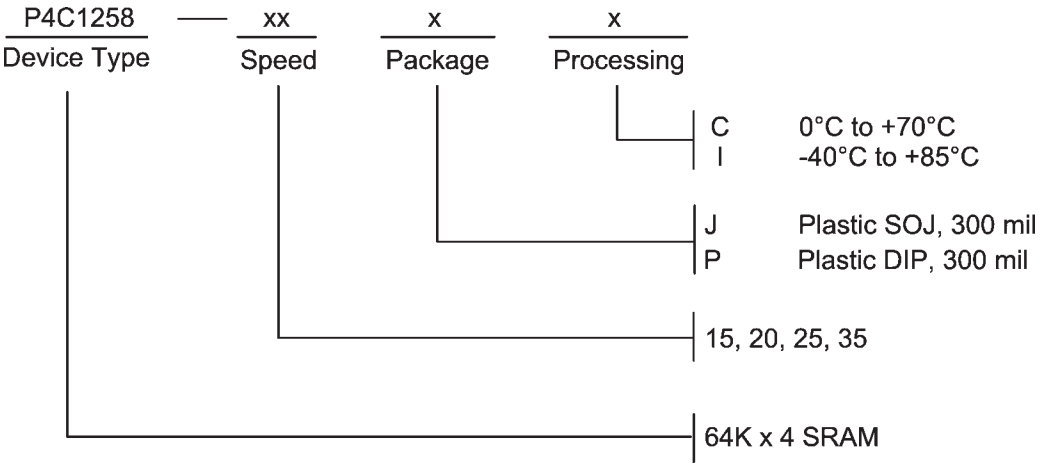



**Figure 2. Thevenin Equivalent**

* including scope and test fixture.

**Note:**
Because of the ultra-high speed of the P4C1258, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the $V_{CC}$ and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between $V_{CC}$ and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with $D_{OUT}$ to match 166Ω (Thevenin Resistance).

## ORDERING INFORMATION



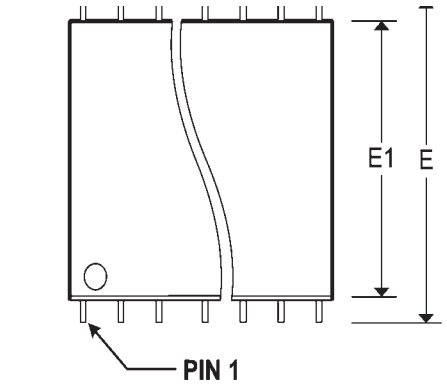

## SELECTION GUIDE

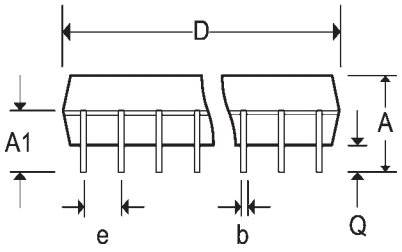
The P4C1258 is available in the following temperature, speed and package options.

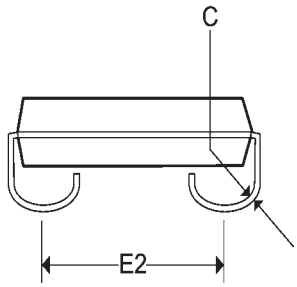
| Temperature Range | Package | Speed | | | |
|---|---|---|---|---|---|
| | | 15 | 20 | 25 | 35 |
| Commercial | Plastic DIP | -15PC | -20PC | -25PC | -35PC |
| | Plastic SOJ | -15JC | -20JC | -25JC | -35JC |
| Industrial | Plastic DIP | -15PI | -20PI | -25PI | -35PI |
| | Plastic SOJ | -15JI | -20JI | -25JI | -35JI |

| Pkg # | J4 | |
|---|---|---|
| # Pins | 24 (300 mil) | |
| Symbol | **Min** | **Max** |
| A | 0.128 | 0.148 |
| A1 | 0.082 | - |
| b | 0.016 | 0.020 |
| C | 0.007 | 0.010 |
| D | 0.620 | 0.630 |
| e | 0.050 BSC | |
| E | 0.335 BSC | |
| E1 | 0.292 | 0.300 |
| E2 | 0.267 BSC | |
| Q | 0.025 | - |

## SOJ SMALL OUTLINE IC PACKAGE

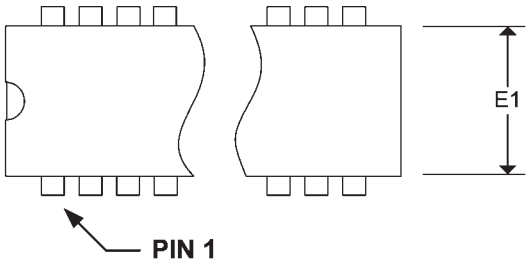


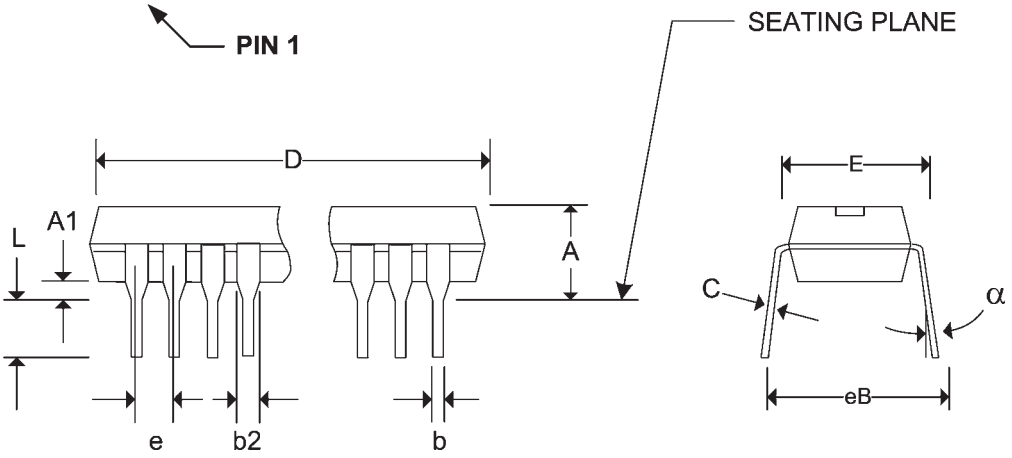




| Pkg # | P4 | |
|---|---|---|
| # Pins | 24 (300 Mil) | |
| Symbol | **Min** | **Max** |
| A | - | 0.210 |
| A1 | 0.015 | - |
| b | 0.014 | 0.022 |
| b2 | 0.045 | 0.070 |
| C | 0.008 | 0.014 |
| D | 1.230 | 1.280 |
| E1 | 0.240 | 0.280 |
| E | 0.300 | 0.325 |
| e | 0.100 BSC | |
| eB | - | 0.430 |
| L | 0.115 | 0.150 |
| $\alpha$ | 0° | 15° |

## PLASTIC DUAL IN-LINE PACKAGE



## REVISIONS

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER**: | SRAM123 | | |
| **DOCUMENT TITLE**: | P4C1258 ULTRA HIGH SPEED 64K x 4 STATIC CMOS RAM | | |
| **REV.** | **ISSUE DATE** | **ORIG. OF CHANGE** | **DESCRIPTION OF CHANGE** |
| OR | Oct-05 | JDB | New Data Sheet |
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