KK74LV174

Hex D-type flip-flop with reset; positive edge-trigger

The 74LV174 is a low–voltage Si–gate CMOS device and is pin and function compatible with the 74HC/HCT174.
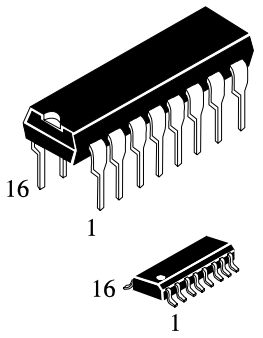
The 74LV174 has six edge–triggered D–type flip–flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip–flops simultaneously.

The register is fully edge–triggered. The state of each D input, one set–up time prior to the LOW–to–HIGH clock transition, is transferred to the corresponding output of the flip–flop.

A LOW level on the $\overline{MR}$ input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.2 to 5.5 V
- Low input current: 1.0 μA; 0.1 μA at T = 25 °C
- Output current: 6 mA at Vcc = 3.0 V; 12 mA at Vcc = 4.5 V
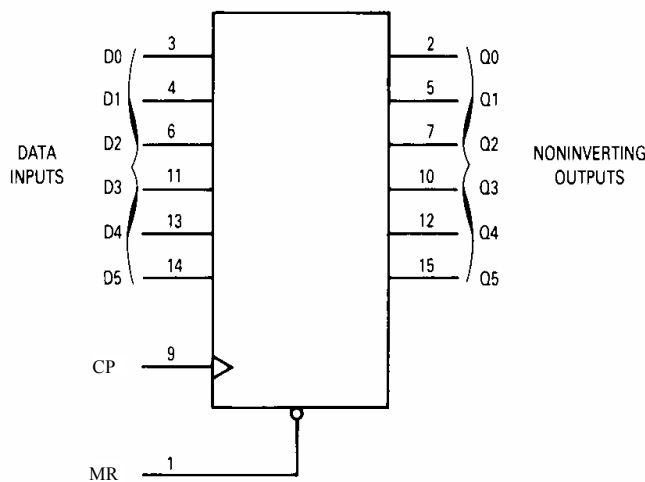- High Noise Immunity Characteristic of CMOS Devices

N SUFFIX
PLASTIC

D SUFFIX
SOIC

ORDERING INFORMATION

KK74LV174N Plastic
KK74LV174D SOIC
T_A = -40° to 125° C for all packages

LOGIC DIAGRAM

PIN 16=V_{CC}
PIN 08 = GND

PIN ASSIGNMENT

$\overline{MR}$	1 ○	16	V_{CC}
Q0	2	15	Q5
D0	3	14	D5
D1	4	13	D4
Q1	5	12	Q4
D2	6	11	D3
Q2	7	10	Q3
GND	8	9	CP

FUNCTION TABLE

Inputs			Outputs
$\overline{MR}$	CP	Dn	Qn
L	X	X	L
H	⟋	H	H
H	⟋	L	L
H	L	X	no change
H	⟍	X	no change

H= high level
L = low level
X = don't care

MAXIMUM RATINGS[*]

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *[1]	Input diode current	±20	mA
I_{OK} *[2]	Output diode current	±50	mA
I_O *[3]	Output source or sink current	±25	mA
I_{CC}	V_{CC} current	±50	mA
I_{GND}	GND current	±50	mA
P_D	Power dissipation per package: *[4] Plastic DIP SO	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

[*]Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*[1] V_I < -0.5 V or V_I > V_{CC} + 0.5 V
*[2] V_O < -0.5 V or V_O > V_{CC} + 0.5 V
*[3] -0.5 V < V_O < V_{CC} + 0.5 V
*[4] Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
        SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	5.5	V
V_{IN}	DC Input Voltage		0	V_{CC}	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	1.0 B ≤V_{CC} <2.0 B 2.0 B ≤V_{CC} <2.7 B 2.7 B ≤V_{CC} <3.6 B 3.6 B ≤V_{CC} ≤5.5 B	0 0 0 0	500 200 100 50	ns/V

        This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.
        Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			2.7	2.0	-	2.0	-	2.0	-	
			3.0	2.0	-	2.0	-	2.0	-	
			3.6	2.0	-	2.0	-	2.0	-	
			4.5	3.15	-	3.15	-	3.15	-	
			5.5	3.85	-	3.85	-	3.85	-	
V_{IL}	LOW level input voltage		1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			2.7	-	0.8	-	0.8	-	0.8	
			3.0	-	0.8	-	0.8	-	0.8	
			3.6	-	0.8	-	0.8	-	0.8	
			4.5	-	1.35	-	1.35	-	1.35	
			5.5	-	1.65	-	1.65	-	1.65	
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} $I_O = -100\ \mu A$	1.2	1.05	-	1.0	-	1.0	-	V
			2.0	1.85	-	1.8	-	1.8	-	
			2.7	2.55	-	2.5	-	2.5	-	
			3.0	2.85	-	2.8	-	2.8	-	
			3.6	3.45	-	3.4	-	3.4	-	
			4.5	4.35	-	4.3	-	4.3	-	
			5.5	5.35	-	5.3	-	5.3	-	
		$V_I = V_{IH}$ or V_{IL} $I_O = -6\ mA$	3.0	2.48	-	2.34	-	2.20	-	V
		$V_I = V_{IH}$ or V_{IL} $I_O = -12\ mA$	4.5	3.70	-	3.60	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} $I_O = 100\ \mu A$	1.2	-	0.15	-	0.2	-	0.2	V
			2.0	-	0.15	-	0.2	-	0.2	
			2.7	-	0.15	-	0.2	-	0.2	
			3.0	-	0.15	-	0.2	-	0.2	
			3.6	-	0.15	-	0.2	-	0.2	
			4.5	-	0.15	-	0.2	-	0.2	
			5.5	-	0.15	-	0.2	-	0.2	
		$V_I = V_{IH}$ or V_{IL} $I_O = 6\ mA$	3.0	-	0.33	-	0.40	-	0.50	V
		$V_I = V_{IH}$ or V_{IL} $I_O = 12\ mA$	4.5	-	0.40	-	0.55	-	0.65	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	5.5	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V $I_O = 0\ \mu A$	5.5	-	8.0	-	80	-	160	μA
I_{CC1}	Additional quiescent supply current per input	$V_I = V_{CC} -$ 0.6 V	2.7	-	0.2	-	0.5	-	0.85	mA
			3.6		0.2		0.5		0.85	

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, R_L = 1 kΩ, t_r=t_f=2.5 ns)

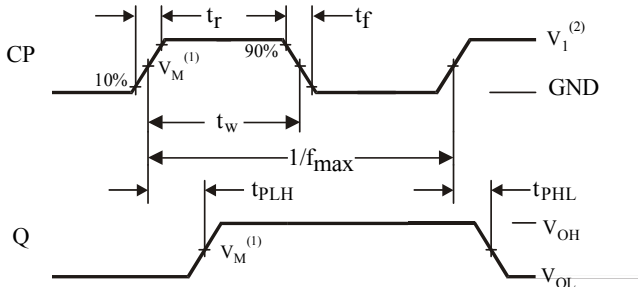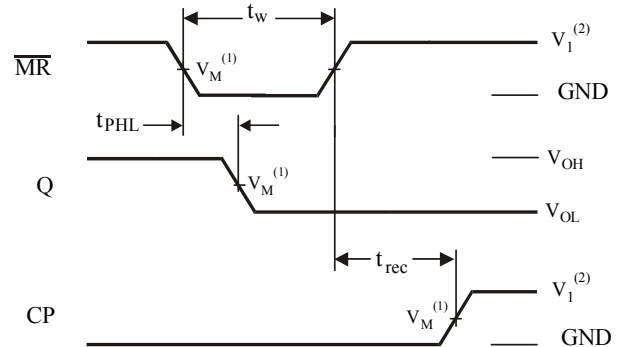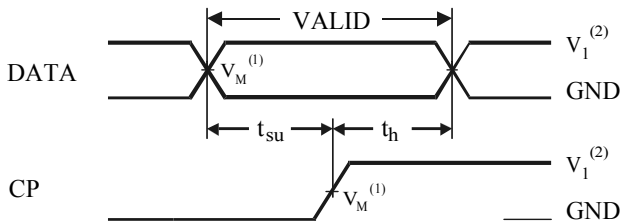| Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay CP to Qn	V_I = 0 V or V_{CC} Figure 1, 4	1.2	-	200	-	230	-	260	ns
			2.0	-	34	-	43	-	53	
			2.7	-	24	-	31	-	39	
			3.0	-	20	-	25	-	31	
			4.5	-	17	-	21	-	26	
t_{PHL}	Propagation delay MR to Qn	V_I = 0 V or V_{CC} Figure 2, 4	1.2	-	160	-	190	-	220	ns
			2.0	-	34	-	43	-	53	
			2.7	-	24	-	31	-	39	
			3.0	-	20	-	25	-	31	
			4.5	-	17	-	21	-	26	
t_W	Clock pulse width HIGH or LOW	V_I = 0 V or V_{CC} Figure 1, 4	1.2	100	-	140	-	180	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	14	-	17	-	20	-	
t_W	Master reset pulse width LOW	V_I = 0 V or V_{CC} Figure 1, 4	1.2	100	-	140	-	180	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	17	-	20	-	24	-	
			4.5	14	-	17	-	20	-	
t_{REM}	Removal time MR to CP	V_I = 0 V or V_{CC} Figure 3, 4	1.2	40	-	60	-	80	-	ns
			2.0	19	-	22	-	26	-	
			2.7	13	-	16	-	19	-	
			3.0	11	-	13	-	15	-	
			4.5	9	-	11	-	13	-	
t_{SU}	Set-up time Dn to CP	V_I = 0 B or V_{CC} Рисунок 3, 4	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
t_h	Hold time Dn to CP	V_I = 0 B or V_{CC} Рисунок 2, 4	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
C_I	Input capacitance	T_A = 25°C	5.0	-	7.0	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per flip-flop)	V_I = 0 V or V_{CC} T_A = 25°C	5.5	-	34	-	-	-	-	pF
fmax	Maximum clock pulse frequency	V_I = 0 B or V_{CC} Рисунок 1	1.2	-	2.0	-	1.0	-	1.0	MHz
			2.0	-	16	-	14	-	12	
			2.7	-	22	-	19	-	16	
			3.0	-	27	-	24	-	20	
			4.5	-	32	-	27	-	24	

Figure 1. Switching Waveforms

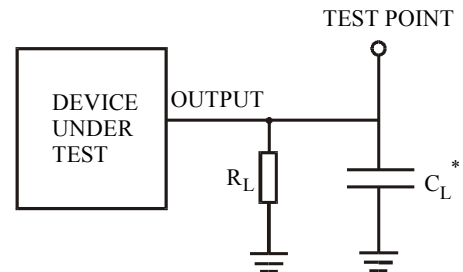
Figure 2. Switching Waveforms
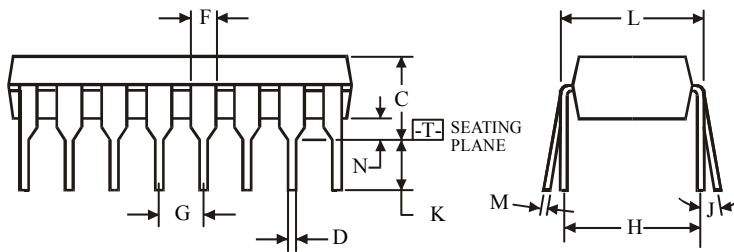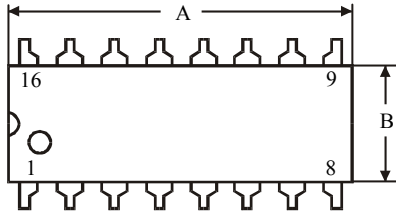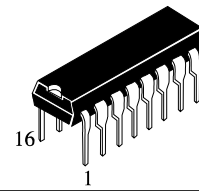

Figure 3. Switching Waveforms

* Includes all probe and jig capacitance

Figure 4. Test Circuit

Note:

(1) V_M = 1.5 V at V_{CC} = 2.7 V
   V_M = 0.5 $\cdot V_{CC}$ at V_{CC} =1.2 V, 2.0 V, 3.0 V, 4.5 V
(2) V_1 = V_{CC} at V_{CC} =1.2 V, 2.0 V, 2.7 V, 4.5 V
   V_1 = 2.7 V at V_{CC} = 3.0 V

K DENSHI

N SUFFIX PLASTIC DIP
(MS - 001BB)

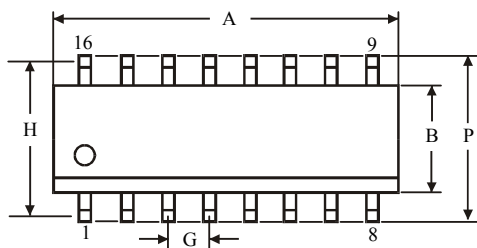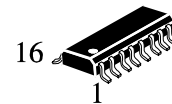|	Dimension, mm	
Symbol	**MIN**	**MAX**
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

⊕ 0.25 (0.010)Ⓜ T

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AC)

	Dimension, mm	
Symbol	**MIN**	**MAX**
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

⊕ 0.25 (0.010)Ⓜ T CⓂ

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.

2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.