AEAS - 7500

Ultra-Precision 16 bit Gray Code Absolute Encoder Module

Data Sheet

Description

The encoder IC consists of 13 signal photo diode channels and 1 monitor photo diode channel and is used for the optical reading of rotary or linear code carriers (i.e. discs or scales). The photodiodes are accompanied with precision amplifiers plus additional circuitry.

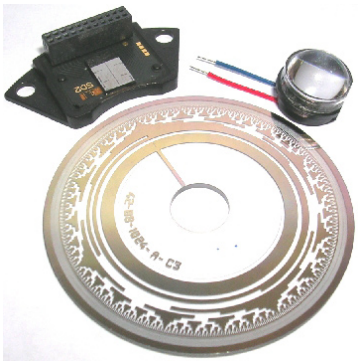
The monitor channel is used to drive a constant current source for the highly collimated IR illumination system.

Functional Description

Background

The 13 signal channels are set up as:

1. Two precision defining signals (A0, A09), which are two 90° electrical shifted sine, cosine signals. These signals are conditioned to be compensated for offset and gain errors. After conditioning they are on-chip interpolated and computed to a combined absolute 16 bit Gray code, together with signal channels A1-A11.
2. 11 analog (A1-A11) channels, which are directly digitized by precision comparators with hysteresis tracking. The digitized signals are called D1-D11.
3. An internal correction and synchronization module allows the composition of a true 16 bit gray code by merging the data bits of (1) and (2) by still keeping the code monotonic.
4. There is a Gray code correction feature for this encoder. This Gray code correction can be disabled/enabled by the pin KORR.
5. The gain and offset conditioning value of the sine and cosine signals are preloaded on-chip by factory. This will minimize mechanical sensor misalignment error.



Features

- Two Sine/Cosine true differential outputs with 1024 periods for unit alignment
- Integrated highly collimated illumination system
- 11 digital tracks plus 2 sin/cos tracks generate precise 16 bit Gray code
- Ultra fast, 1µs cycle for serial data output word equals 16MHz
- The 12 bits MSB is functionable up to 12000 RPM, 16 bit up to 1000RPM
- MSB can be inverted for changing the counting direction
- Monitor track for tracking the light level of the LED
- Watch dog with alarm output pin LERR
- -25 °C to + 85 °C operating temperature

Benefits

- No battery or capacitor required for position detection during power failure
- Immediate position detection on power up

Applications

- Rotary application up to 16 bits / 360° absolute position
- Cost effective solution for direct integration into OEM systems
- Linear positioning system

Signal-channels A1-A11

The photocurrent of the photodiodes is fed into a transimpedance amplifier. The analog output of the amplifier has a voltage swing of(dark/light) about 1.3V. Every output is transformed by precision comparators into digital signals (D1-D11). The threshold is at VDD/2(=Analog-reference), regulated by the monitor channel.

Monitor Channel with LED Control at pins LEDR and LERR

The analog output signal of the monitor channel is regulated by the LED current. An external bipolar transistor(to be connected by user) sets this level to VDD/2 (control voltage at pin LEDR). Thus the signal swing of each output is symmetrical to VDD/2(=Analog-reference)

The error bit at pin LERR is triggered if the Ve of the internal bipolar transistor is larger than VDD/2

Signals Channels A0, A09 with signal conditioning and calibration

These two channels give out a sine and cosine wave, which are 90 degree phase shifted. These signals have amplitudes, which are almost constant due to the LED current monitoring. Due to amplifier mismatch and mechanical misalignment the signals have gain and offset errors. These errors are eliminated by an adaptive signal conditioning circuitry. The conditioning values are on-chip preprogrammed by factory. The analog output signals of A0 and A09 are supplied as true-differential voltage with a peak to peak value of 2.0V at the pins A09P, A09N, A0P, A0N.

Interpolator for Channels A0,A09

The interpolator generates the digital signals D0,D09 and D-1 to D-4. The interpolated signals D-1 to D-4 extend the 12 bit Gray code of the signals D11….D0 to form a 16 bit Gray code.

D0 and D09 are digitized from A0 and A09. The channels A0-A11 and A09 have very high dynamic bandwidth, which allows a real time monotone 12Bit Gray code at 12000 RPM.

The interpolated 16 bit Gray code can be used up to 1000RPM only. At more than 1000RPM, only the 12 bit Gray code from the MSB side can be used.

LSB gray code Correction (Pin KORR)

This function block synchronizes the switching points for the 11 bit gray code of the digital signals D1 to D11 with D0 and D09 (digitized signal of A0 and A09).

The accuracy of the complete 12 bit gray is defined by the precision of the signals D0/D09. As these two signals are generated by the gain and offset conditioned analog signals A0 and A09, they are very precise.

This Gray code correction only works for the full 12 bit (4096 steps per revolution).

The correction is not for the 4 excess interpolated bits of the 16 bit Gray code. Gray code correction can be switched on or off by putting the pin KORR =1(on) or =0(off).

MSBINV and DOUT pins

The serial interface consists of a shift register. The most significant bit, MSB(D11) will always be sent first to DOUT. The MSB can be inverted (change code direction) by using pin MSBINV.

DIN and NSL pins

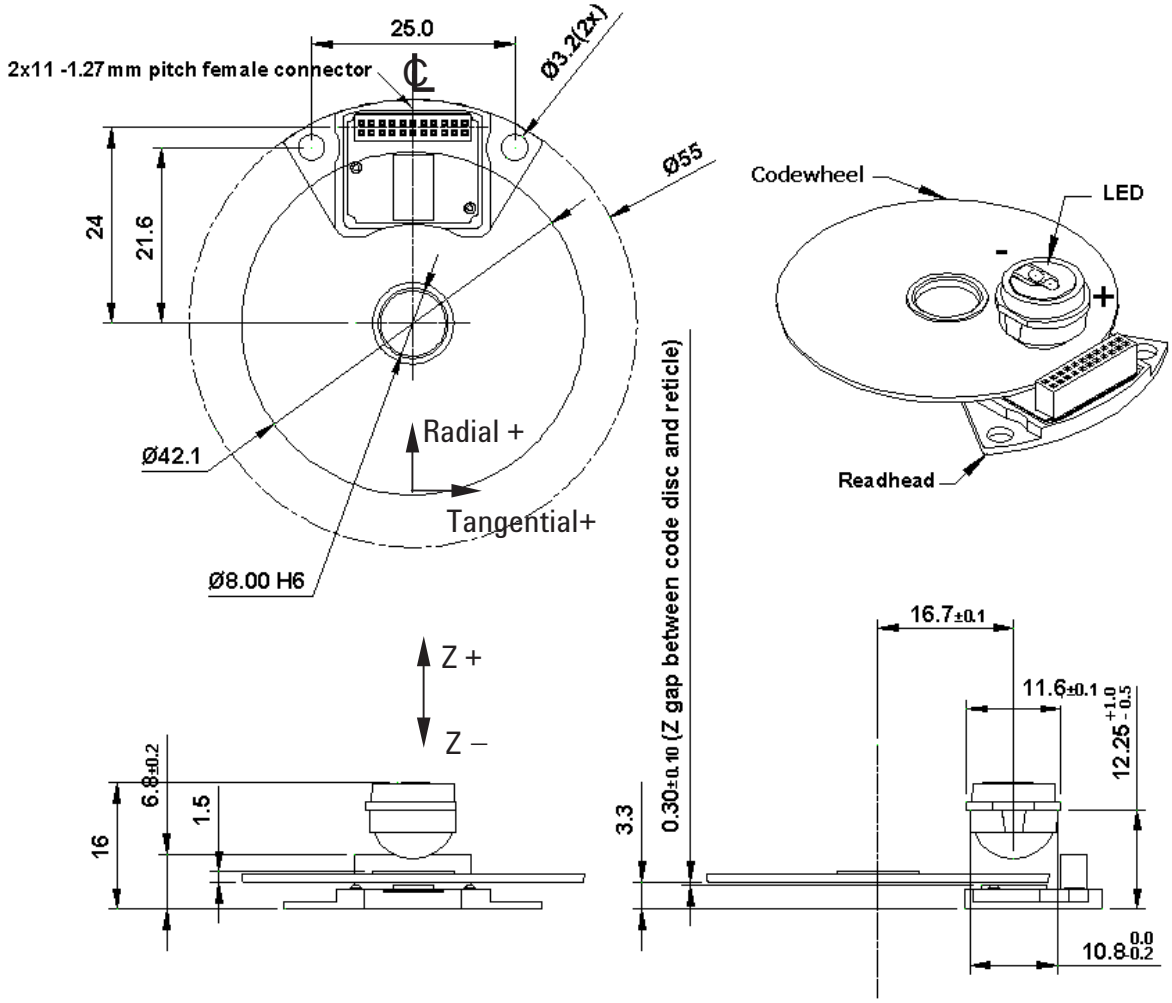
The Serial input DIN allows the configuration as ring register for multiple transmissions or for cascading 2 or more encoders. DIN is the input of the shift register that shifts the data to DOUT.

The NSL pin controls the shift register, to switch it between load (1) or shift(0) mode. Under load mode, DOUT will give the logic of the MSB, i.e. D11.

Under shift mode (0), coupled with the SCL, the register will be clocked, and gives out the serial word output bit by bit. As the clock frequency can be up to 16 MHz, the transmission of the full 16 bit word can be done within 1 µs.

Valid data of DOUT should be read when the SCL clock is low. Please refer to timing diagram Figure 4.

Package Dimensions



Notes:
1. 3rd Angle Projection
2. Dimensions are in millimeters
3. Unless specified otherwise, the tolerances are: XX. – ±0.5; XX.X – ±0.2; XX.XX – ±0.03
4. Note: Codewheel and readhead mounting tolerances for radial, tangential and Z gap are:
   Radial : ± 50 um
   Tangential : ± 40um
   Z Gap : ± 50um

Figure 1. Package Dimensions

Device Selection Guide [1]

Part Number	Resolution	Operating Temperature (°C)	Output	Output Code	DC Supply Voltage (V)
AEAS-7500-1GSG0	16 bit	-25 to 85	SSI + 1024 Sine/Cosine Incremental	Gray Code	+4.5 to +5.5

Notes:
1. For other options of absolute encoder module, please refer to factory.

Absolute Maximum Ratings [1, 2]

Parameter	Symbol	Limits	Units
DC Supply Voltage	VD	-0.3 to + 6.0	V
Input Voltage	V_{in}	-0.3 to +VD +0.3	V
Output Voltage	V_{out}	-0.5 to +VD +0.3	V
Moisture Level (Non-Condensing)	%RH	85	%
Operating Temperature	T_A	-25 to 85	°C
Storage Temperature	T_S	- 40 to 100	°C

Notes:
1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Condition

		Values				
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
DC Supply Voltage	VD	+ 4.5	+ 5.0	+5.5	V	1
Operating Temperature	T_A	- 25	25	+85	°C	
Input High Level	V_{IH}	0.7*VD		VD	V	
Input Low Level	V_{LH}	0		0.3*VD	V	

Notes:
1. Voltage ripple of supply voltage, V_{ripple}, should be within 100mVpp or less for improved accuracy.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at T_A=25 °C and VD = 5V

			Values			
Parameter	**Symbol**	**Condition**	**Min**	**Typ.**	**Max**	**Units**
Total Operating Current	I_{total}			25		mA
Digital Input-Pull Down Current	I_{pd}		-20		-5	mA
Digital Input-Pull Up Current	I_{pu}		30		160	mA
Digital Ouput-H-Level	V_{OH}	I_{OH} = 2 mA	VD -0.5 V		VD	V
Digital Ouput-L-Level	V_{OL}	I_{OL} = - 2 mA	0		0.5	V
SCL Clock Frequency	f_{SCL}				16	MHz
Duty Cycle SCL Clock	T_{LH}	T_{LH} = H/(L+H)	0.4		0.6	
Accuracy within one revolution [1, 2, 3]		f_{SCL} = 5MHz RPM =80 V_{ripple} <50mVpp		±2 bit		
Signal frequency of A0, A09	f_{A0}, f_{A09}				250	kHz

Notes:
1. LSB accuracy will also depend on mechanical precision of the shaft, bearings, hub etc. As the AEAS-7500 is a detached encoder set as different from AEAS-7000 series, which are modular, where final testing, programming and assembly take place at the customer facility, final accuracies of the encoder cannot be guaranteed by Avago.
2. Accuracy would be influenced by installation control and the bearing and shaft type being used.
3. Other test conditions to determine accuracy are briefly listed as follows:
   (a) At nominal radial, tangential and gap position
   (b) On dual preloaded bearing with absolute assembly total runout of not exceeding 0.01 mm TIR
   (c) Both VDD & VDDA RC filters placed not more than 20mm from header pins

Pin Description

No.	Pin Name	Description	Function	Notes
1	NC		Do not use	
2	KORR	Digital-input	1 = Gray Code Correction Active	CMOS, internal pu
3	PROBE_ON	Digital-Input	Do not use	CMOS, internal pd
4	PCL	Digital Input Positive edge	Do not use	CMOS, internal pu
5	STCAL	Digital Input Positive edge Negative edge	Do not use unnecessarily	CMOS, internal pd
6	MSBINV	Digital-Input	1 = Most Significant Bit, MSB, inverted	CMOS, internal pd
7	DIN	Digital Input	Shift Register Input. Use for cascading only.	CMOS, internal pd
8	NSL	Digital-Input	Shift-register Shift (=0) / Load(=1) Control	CMOS, internal pu
9	SCL	Digital-Input Positive Edge	Shift-register Clock	CMOS, internal pu
10	DOUT	Digital Output	Shift-Register Data Out (MSB first)	CMOSS, 2mA
11	DO	Digital Output	DO signal	CMOS, 2mA
12	DPROBE	Digital Output	DO9 signal	CMOS, 2mA
13	VDD	Supply Voltage	+5V Supply Digital	
14	GND	Ground for supply voltage	GND for 5V supply analog/digital	
15	A09P	Analog output	A09 positive(+True diff.)	CMOS, analog out
16	GND	Ground for supply voltage	GND for 5V supply analog/digital	
17	A0P	Analog Output	A0 positive(+True diff.)	CMOS, analog out
18	A09N	Analog output	A09 negative(-True diff.)	CMOS, analog out
19	VDDA	Supply Voltage	+5V Supply Analog	
20	A0N	Analog Output	A0 negative (- True dif)	CMOS, analog out
21	LERR	Digital Output	IR-LED Current Limit Signal	CMOS, 2mA
22	LEDR	Analog Output	To be connected by user to the base of a NPN transistor with a series resistor as per Figure 5	CMOS, analog out

Notes:
1. Internal pu/pd = internal pull-up (typ. 50uA)/ pull-down (typ. 10uA) CMOS-transistor-Rs

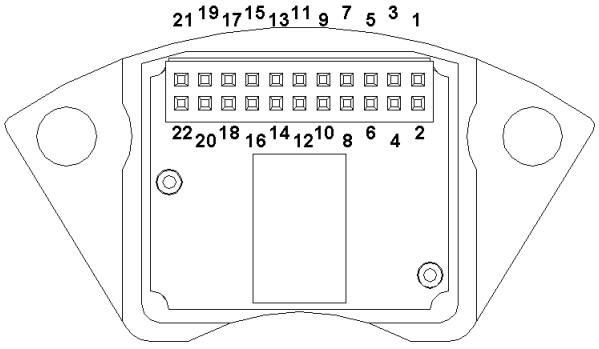
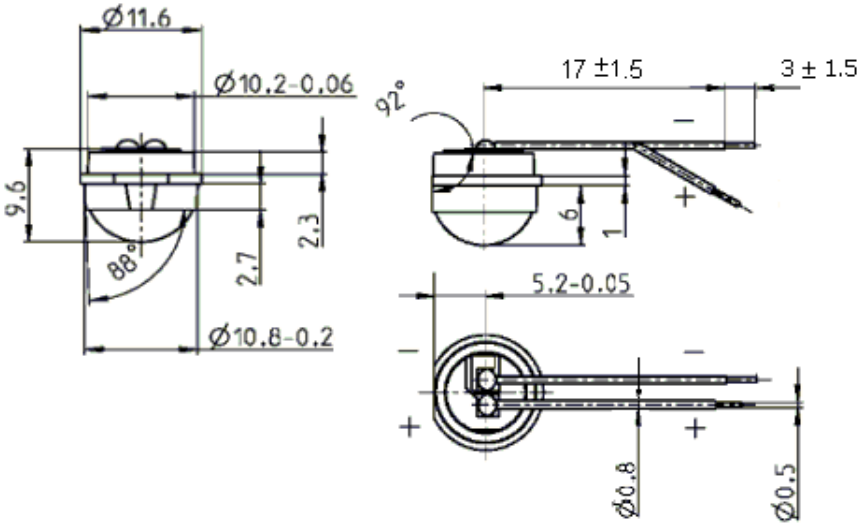


Figure 2. Pinout Configuration

LED Module Dimensions



Notes:
1 3rd Angle Projection
2. Dimensions are in millimeters
3. LED Module spatial misalignment tolerance absolute limits are as follows: (Refer to Figure 1 for directional indication)
   (a) Radial limit from nominal : ± 0.4 mm
   (b) Tangential limit from nominal : ± 0.4 mm
   (c) LED module placement height at Z direction : + 1 mm, - 0.5 mm (as long as no contact with codewheel)
   (d) Tilting at XZ plane along PDA or Center line (CL) : ± 1 degree

Figure 3. LED Module Dimensions

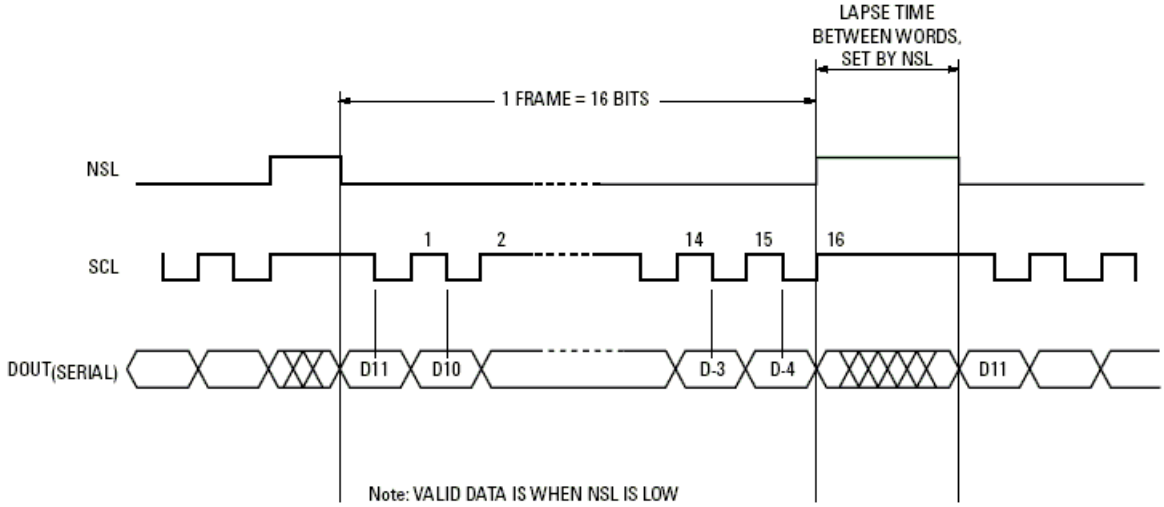


Figure 4. Timing Diagram

Using the AEAS-7500

IMPORTANT NOTE: The RC-filter combination, especially on VDDA, is used to filter spikes and transients and is strongly recommended. It is advised that the tantalum caps be put as close to the VDD and VDDA pins as possible.

It is recommended to ground the PROBE_ON pin during normal operation.

Leave PCL unconnected. A09N and A0N are the negative cosine and sine waves, the negative versions of A09P and A0P.

D0 is used to check the D0 signal. D0 is the digitized signal of A0. DPROBE is used to check D09, the digitized signal of A09. Recommended to be used for testing purpose only.

KORR is for Gray Code correction for 12 bits resolution only.

MSBINV is for user to change between counting up and counting down for a given rotating direction. MSB(D11) will always be sent out to DOUT first

LEDR is an internal voltage monitor which is linked to the Monitor channel. It should be connected to the base of an NPN transistor via a series resistor to control the LED brightness per the photodiodes' need. (Refer to Figure 5)

LERR will be high when the light output perceived by the photo diode array is low, and the LED current is under overdrive mode. This is an indicator when light intensity is at a critical stage affecting the performance of the encoder. It is caused either by contamination of the codewheel or LED degradation.

Operation

After powering up the unit using VD =+5V and connecting GND to ground, trigger input pins NSL and SCL using the timing diagram (Figure 4). NSL is a control pin for the internal shift register. NSL=1 is load mode while NSL=0 is shift mode for the shift register. When NSL=0 and combined with clock pulses, the serial Gray code will be shifted out to DOUT bit by bit per every clock pulse. Valid data of DOUT should be sampled at the low point of the clock pulses.

The 16 bit serial gray code can be tapped out from pin DOUT, most significant bit (D11) first. The rate of the 16bit Gray code serial transfer rate is dependent on the SCL clock frequency. The faster the clock, the faster the transfer rate. The maximum clock rate the AEAS-7500 can take is 16 MHz, which means the entire 16 bit Gray code can be serially transferred out in 1 us.

Whenever NSL is high (load mode), the DOUT will have the logic of the MSB (D11). After NSL goes low, the number of bits being transferred out will depend on the number of clock pulses given to SCL. The default is 16 clock pulses for the 16 bit Gray code.

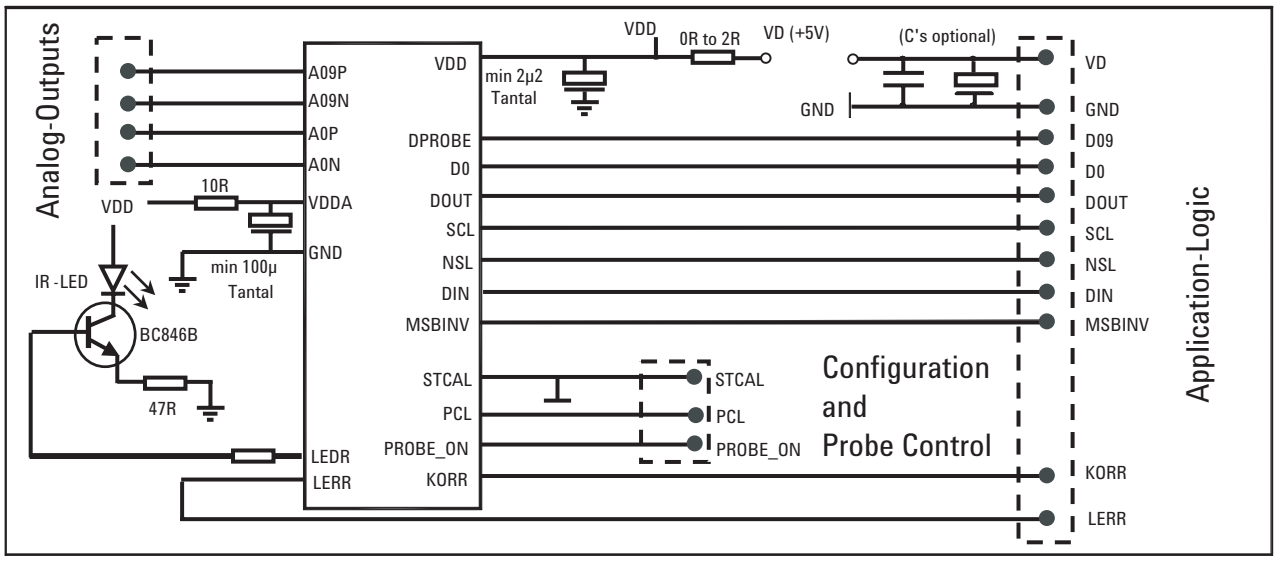


Figure 5. Schematic for using AEAS-7500

Ordering Information

AEAS-7500-1GSG0

Single-turn, -25 to +85ºC, detached encoder set, 5V, serial, 16 bit

Note:
For alignment process, please refer to Avago Technologies' website for application note or contact factory.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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