OPB 16450 UART

DS433 August 18, 2004 **Product Specification**

Introduction

This document provides the specification for the OPB Universal Asynchronous Receiver/Transmitter (UART) Intellectual Property (IP).

The UART described in this document has been designed incorporating the features described in *National Semiconductor PC16550D UART with FIFOs* data sheet (June, 1995), (http://www.national.com/pf/PC/PC16550D.html).

The National Semiconductor PC16550D data sheet is referenced throughout this document and should be used as the authoritative specification. Differences between the National Semiconductor implementation and the OPB UART Point Design implementation are highlighted and explained in Specification Exceptions

Features

- Hardware and software register compatible with all standard 16450 UARTs
- Implements all standard serial interface protocols
  - 5, 6, 7, or 8 bits per character
  - Odd, Even, or no parity detection and generation
  - 1, 1.5, or 2 stop bit detection and generation
  - Internal baud rate generator and separate receiver clock input
  - Modem control functions
  - False start bit detection and recovery
  - Prioritized transmit, receive, line status, and modem control interrupts
  - Line break detection and generation
  - Internal loop back diagnostic functionality
- Registers
  - Receiver Buffer Register (Read Only)
  - Transmitter Holding Register (Write Only)
  - Interrupt Enable Register
  - Interrupt Identification Register (Read Only)
  - Line Control and Line Status Registers
  - Modem Control and Modem Status Registers
- Scratch Register
  - Divisor Latch (least and more significant byte)

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-II Pro™, Virtex™, Virtex-II™, Virtex-4™, QPro™-R Virtex-II, QPro Virtex-II, Virtex-E, Spartan-II™, Spartan-IIE™, Spartan-3™	
Version of Core	opb_uart16450	v1.00c
Resources Used		
	Min	Max
Slices	341	341
LUTs	357	357
FFs	347	347
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification.	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

- System clock frequency of 100 MHz

UART Background

The OPB 16450 performs parallel to serial conversion on characters received from the CPU and serial to parallel conversion on characters received from a modem or microprocessor peripheral.

The OPB 16450 is capable of transmitting and receiving 8, 7, 6, or 5 bit characters, with 2, 1.5 or 1 stop bits and odd, even or no parity. The OPB 16450 can transmit and receive independently.

The device can be configured and it's status monitored via the internal register set. The OPB 16450 is capable of signaling receiver, transmitter and modem control interrupts. These interrupts can be masked, are prioritized and can be identified by reading an internal register.

16450 UART Design Parameters

To allow you to obtain an OPB UART that is uniquely tailored for your system, certain features can be parameterized in the OPB UART design. This allows you to have a design that only utilizes the resources required by your system and runs at the best possible performance. The features that can be parameterized in the Xilinx OPB UART design are shown in Table 1.

Table 1: **Design Parameters**

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
OPB Interface	G1	OPB UART Base Address	C_BASEADDR	Valid Word Aligned Address. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1.	A0000000	std_logic_vector
	G2	OPB Data Bus Width	C_OPB_DWIDTH	32	32	integer
	G3	OPB Address Bus Width	C_OPB_AWIDTH	32	32	integer
	G4	Device Block ID(1)	C_DEV_BLK_ID	0-255	0	integer
	G5	Module Identification Register (1)	C_DEV_MIR_ENABLE	0,1.	0	integer
	G6	OPB UART High Address	C_HIGHADDR	C_HIGHADDR -C_BASEADDR must be a power of 2 >= to C_BASEADDR+1FFF	A0001FFF	std_logic_vector
UART Features	G7	External XIN	C_HAS_EXTERNAL_XIN	0,1	0	integer
	G8	External RCLK	C_HAS_EXTERNAL_RCLK	0,1	0	integer
	G9	Select UART	C_IS_A_16550	0,1	1	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

UART I/O Signals

The I/O signals for the UART are listed in Table 2. The interfaces referenced in this table are shown in Figure 1 in the UART block diagram.

Table 2: **UART I/O Signals**

Grouping		Signal Name	Interface	I/O	Initial diagram State	Description
OPB Slave Signals	P1	OPB_ABus(0:C_OPB_AWIDTH-1)	IPIF	I		OPB Address Bus
	P2	OPB_BE(0:(C_OPB_AWIDTH/8)-1)	IPIF	I		OPB Byte Enable
	P3	OPB_DBus(0:C_OPB_DWIDTH-1)	IPIF	I		OPB Data Bus
	P4	OPB_RNW	IPIF	I		Read Not Write
	P5	OPB_Select	IPIF	I		OPB Select
	P6	OPB_seqAddr	IPIF	I		OPB sequential address (unused)
	P7	Sln_DBus(0:C_OPB_DWIDTH-1)	IPIF	O	0	Output Data Bus
	P8	Sln_ErrAck	IPIF	O	0	Slave Error Acknowledge (always inactive)
	P9	Sln_Retry	IPIF	O	0	Slave Bus Cycle Retry (always inactive)
	P10	Sln_ToutSup	IPIF	O	0	Slave Time Out Suppress (always inactive)
	P11	Sln_XferAck	IPIF	O	0	Slave Transfer Acknowledge
	P12	IP2INTC_Irpt	IPIF	O	0	IPIF interrupt Output

Table 2: **UART I/O Signals *(Continued)***

Grouping		Signal Name	Interface	I/O	Initial diagram State	Description
UART Signals	P13	baudoutN	Serial	O	1	Transmitter Clock
	P14	rclk	Serial	I		Receiver 16x Clock (Optional. May be driven by baudoutN under control of the C_HAS_EXTERNAL_RCLK parameter).
	P15	sin	Serial	I		Serial Data Input
	P16	sout	Serial	O	1	Serial Data Output
	P17	xin	Serial	I		Baud Rate Generator reference clock. (Optional. May be driven by OPB_Clk under control of the C_HAS_EXTERNAL_XIN parameter).
	P18	xout	Serial	O	~XIN	Inverted XIN
	P19	ctsN	Modem	I		ClearToSend (active low)
	P20	dcdN	Modem	I		Data Carrier Detect (active low)
	P21	dsrN	Modem	I		Data Set Ready (active low)
	P22	dtrN	Modem	O	1	Data Terminal Ready (active low)
	P23	riN	Modem	I		Ring Indicator (active low)
	P24	rtsN	Modem	O	1	Request To Send (active low)
	P25	ddis	User	O	1	Driver Disable. Low when CPU is reading OPB UART
	P26	out1N	User	O	1	User controlled output
	P27	out2N	User	O	1	User controlled output
	P28	rxrdyN	User	O	1	DMA control signal
	P29	txrdyN	User	O	1	DMA control signal
System	P30	OPB_Clk	System	I		System clock
	P31	OPB_Rst	System	I		System Reset (active high)
	P32	Freeze	System	I		Freezes UART for software debug (active high)

Parameter - Port Dependencies

The width of many of the OPB UART signals depends on parameter. In addition, when certain features are parameterized away, the related input signals are unconnected. The dependencies between the OPB UART design parameters and I/O signals are shown in Table 3. parameters and I/O signals are shown in the following table.

Table 3: **Parameter-Port Dependencies**

		Name	Affects	Depends	Relationship Description
Design Parameters	G1	C_BASEADDR		G3	Bus width affects maximum allowable address.
	G2	C_OPB_DWIDTH	P3, P7		Affects number of bits in bus.
	G3	C_OPB_AWIDTH	P1, P2		Affects number of bits in bus.
	G4	C_DEV_BLK_ID			
	G5	C_DEV_MIR_ENABLE			
	G6	D_HIGHADDR		G3	Bus width affects maximum allowable address.
	G7	C_HAS_EXTERNAL_XIN	P17		Connects XIN to OPB_CLK
	G8	C_HAS_EXTERNAL_RCLK	P14		Connects RCLK to baudoutN
	G9	C_IS_A_16550			
I/O Signals	P1	OPB_ABus(0:C_OPB_AWIDTH-1)		G3	Width varies with the size of the OPB Address bus.
	P2	OPB_BE(0:(C_OPB_AWIDTH/8)-1)		G3	Width varies with the size of the OPB Address bus.
	P3	OPB_DBus(0:C_OPB_DWIDTH-1)		G2	Width varies with the size of the OPB Data bus.
	P4	OPB_RNW			
	P5				
	P6	OPB_seqAddr			
	P7	Sln_DBus(0:C_OPB_DWIDTH-1)		G2	Width varies with the size of the OPB Data bus.
	P8	Sln_ErrAck			
	P9	Sln_Retry			
	P10	Sln_ToutSup			
	P11	Sln_XferAck			

Table 3: **Parameter-Port Dependencies *(Continued)***

		Name	Affects	Depends	Relationship Description
I/O Signals	P12	IP2INTC_Irpt(1)			UART Interrupt Signal
	P13	baudoutN			
	P14	rclkK		G8, P13	This input is unconnected and UART receiver clock is connected to BAUDOUTn if C_HAS_EXTERNAL_RCLK=0.
	P15	sin			
	P16	sout			
	P17	xin		G7, P30	This input is unconnected and UART reference clock is connected to OPB_Clk if C_HAS_EXTERNAL_XIN=0.
	P18	xout			
	P19	ctsN			
	P20	dcdN			
	P21	dsrN			
	P22	dtrN			
	P23	riN			
	P24	rtsN			
	P25	ddis			
	P26	out1N			
	P27	out2Nn			
	P28	rxrdyN			
	P29	txrdyN			
System	P30	OPB_Clk			
	P31	OPB_Rst			
	P32	Freeze			

UART Register Definition

UART Interface (IPIF)

The OPB memory map location of the OPB 16450 UART is determined by setting the parameter C_BASEADDR, in the IPIF interface module. The internal registers of the OPB 16450 UART are offset from the C_BASEADDR base address. Additionally, some of the internal registers are accessible only when bit 7of the Line Control Register (LCR) is set. The UART internal register set is described in Table 4.

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Table 4: **UART Registers**

Register Name	LCR(7)[1]+ C_BASEADDR + Address	Access
Receiver Buffer Register (RBR)	0 + C_BASEADDR + 0x1000	Read
Transmitter Holding Register (THR)	0 + C_BASEADDR + 0x1000	Write
Interrupt Enable Register (IER)	0 + C_BASEADDR + 0x1004	Read/Write
Interrupt Identification Register (IIR)	0 + C_BASEADDR + 0x1008	Read
Line Control Register (LCR)	X + C_BASEADDR + 0x100C	Read/Write
Modem Control Register (MCR)	X + C_BASEADDR + 0x1010	Read/Write
Line Status Register (LSR)	X + C_BASEADDR + 0x1014	Read/Write
Modem Status Register (MSR)	X + C_BASEADDR + 0x1018	Read/Write
Scratch Register (SCR)	X + C_BASEADDR + 0x101C	Read/Write
Divisor Register (DLL)	1 + C_BASEADDR + 0x1000	Read/Write
Divisor Register (DLM)	1 + C_BASEADDR + 0x1004	Read/Write

Notes:
1. X denotes a don't care

UART Register Logic

This section tabulates the internal UART registers, including their reset values (if any).

Please refer to the National Semiconductor *PC16550D UART with FIFOs* data sheet (June, 1995), (http://www.national.com/pf/PC/PC16550D.html) for a more detailed description of the register behavior.

Receiver Buffer Register

As shown in Table 5, the Receiver Buffer Register contains the last received character.

Table 5: **Receiver Buffer Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	RBR	Read	"00000000"	RBR. Last received character

Transmitter Buffer Register

As shown in Table 6, the Transmitter Holding Register contains the character to be transmitted next.

Table 6: **Transmitter Holding Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	THR	Write	"11111111"	THR. Holds the character to be transmitted next

Interrupt Enable Register

As shown in Table 7, the Interrupt Enable Register contains the bits which enable interrupts.

Table 7: **Interrupt Enable Register Bit Definitions(1)**

Bit Location	Name	Access	Reset Value	Description
7-4		Read/Write	“**0**"	
3	EDSSI	Read/Write	"0"	Enable Modem Status Interrupt. "0" -> Disables Modem Status Interrupts. "1" -> Enables Modem Status Interrupts.
2	ELSI	Read/Write	"0"	Enable Receiver Line Status Interrupt. "0" -> Disables Receiver Line Status Interrupts. "1" -> Enables Receiver Line Status Interrupts.
1	ETBEI	Read/Write	"0"	Enable Transmitter Holding Register Empty Interrupt. "0" -> Disables Transmitter Holding Register Empty Interrupts. "1" -> Enables Transmitter Holding Register Interrupts.
0	ERBFI	Read/Write	"0"	Enable Received Data Available Interrupt. "0" -> Disables Received Data Available Interrupts. "1" -> Enables Received Data Available Interrupts.

Notes:
1. Bold faced bits are permanently low. Writing to these bits is allowed. Reading always returns "0"

Interrupt Identification Register

As shown in Table 8, the Interrupt Identification Register contains the priority interrupt identification.

Table 8: **Interrupt Identification Register Bit Definitions(1)**

Bit Location	Name	Access	Reset Value	Description
7-4		Read	“**0000**"	Always returns "0000"
3-1	INTID2	Read	“000"	Interrupt ID. (2) "011" -> Receiver Line Status (Highest). "010" -> Received Data Available (Second). "110" -> Character Timeout (Second). "001" -> Transmitter Holding Register Empty (Third). "000" -> Modem Status (Fourth).
0	INTPEND	Read	“1"	Interrupt Pending. Interrupt is pending when cleared.

Notes:
1. Bold faced bits are permanently low. Reading these bits always return "0"
2. If bit 0 is cleared. See National Semiconductor PC16550D data sheet for more detail.

Line Control Register

As shown in Table 9, the Line Control Register contains the serial communication configuration bits.

Table 9: **Line Control Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7	DLAB	Read/Write	“0”	Divisor Latch Access Bit. "1" -> Allows access to the Divisor Latch Registers and reading of the FIFO Control Register.
6	Set Break	Read/Write	“0”	Set Break. "1" -> Sets SOUT to "0".
5	Stick Parity	Read/Write	“0”	Stick Parity. "1" -> Forces parity to "1" or "0" based on bits 3 and 4.
4	EPS	Read/Write	“0”	Even Parity Select. 1 -> Selects Even parity. 0-> Selects Odd parity.
3	PEN	Read/Write	“0”	Parity Enable. "1" -> Enables parity.
2	STB	Read/Write	“0”	Number of Stop Bits. "0" -> 1 Stop bit. "1" -> 2 Stop bits or 1.5 if 5 bits/character selected).
1-0	WLS	Read/Write	“00”	Word Length Select. "00" -> 5 bits/character. "01" -> 6 bits/character. "10" -> 7 bits/character. "11" -> 8 bits/character.

Modem Control Register

As shown in Table 10, the Modem Control Register contains the modem signaling configuration bits.

Table 10: **Modem Control Register Bit Definitions** (1)

Bit Location	Name	Access	Reset Value	Description
7-5		Read/Write	“**000**"	
4	Loop	Read/Write	"0"	Loop Back. "1" -> Enables loop back.
3	Out2	Read/Write	"0"	User Output 2. "1" -> Drives OUT2N low. "0" -> Drives OUT2N high.

Table 10: **Modem Control Register Bit Definitions (1)**

Bit Location	Name	Access	Reset Value	Description
2	Out1	Read/Write	"0"	User Output 1. "1" -> Drives OUT1N low. "0" -> Drives OUT1N high.
1	RTS	Read/Write	"0"	Request To Send. "1" -> Drives RTSN low. "0" -> Drives RTSN high.
0	DTR	Read/Write	"0"	Data Terminal Ready. "1" -> Drives DTRN low. "0" -> Drives DTRN high.

Notes:
1. Bold faced bits permanently low.

Line Status Register

As shown in Table 11, the Line Status Register contains the current status of the receiver and transmitter.

Table 11: **Line Status Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7	Error in RCVR FIFO	Read/Write	“0”	Error in RCVR FIFO. RCVR FIFO contains at least one receiver error.
6	TEMT	Read/Write	“0”	Transmitter Empty.
5	THRE	Read/Write	“1”	Transmitter Holding Register Empty.
4	BI	Read/Write	“1”	Break Interrupt. Set when SIN is held low for an entire character time.
3	FE	Read/Write	“0”	Framing Error. Character missing a stop bit. Receiver resynchs with next character, if possible.
2	PE	Read/Write	“0”	Parity Error.
1	OE	Read/Write	“0”	Overrun Error. RBR not read before next character is received.
0	DR	Read/Write	“0”	Data Ready.

Modem Status Register

As shown in Table 12, the Modem Status Register contains the current state of the Modem interface.

Table 12: **Modem Status Register Bit Definitions (1)**

Bit Location	Name	Access	Reset Value	Description
7	DCD	Read/Write	“X”	Data Carrier Detect. Complement of DCDN input.
6	RI	Read/Write	"X"	Ring Indicator. Complement of RIN input.
5	DSR	Read/Write	"X"	Data Set Ready. Complement of DSRN input.
4	CTS	Read/Write	"X"	Clear To Send. Complement of CTSN input.
3	DDCD	Read/Write	"0"	Delta Data Carrier Detect. Change in DCDN since last MSR read.
2	TERI	Read/Write	"0"	Trailing Edge Ring Indicator. RIN has changed from a low to a high.
1	DDSR	Read/Write	"0"	Delta Data Set Ready. Change in DSRN since last MSR read.
0	DCTS	Read/Write	"0"	Delta Clear To Send. Change in CTSN since last MSR read.

Notes:
1. X represents bit driven by external input.

Scratch Register

As shown in Table 13, the Scratch Register can be used to hold user data.

Table 13: **Scratch Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	Scratch	Read/Write	“00000000”	Scratch.

Divisor (Least Significant Byte) Register

As shown in Table 14, the Divisor (Least Significant Byte) Register holds the least significant byte of the baud rate generator counter.

Table 14: **Divisor (Least Significant Byte) Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	DLL	Read/Write	“00000000”	Divisor Least Significant Byte.

Divisor (Most Significant Byte) Register

As shown in Table 15, the Divisor (Most Significant Byte) Register holds the most significant byte of the baud rate generator counter.

Table 15: **Divisor (Most Significant Byte) Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	DLM	Read/Write	“00000000”	Divisor Most Significant Byte.

UART Block Diagram

The top-level block diagram for the UART is shown in Figure 1.

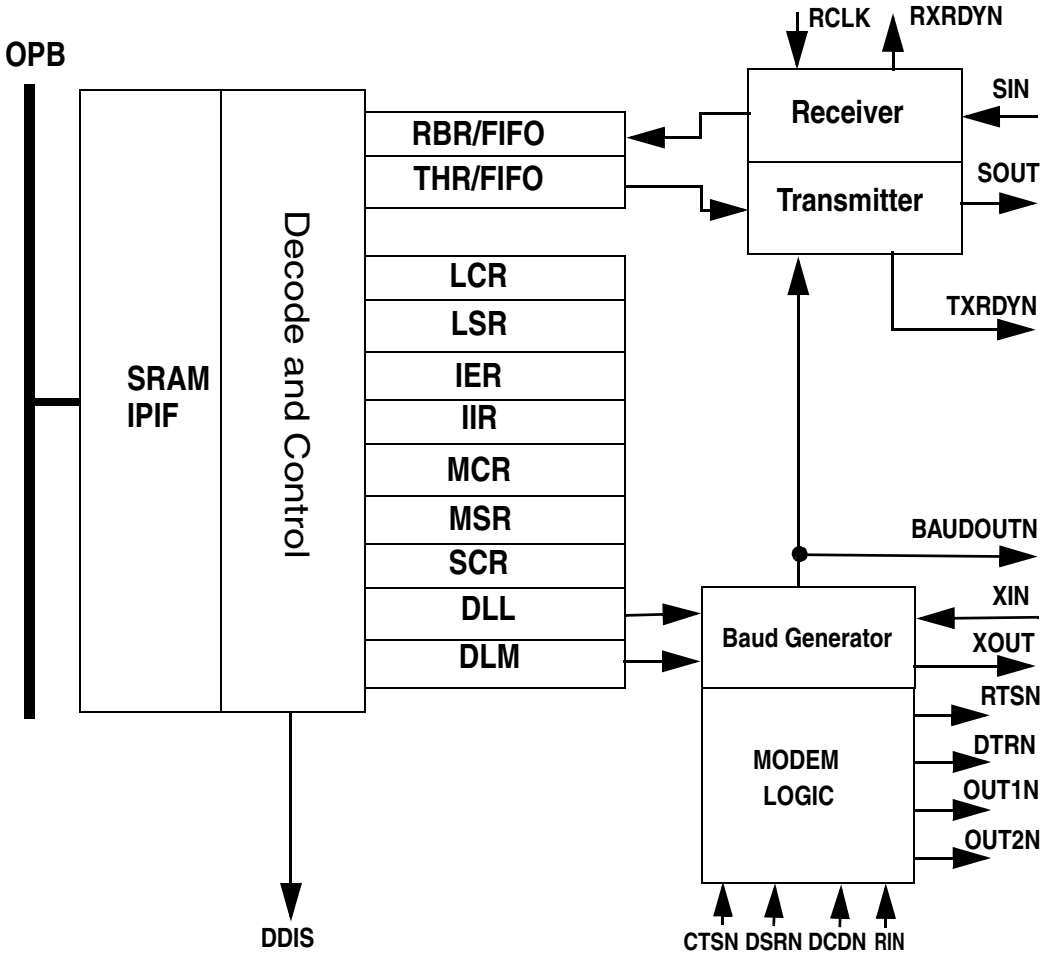

Figure 1: **UART Top-level Block Diagram**

Raw UART Interface

UART without an OPB interface

The raw UART interface (the OPB UART without the OPB IPIF) is nearly identical to the interface described in the National Semiconductor *PC16550D UART with FIFOs* data sheet (June, 1995), (http://www.national.com/pf/PC/PC16550D.html) with the following major differences:

- Sysclock. All bus transactions and UART operations are synchronized to this input clock.
- Freeze. Asserting this signal disables interrupts and places the UART receiver and transmitter in the marking state.
- Xin is a clock enable input, rather than a true clock.
- Rclk is a clock enable input rather than a true clock.
- Wr/WrN are clock enables.
- Rd/RdN are clock enables.
- AdsN is a clock enable.
- Three state data bus (D) is separated into a read bus (Dout) and a write bus (D). Dout is always driven.

Description of the raw interface signals

Sysclock. This is the primary UART reference clock. All UART operations and bus transactions are synchronized to this signal.

Xin. Xin is the reference for the UART baud rate generator circuit. Xin is a clock enable input. If Xin is tied high, the baud rate reference will be Sysclock. Otherwise, Xin should be a single Sysclock period pulse high, with whatever duty cycle is required by the application.

Rclk. This is the 16x reference for the receiver portion of the UART. It is a clock enable and should be a single Sysclock period pulse high, with whatever duty cycle is required by the application. To simplify a system design Rclk may be tied to the inverse of baudoutN.

Dout(7:0). UART read bus. Valid data will appear on this bus on the second Sysclock following Rd/RdN being brought active. This bus is always driven.

Ddis. This signal goes low on the second Sysclock following Rd/RdN being brought active.

D(7:0). UART write bus.Valid data will be sampled during any clock period in which Wr/WrN are active with a valid address and chip select applied.

AdsN. Address Strobe. This is a clock enable. Address pins (A2:A0) and Chip Select pins (Cs0, Cs1 and Cs2N) will be sampled when AdsN is low and held when AdsN is high.

Wr/WrN. UART write pins. Data on D(7:0) is sampled during any Sysclock period in which Wr or WrN is active.

Rd/RdN. UART read pins. Data from the currently addressed register will appear on Dout(7:0) 2 Sysclock cycles following Rd or RdN being asserted.

A(2:0). UART address bus. This address bus is a three bit address. The register map is identical to that described in the National Semiconductor *PC16550D UART with FIFOs* data sheet (June, 1995):

(http://www.national.com/pf/PC/PC16550D.html).

These pins are sampled when AdsN is low and held when AdsN is high. If AdsN is tied low, A(2:0) must be stable while Rd/RdN/Wr/WrN are active.

Cs0, Cs1, Cs2N. UART chip selects. These pins are sampled when AdsN is low and held when AdsN is high. If AdsN is tied low, these pins must be stable while Rd/RdN/Wr/WrN are active.

All other signals. All other interface signals are as described in the National Semiconductor *PC16550D UART with FIFOs* data sheet (June, 1995). (http://www.national.com/pf/PC/PC16550D.html).

Design Implementation

Target Technology

The intended target technology is Virtex-II FPGA

Device Utilization and Timing

OPB_Clk is capable of running at 100 MHz. XIN and RCLK must be less than 1/2 OPB_Clk frequency.

Performance Benchmarks

Table 16: **Performance and Resource Utilization Benchmarks**

Parameter Values	Device Resources			f_{MAX} (MHz)
	Slices	Slice Flip-Flops	LUTs	f_{MAX}
OPB UART 16450	341	N/A	357	N/A

Specification Exceptions

System Clock

The asynchronous microprocessor interface of the National Semiconductor PC16550D is synchronized to the system clock input of the UART**.**

Register Addresses

All internal registers reside on a 32 bit word boundary not on 8 bit byte boundaries.

Reference Documents

The following documents contain reference information important to understanding the UART design:

- National Semiconductor *PC16550D UART with FIFOs* data sheet (June, 1995).

  (http://www.national.com/pf/PC/PC16550D.html)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/03/01	1.0	Initial Xilinx release.
05/28/02	1.1	Update for EDK 1.0
07/23/02	1.2	Add XCO parameters for System Generator
01/08/03	1.3	Update for EDK SP3
05/15/03	1.4	Change LS and MS register names
07/28/03	1.5	Update to new template
08/01/03	1.5.1	Add generic per CR 175375; remove conditional text table notes per CR 175368
05/21/04	1.5.2	Update narrative in Device Utilization and Timing section per CR 188487
06/01/04	1.5.3	Correct C_HIGHADDR value
8/18/04	1.6	Updated for Gmm; updated trademarks and supported device family listing.