Data Sheet | July 19, 2007 | FN6498.1

Highly Integrated Battery Charger Controller for Notebook Computers

The ISL6252, ISL6252A is a highly integrated battery charger controller for Li-Ion/Li-Ion polymer batteries. High Efficiency is achieved by a synchronous buck topology. The low side MOSFET emulates a diode at light loads to improve the light load efficiency and prevent system bus boosting.

The constant output voltage can be selected for 2, 3 and 4 series Li-Ion cells with 0.5% accuracy over-temperature. It can also be programmed between 4.2V + 5%/cell and 4.2V - 5%/cell to optimize battery capacity. When supplying the load and battery charger simultaneously, the input current limit for the AC adapter is programmable to within 3% accuracy to avoid overloading the AC adapter, and to allow the system to make efficient use of available adapter power for charging. It also has a wide range of programmable charging current. The ISL6252, ISL6252A provides outputs that are used to monitor the current drawn from the AC adapter, and monitor for the presence of an AC adapter. The ISL6252, ISL6252A automatically transitions from regulating current mode to regulating voltage mode.

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6252HRZ*	ISL 6252HRZ	-10 to +100	28 Ld 5x5 QFN	L28.5×5
ISL6252HAZ*	ISL 6252HAZ	-10 to +100	24 Ld QSOP	M24.15
ISL6252AHRZ*	ISL6252 AHRZ	-10 to +100	28 Ld 5x5 QFN	L28.5×5
ISL6252AHAZ*	ISL6252 AHAZ	-10 to +100	24 Ld QSOP	M24.15

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-T” for Tape and Reel. Please refer to TB347 for details on reel specifications.

Features

- ±0.5% Charge Voltage Accuracy (-10°C to +100°C)
- ±3% Accurate Input Current Limit
- ±3% Accurate Battery Charge Current Limit
- ±25% Accurate Battery Trickle Charge Current Limit
- Programmable Charge Current Limit, Adapter Current Limit and Charge Voltage
- Fixed 300kHz PWM Synchronous Buck Controller with Diode Emulation at Light Load
- Overvoltage Protection
- Output for Current Drawn from AC Adapter
- AC Adapter Present Indicator
- Fast Input Current Limit Response
- Input Voltage Range 7V to 25V
- Support 2-, 3- and 4-Cells Battery Pack
- Up to 17.64V Battery-Voltage Set Point
- Thermal Shutdown
- Less than 10µA Battery Leakage Current
- Supports Pulse Charging
- Pb-Free Plus Anneal Available (RoHS Compliant)

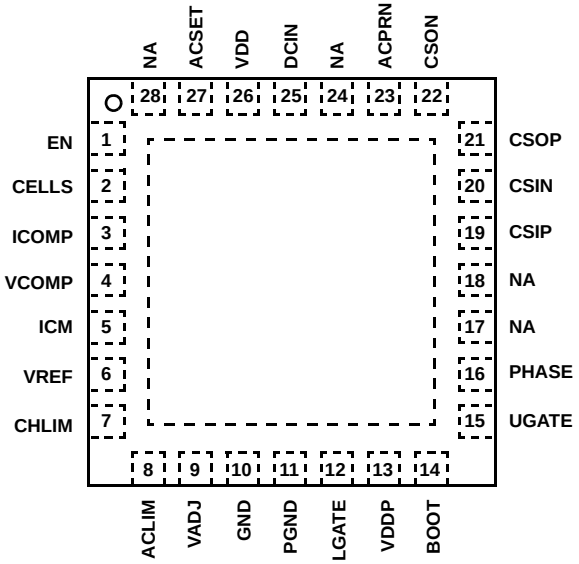
Applications

- Notebook, Desknote and Sub-notebook Computers
- Personal Digital Assistant

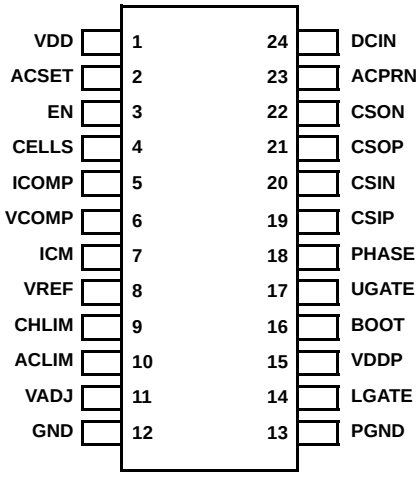
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 2007. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

Pinouts

ISL6252, ISL6252A
(28 LD QFN)
TOP VIEW



ISL6252, ISL6252A
(24 LD QSOP)
TOP VIEW



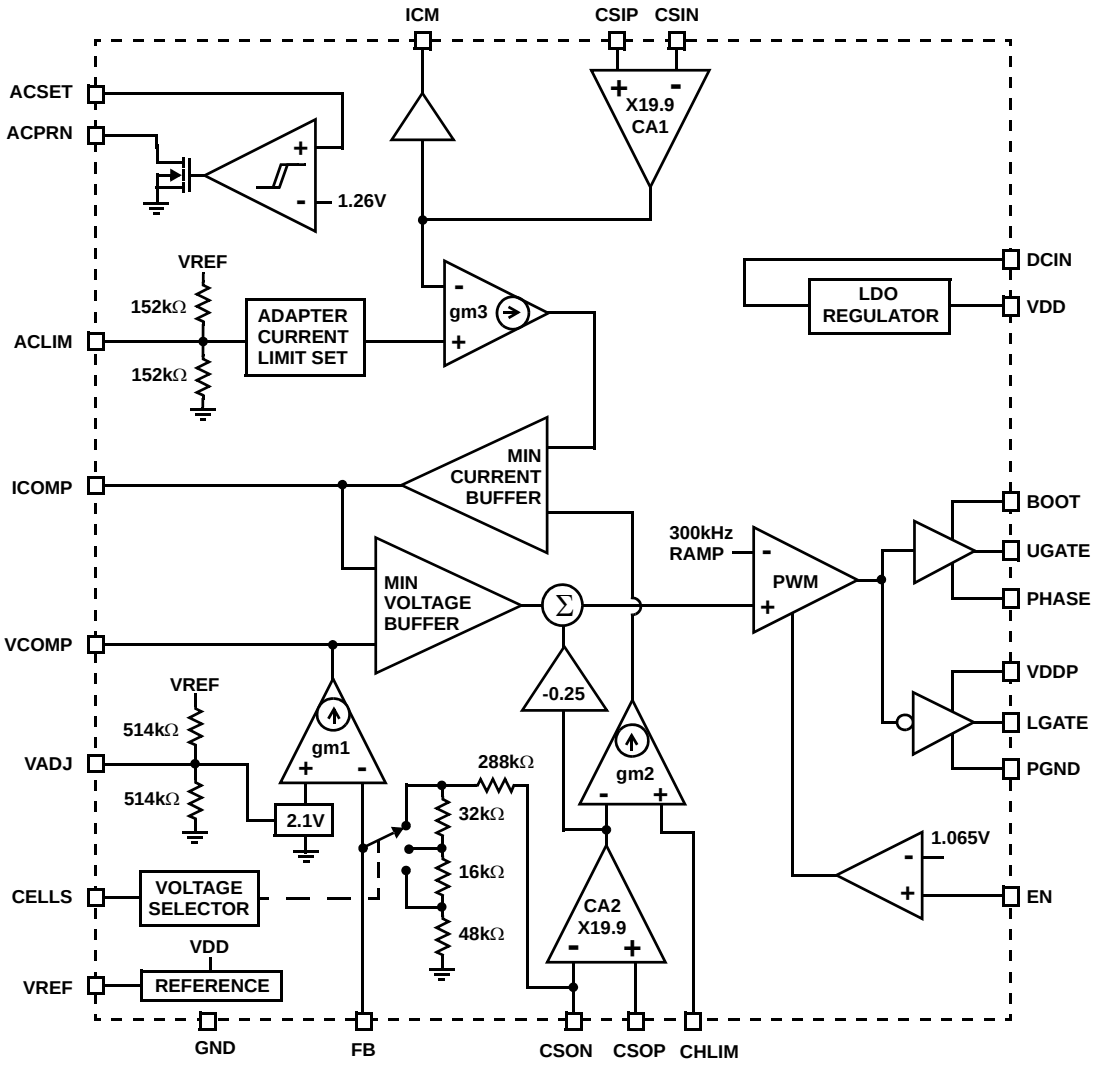


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

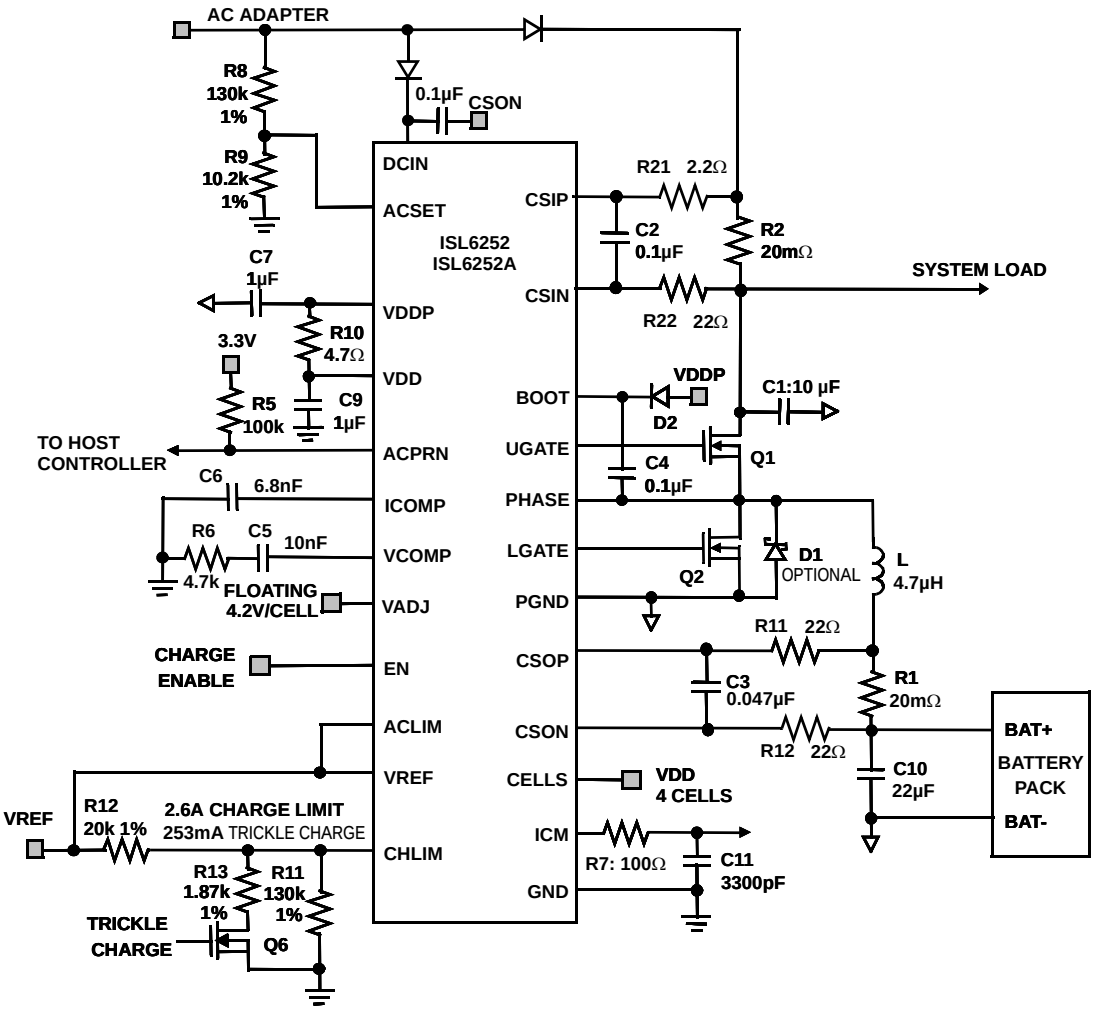


FIGURE 2. ISL6252, ISL6252A TYPICAL APPLICATION CIRCUIT WITH FIXED CHARGING PARAMETERS

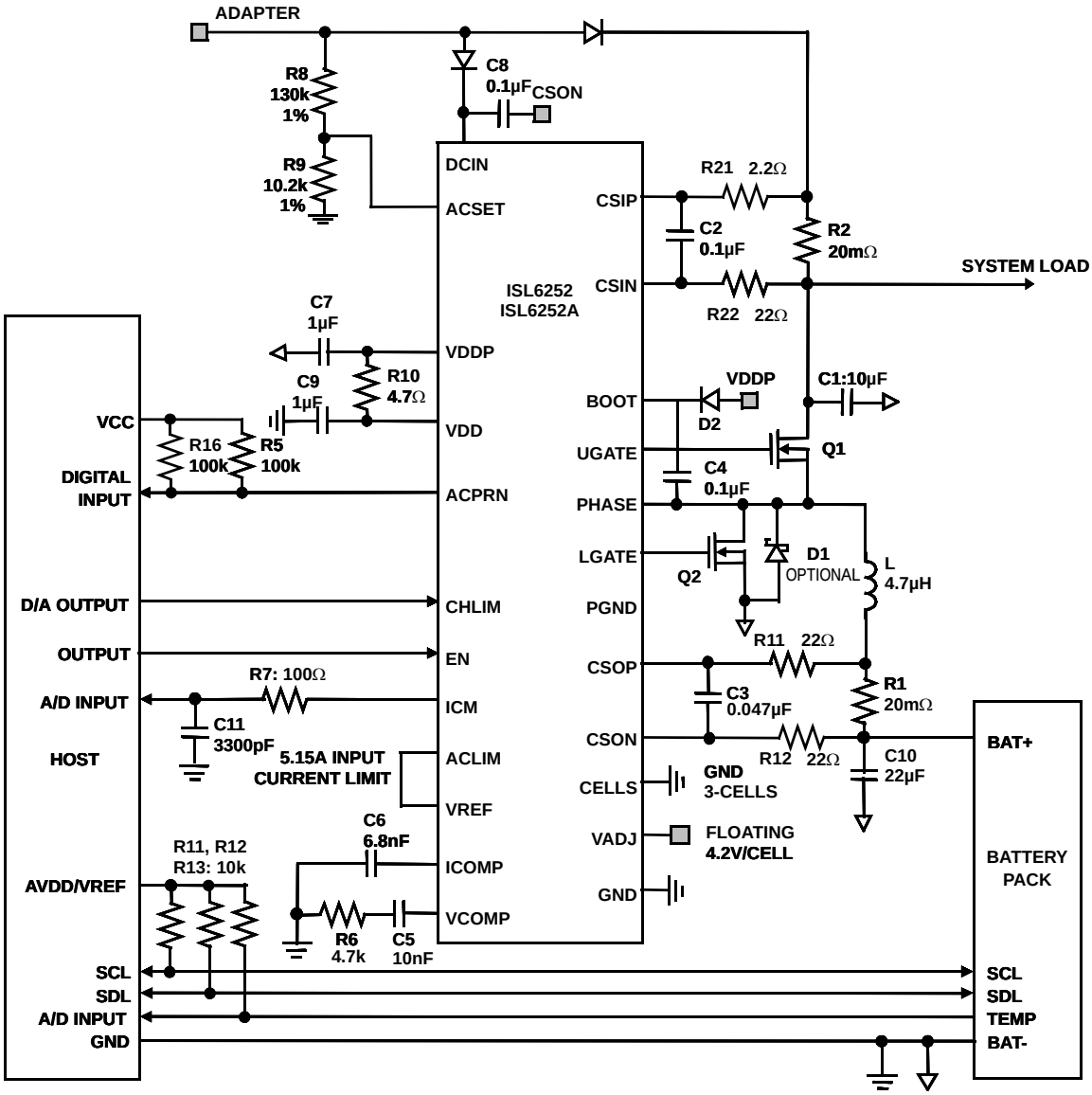


FIGURE 3. ISL6252, ISL6252A TYPICAL APPLICATION CIRCUIT WITH µP CONTROL

Absolute Maximum Ratings

ACSET to GND (Note 3) . . . . . -0.3V to VDD +0.3V
DCIN, CSIP, CSON to GND . . . . . -0.3V to +28V
CSIP-CSIN, CSOP-CSON . . . . . -0.3V to +0.3V
PHASE to GND . . . . . -7V to 30V
BOOT to GND . . . . . -0.3V to +35V
BOOT to VDDP . . . . . -2V to 28V
ACLIM, ACPRN, CHLIM, VDD to GND . . . . . -0.3V to 7V
BOOT-PHASE, VDDP-PGND . . . . . -0.3V to 7V
ICM, ICOMP, VCOMP to GND . . . . . -0.3V to VDD +0.3V
VREF, CELLS to GND . . . . . -0.3V to VDD +0.3V
EN, VADJ, PGND to GND . . . . . -0.3V to VDD +0.3V
UGATE . . . . . PHASE -0.3V to BOOT +0.3V
LGATE . . . . . PGND -0.3V to VDDP +0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	39	9.5
QSOP Package (Note 4)	80	NA

Junction Temperature Range . . . . . -10°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. ACSET may be operated 1V below GND if the current through ACSET is limited to less than 1mA.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125$°C, Unless Otherwise Noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND BIAS REGULATOR					
DCIN Input Voltage Range		7		25	V
DCIN Quiescent Current	EN = VDD or GND, 7V ≤ DCIN ≤ 25V		1.4	3	mA
Battery Leakage Current (Note 6)	DCIN = 0, no load		3	10	µA
VDD Output Voltage/Regulation	7V ≤ DCIN ≤ 25V, 0 ≤ I_{VDD} ≤ 30mA	4.925	5.075	5.225	V
VDD Undervoltage Lockout Trip Point	VDD Rising	4.0	4.4	4.6	V
	Hysteresis	200	250	400	mV
Reference Output Voltage VREF	0 ≤ I_{VREF} ≤ 300µA	2.365	2.39	2.415	V
Battery Charge Voltage Accuracy	CSON = 16.8V, CELLS = VDD, VADJ = Float	-0.5		0.5	%
	CSON = 12.6V, CELLS = GND, VADJ = Float	-0.5		0.5	%
	CSON = 8.4V, CELLS = Float, VADJ = Float	-0.5		0.5	%
	CSON = 17.64V, CELLS = VDD, VADJ = VREF	-0.5		0.5	%
	CSON = 13.23V, CELLS = GND, VADJ = VREF	-0.5		0.5	%
	CSON = 8.82V, CELLS = Float, VADJ = VREF	-0.5		0.5	%
	CSON = 15.96V, CELLS = VDD, VADJ = GND	-0.5		0.5	%
	CSON = 11.97V, CELLS = GND, VADJ = GND	-0.5		0.5	%
	CSON = 7.98V, CELLS = Float, VADJ = GND	-0.5		0.5	%
TRIP POINTS					
ACSET Threshold		1.24	1.26	1.28	V
ACSET Input Bias Current Hysteresis		2.4	3.4	4.4	µA
ACSET Input Bias Current	ACSET ≥ 1.26V	2.4	3.4	4.4	µA
ACSET Input Bias Current	ACSET < 1.26V	-1	0	1	µA

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125$°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Frequency		245	300	355	kHz
PWM Ramp Voltage (peak-peak)	CSIP = 18V		1.6		V
	CSIP = 11V		1		V
SYNCHRONOUS BUCK REGULATOR					
Maximum Duty Cycle		97	99	99.6	%
UGATE Pull-Up Resistance	BOOT-PHASE = 5V, 500mA source current		1.8	3.0	Ω
UGATE Source Current	BOOT-PHASE = 5V, BOOT-UGATE = 2.5V		1.0		A
UGATE Pull-down Resistance	BOOT-PHASE = 5V, 500mA sink current		1.0	1.8	Ω
UGATE Sink Current	BOOT-PHASE = 5V, UGATE-PHASE = 2.5V		1.8		A
LGATE Pull-Up Resistance	VDDP-PGND = 5V, 500mA source current		1.8	3.0	Ω
LGATE Source Current	VDDP-PGND = 5V, VDDP-LGATE = 2.5V		1.0		A
LGATE Pull-Down Resistance	VDDP-PGND = 5V, 500mA sink current		1.0	1.8	Ω
LGATE Sink Current	VDDP-PGND = 5V, LGATE = 2.5V		1.8		A
Dead Time	Falling UGATE to rising LGATE or falling LGATE to rising UGATE	10		30	ns
CHARGING CURRENT SENSING AMPLIFIER					
Input Common-Mode Range		0		18	V
Input Bias Current at CSOP	5 < CSOP < 18V		0.25	2	µA
Input Bias Current at CSON	5 < CSON < 18V		75	100	µA
CHLIM Input Voltage Range		0		3.6	V
ISL6252 CSOP to CSON Full-Scale Current Sense Voltage	ISL6252: CHLIM = 3.3V	160	165	170	mV
	ISL6252: CHLIM = 2.0V	95	100	105	mV
	ISL6252: CHLIM = 0.2V	5.0	10	15.0	mV
ISL6252A CSOP to CSON Full-Scale Current Sense Voltage	ISL6252A: CHLIM = 3.3V	161.7	165	168.3	mV
	ISL6252A: CHLIM = 2.0V	97	100	103	mV
	ISL6252A: CHLIM = 0.2V	7.5	10	12.5	mV
ISL6252 CSOP to CSON Full-Scale Current Sense Voltage formula	Charge current limit mode 0.2V < CHLIM < 3.3V	CHLIM*50 -5		CHLIM*50 +5	mV
ISL6252A CSOP to CSON Full-Scale Current Sense Voltage formula	Charge current limit mode 0.2V < CHLIM < 3.3V	CHLIM*49.72 -2.4		CHLIM*50.28 +2.4	mV
CHLIM Input Bias Current	CHLIM = GND or 3.3V, DCIN = 0V	-1		1	µA
CHLIM Power-Down Mode Threshold Voltage	CHLIM rising	80	88	95	mV
CHLIM Power-Down Mode Hysteresis Voltage		15	25	40	mV
ADAPTER CURRENT SENSING AMPLIFIER					
Input Common-Mode Range		7		25	V
Input Bias Current at CSIP and CSIN Combined	CSIP = CSIN = 25V		100	130	µA
Input Bias Current at CSIN	0 < CSIN < DCIN		0.10		µA

Electrical Specifications DCIN = CSIP = CSIN = 18V, CSOP = CSON = 12V, ACSET = 1.5V, ACLIM = VREF, VADJ = Floating, EN = VDD = 5V, BOOT-PHASE = 5.0V, GND = PGND = 0V, C_{VDD} = 1µF, I_{VDD} = 0mA, T_A = -10°C to +100°C, $T_J \leq +125$°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ADAPTER CURRENT LIMIT THRESHOLD					
CSIP to CSIN Full-Scale Current Sense Voltage	ACLIM = VREF	97	100	103	mV
	ACLIM = Float	72	75	78	mV
	ACLIM = GND	47	50	53	mV
ACLIM Input Bias Current	ACLIM = VREF	10	16	20	µA
	ACLIM = GND	-20	-16	-10	µA
VOLTAGE REGULATION ERROR AMPLIFIER					
Error Amplifier Transconductance from CSON to VCOMP	CELLS = VDD		30		µA/V
CURRENT REGULATION ERROR AMPLIFIER					
Charging Current Error Amplifier Transconductance			50		µA/V
Adapter Current Error Amplifier Transconductance			50		µA/V
BATTERY CELL SELECTOR					
CELLS Input Voltage for 4 Cell Select		4.3			V
CELLS Input Voltage for 3 Cell Select				2	V
CELLS Input Voltage for 2 Cell Select		2.1		4.2	V
LOGIC INTERFACE					
EN Input Voltage Range		0		VDD	V
EN Threshold Voltage	Rising	1.030	1.06	1.100	V
	Falling	0.985	1.000	1.025	V
	Hysteresis	30	60	90	mV
EN Input Bias Current	EN = 2.5V	1.8	2.0	2.2	µA
ACPRN Sink Current	ACPRN = 0.4V	3	8	11	mA
ACPRN Leakage Current	ACPRN = 5V	-0.5		0.5	µA
ICM Output Accuracy (V_{ICM} = 19.9 x (V_{CSIP} - V_{CSIN}))	CSIP-CSIN = 100mV	-3	0	+3	%
	CSIP-CSIN = 75mV	-4	0	+4	%
	CSIP-CSIN = 50mV	-5	0	+5	%
Thermal Shutdown Temperature			150		°C
Thermal Shutdown Temperature Hysteresis			25		°C

NOTE:

6. This is the sum of currents in these pins (CSIP, CSIN, BOOT, UGATE, PHASE, CSOP, CSON) all tied to 16.8V. No current in pins EN, ACSET, VADJ, CELLS, ACLIM, CHLIM.

Typical Operating Performance

DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, Unless Otherwise Noted.

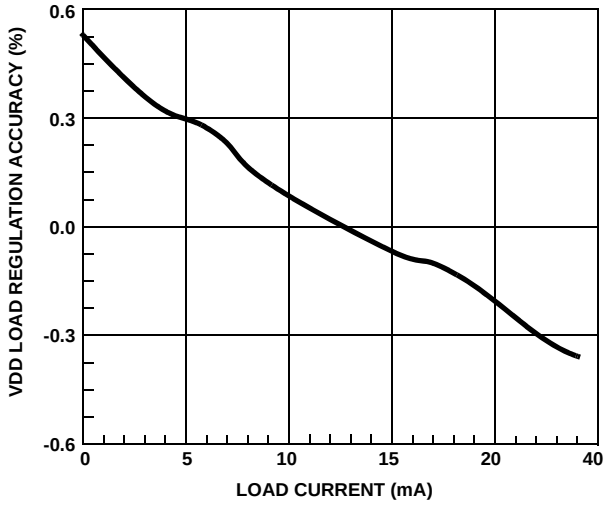


FIGURE 4. VDD LOAD REGULATION

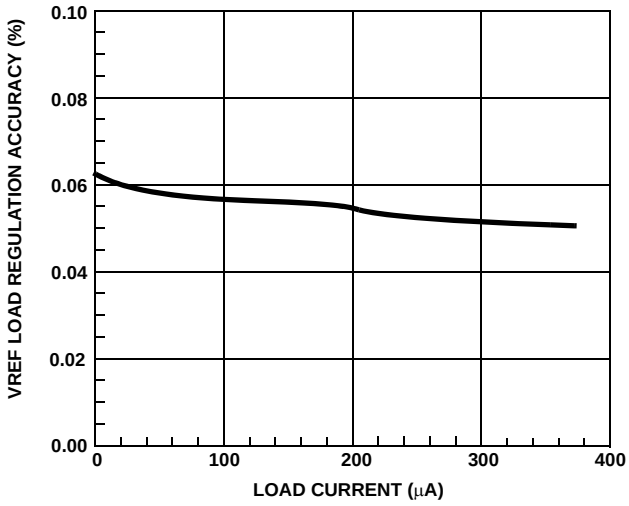


FIGURE 5. VREF LOAD REGULATION

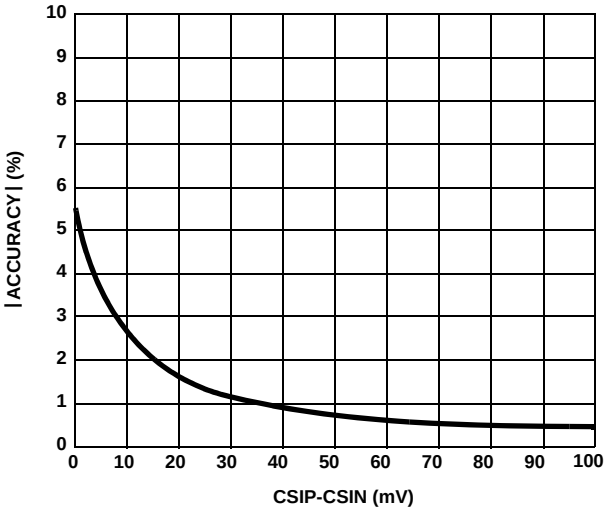


FIGURE 6. ACCURACY vs AC ADAPTER CURRENT

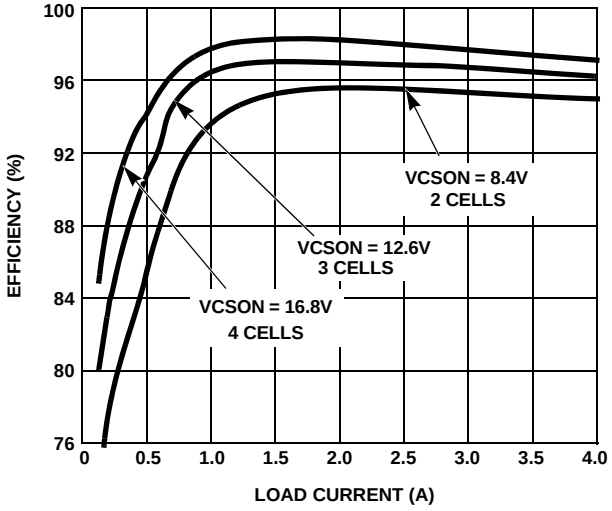


FIGURE 7. SYSTEM EFFICIENCY vs CHARGE CURRENT

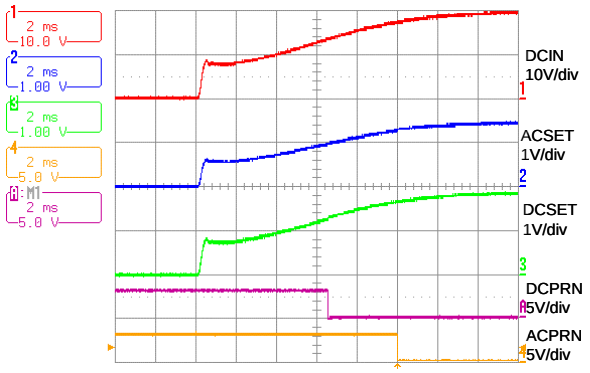


FIGURE 8. AC AND DC ADAPTER DETECTION

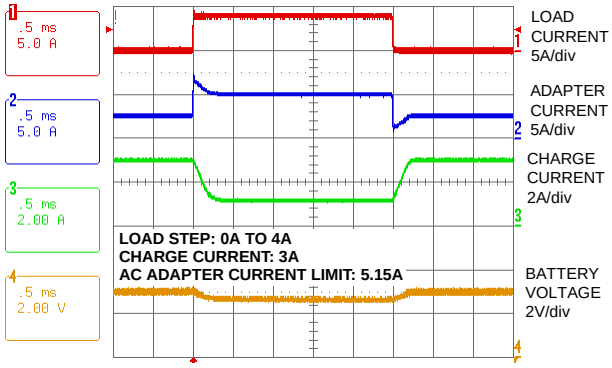


FIGURE 9. LOAD TRANSIENT RESPONSE

Typical Operating Performance

DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, Unless Otherwise Noted. **(Continued)**

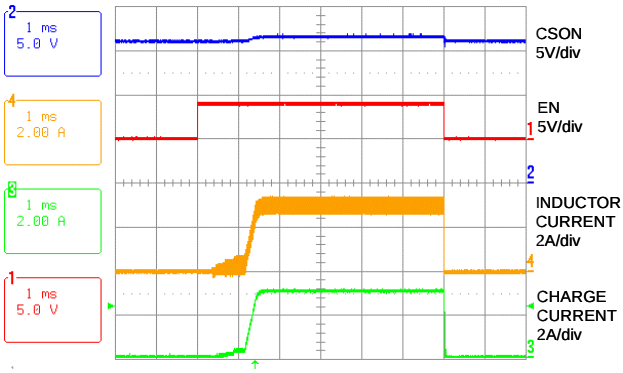


FIGURE 10. CHARGE ENABLE AND SHUTDOWN

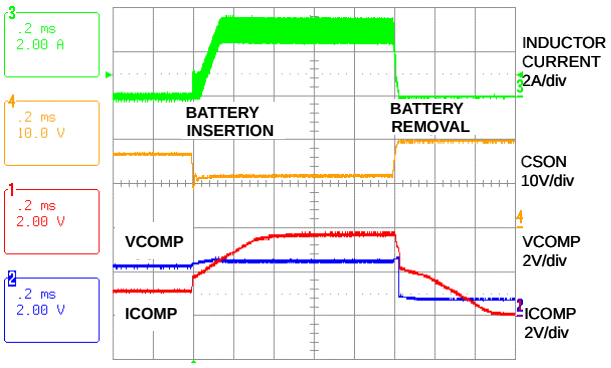


FIGURE 11. BATTERY INSERTION AND REMOVAL

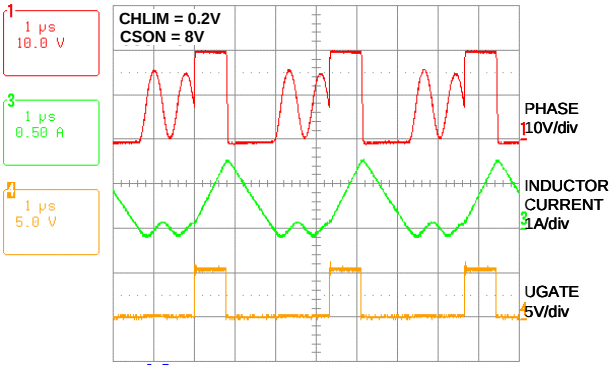


FIGURE 12. AC ADAPTER REMOVAL

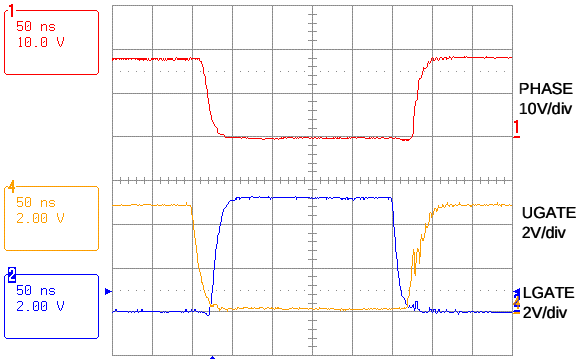


FIGURE 13. AC ADAPTER INSERTION

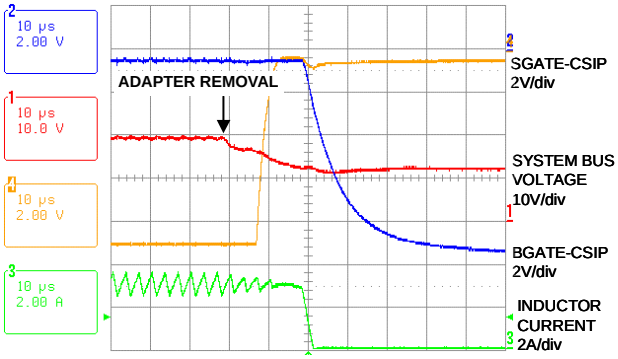


FIGURE 14. SWITCHING WAVEFORMS AT DIODE EMULATION

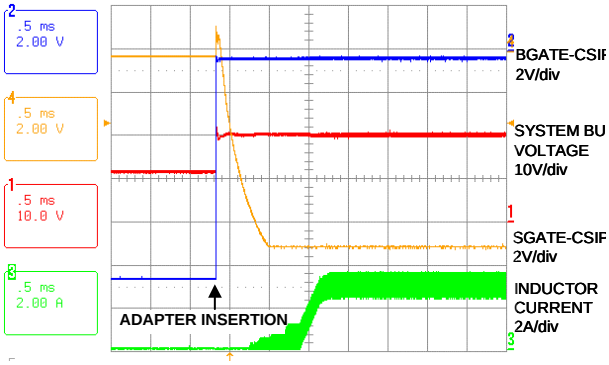


FIGURE 15. SWITCHING WAVEFORMS IN CC MODE

Typical Operating Performance

DCIN = 20V, 4S2P Li-Battery, T_A = +25°C, Unless Otherwise Noted. **(Continued)**

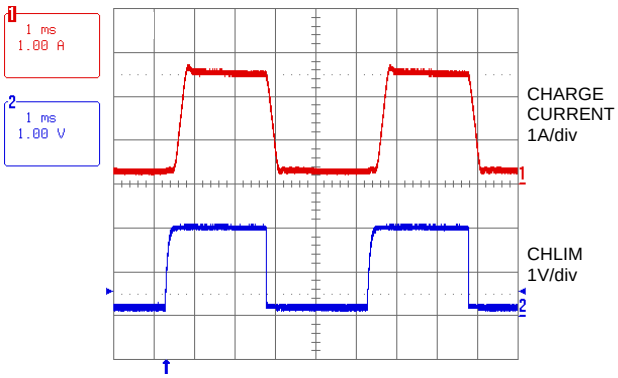


FIGURE 16. TRICKLE TO FULL-SCALE CHARGING

Functional Pin Descriptions

BOOT

Connect BOOT to a 0.1µF ceramic capacitor to PHASE pin and connect to the cathode of the bootstrap Schottky diode.

UGATE

UGATE is the high side MOSFET gate drive output.

LGATE

LGATE is the low side MOSFET gate drive output; swing between 0V and VDDP.

PHASE

The Phase connection pin connects to the high side MOSFET source, output inductor, and low side MOSFET drain.

CSOP/CSON

CSOP/CSON is the battery charging current sensing positive/negative input. The differential voltage across CSOP and CSON is used to sense the battery charging current, and is compared with the charging current limit threshold to regulate the charging current. The CSON pin is also used as the battery feedback voltage to perform voltage regulation.

CSIP/CSIN

CSIP/CSIN is the AC adapter current sensing positive/negative input. The differential voltage across CSIP and CSIN is used to sense the AC adapter current, and is compared with the AC adapter current limit to regulate the AC adapter current.

GND

GND is an analog ground.

DCIN

The DCIN pin is the input of the internal 5V LDO. Connect it to the AC adapter output. Connect a 0.1µF ceramic capacitor from DCIN to CSON.

ACSET

ACSET is an AC adapter detection input. Connect to a resistor divider from the AC adapter output.

ACPRN

Open-drain output signals AC adapter is present. ACPRN pulls low when ACSET is higher than 1.26V; and pulled high when ACSET is lower than 1.26V.

EN

EN is the Charge Enable input. Connecting EN to high enables the charge control function, connecting EN to low disables charging functions. Use with a thermistor to detect a hot battery and suspend charging.

ICM

ICM is the adapter current output. The output of this pin produces a voltage proportional to the adapter current.

PGND

PGND is the power ground. Connect PGND to the source of the low side MOSFET.

VDD

VDD is an internal LDO output to supply IC analog circuit. Connect a 1µF ceramic capacitor to ground.

VDDP

VDDP is the supply voltage for the low-side MOSFET gate driver. Connect a 4.7Ω resistor to VDD and a 1µF ceramic capacitor to power ground.

ICOMP

ICOMP is a current loop error amplifier output.

VCOMP

VCOMP is a voltage loop amplifier output.

CELLS

This pin is used to select the battery voltage. CELLS = VDD for a 4S battery pack, CELLS = GND for a 3S battery pack, CELLS = Float for a 2S battery pack.

VADJ

VADJ adjusts battery regulation voltage. VADJ = VREF for 4.2V+5%/cell; VADJ = Floating for 4.2V/cell; VADJ = GND for 4.2V-5%/cell. Connect to a resistor divider to program the desired battery cell voltage between 4.2V-5% and 4.2V+5%.

CHLIM

CHLIM is the battery charge current limit set pin. CHLIM input voltage range is 0.1V to 3.6V. When CHLIM = 3.3V, the set point for CSOP to CSON is 165mV. The charger shuts down if CHLIM is forced below 88mV.

ACLIM

ACLIM is the adapter current limit set pin. ACLIM = VREF for 100mV, ACLIM = Floating for 75mV, and ACLIM = GND for 50mV. Connect a resistor divider to program the adapter current limit threshold between 50mV and 100mV.

VREF

VREF is a 2.39V reference output pin. It is internally compensated. Do not connect a decoupling capacitor.

Theory of Operation

Introduction

Unless otherwise noted, all descriptions of ISL6252 refer to both ISL6252 and ISL6252A. The ISL6252 includes all of the functions necessary to charge 2 to 4 cell Li-Ion and Li-polymer batteries. A high efficiency synchronous buck converter is used to control the charging voltage and charging current up to 10A. The ISL6252 has input current limiting and analog inputs for setting the charge current and charge voltage; CHLIM inputs are used to control charge current and VADJ inputs are used to control charge voltage.

The ISL6252 charges the battery with constant charge current, set by CHLIM input, until the battery voltage rises up to a programmed charge voltage set by VADJ input; then the charger begins to operate at a constant voltage charge mode. The charger also drives an adapter isolation P-Channel MOSFET to efficiently switch in the adapter supply.

ISL6252 is a complete power source selection controller for single battery systems and also aircraft power applications. It drives a battery selector P-Channel MOSFET to efficiently select between a single battery and the adapter. It controls the battery discharging MOSFET and switches to the battery when the AC adapter is removed, or, switches to the AC adapter when the AC adapter is inserted for single battery system.

The EN input allows shutdown of the charger through a command from a micro-controller. It also uses EN to safely shutdown the charger when the battery is in extremely hot conditions. The amount of adapter current is reported on the ICM output. Figure 1 shows the IC functional block diagram.

The synchronous buck converter uses external N-Channel MOSFETs to convert the input voltage to the required charging current and charging voltage. Figure 2 shows the ISL6252 typical application circuit with charging current and charging voltage fixed at specific values. The typical application circuit shown in Figure 3 shows the ISL6252 typical application circuit which uses a micro-controller to adjust the charging current set by CHLIM input for aircraft power applications. The voltage at CHLIM and the value of R_1 sets the charging current. The DC/DC converter generates the control signals to drive two external N-Channel MOSFETs to regulate the voltage and current set by the ACLIM, CHLIM, VADJ and CELLS inputs.

The ISL6252 features a voltage regulation loop (VCOMP) and two current regulation loops (ICOMP). The VCOMP voltage regulation loop monitors CSON to ensure that its voltage never exceeds the voltage and regulates the battery charge voltage set by VADJ. The ICOMP current regulation loops regulate the battery charging current delivered to the battery to ensure that it never exceeds the charging current limit set by CHLIM; and the ICOMP current regulation loops also regulate the input current drawn from the AC adapter to ensure that it never exceeds the input current limit set by ACLIM, and to prevent a system crash and AC adapter overload.

PWM Control

The ISL6252 employs a fixed frequency PWM current mode control architecture with a feed-forward function. The feed-forward function maintains a constant modulator gain of 11 to achieve fast line regulation as the buck input voltage changes. When the battery charge voltage approaches the input voltage, the DC/DC converter operates in dropout mode, where there is a timer to prevent the frequency from dropping into the audible frequency range. It can achieve duty cycle of up to 99.6%.

To prevent boosting of the system bus voltage, the battery charger operates in standard-buck mode when CSOP-CSON drops below 4.25mV. Once in standard-buck mode, hysteresis does not allow synchronous operation of the DC/DC converter until CSOP-CSON rises above 12.5mV.

An adaptive gate drive scheme is used to control the dead time between two switches. The dead time control circuit monitors the LGATE output and prevents the upper side MOSFET from turning on until LGATE is fully off, preventing cross-conduction and shoot-through. In order for the dead time circuit to work properly, there must be a low resistance, low inductance path from the LGATE driver to MOSFET gate, and from the source of MOSFET to PGND. The external Schottky diode is between the VDDP pin and BOOT pin to keep the bootstrap capacitor charged.

Setting the Battery Regulation Voltage

The ISL6252 uses a high-accuracy trimmed band-gap voltage reference to regulate the battery charging voltage. The VADJ input adjusts the charger output voltage, and the VADJ control voltage can vary from 0 to VREF, providing a

10% adjustment range (from 4.2V-5% to 4.2V+5%) on CSON regulation voltage. An overall voltage accuracy of better than 0.5% is achieved.

The per-cell battery termination voltage is a function of the battery chemistry. Consult the battery manufacturers to determine this voltage.

- Float VADJ to set the battery voltage V_{CSON} = 4.2V × number of the cells,
- Connect VADJ to VREF to set 4.41V × number of cells,
- Connect VADJ to ground to set 3.99V × number of cells.

So, the maximum battery voltage of 17.6V can be achieved. Note that other battery charge voltages can be set by connecting a resistor divider from VREF to ground. The resistor divider should be sized to draw no more than 100µA from VREF; or connect a low impedance voltage source like the D/A converter in the micro-controller. The programmed battery voltage per cell can be determined by Equation 1:

$$V_{CELL} = 0.175 \cdot V_{VADJ} + 3.99V \quad \text{(EQ. 1)}$$

An external resistor divider from VREF sets the voltage at VADJ according to Equation 2:

$$V_{VADJ} = VREF \times \frac{R_{bot\_VADJ} \parallel 514k\Omega}{R_{top\_VADJ} \parallel 514k\Omega + R_{bot\_VADJ} \parallel 514k\Omega} \quad \text{(EQ. 2)}$$

To minimize accuracy loss due to interaction with VADJ's internal resistor divider, ensure the AC resistance looking back into the external resistor divider is less than 25k.

Connect CELLS as shown in Table 1 to charge 2, 3 or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger. The internal error amplifier gm1 maintains voltage regulation. The voltage error amplifier is compensated at VCOMP. The component values shown in Figure 3 provide suitable performance for most applications. Individual compensation of the voltage regulation and current-regulation loops allows for optimal compensation.

TABLE 1. CELL NUMBER PROGRAMMING

CELLS	CELL NUMBER
VDD	4
GND	3
Float	2

Setting the Battery Charge Current Limit

The CHLIM input sets the maximum charging current. The current set by the current sense-resistor connects between CSOP and CSON. The full-scale differential voltage between CSOP and CSON is 165mV for CHLIM = 3.3V, so the maximum charging current is 4.125A for a 40mΩ sensing resistor. Other battery charge current-sense threshold values can be set by connecting a resistor divider from VREF or 3.3V to ground, or by connecting a low impedance voltage source like a D/A converter in the micro-controller. Unlike VADJ and ACLIM, CHLIM does not have an internal resistor divider network. The charge current limit threshold is given by Equation 3:

$$I_{CHG} = \left(\frac{165mV}{R_1}\right)\left(\frac{V_{CHLIM}}{3.3V}\right) \quad \text{(EQ. 3)}$$

To set the trickle charge current for the dumb charger, an A/D output controlled by the micro-controller is connected to CHLIM pin. The trickle charge current is determined by Equation 4:

$$I_{CHG} = \left(\frac{165mV}{R_1}\right)\left(\frac{V_{CHLIM,trickle}}{3.3V}\right) \quad \text{(EQ. 4)}$$

When the CHLIM voltage is below 88mV (typical), it will disable the battery charge. When choosing the current sensing resistor, note that the voltage drop across the sensing resistor causes further power dissipation, reducing efficiency. However, adjusting CHLIM voltage to reduce the voltage across the current sense resistor R_1 will degrade accuracy due to the smaller signal to the input of the current sense amplifier. There is a trade-off between accuracy and power dissipation. A low pass filter is recommended to eliminate switching noise. Connect the resistor to the CSOP pin instead of the CSON pin, as the CSOP pin has lower bias current and less influence on current-sense accuracy and voltage regulation accuracy.

Charge Current Limit Accuracy

The “Electrical Specifications” table on page 6 gives minimum and maximum values for the CSOP-CSON voltage resulting from IC variations at 3 different CHLIM voltages (CSOP-CSON Full-Scale Current Sense Voltage on page 7). It also gives formulae for calculating the minimum and maximum CSOP-CSON voltage at any CHLIM voltage. Equation 5 shows the formula for the max full scale CSOP-CSON voltage (in mV) for the ISL6252A:

$$(CSOP-CSON)_{MAX}^{ISL6252A} = CHLIM \bullet 50.28 + 2.4$$
$$(CSOP-CSON)_{MIN} = CHLIM \bullet 49.72 - 2.4 \quad \text{(EQ. 5)}$$

Equation 5 shows the formula for the max full scale CSOP-CSON voltage (in mV) for the ISL6252:

$$MAX(CSOP-CSON)^{ISL6252} = CHLIM \bullet 50 + 5$$
$$MIN(CSOP-CSON) = CHLIM \bullet 50 - 5 \quad \text{(EQ. 6)}$$

With CHLIM = 1.5V, the maximum CSOP-CSON voltage is 78mV and the minimum CSOP-CSON voltage is 72mV.

When ISL6252A is in charge current limiting mode, the maximum charge current is the maximum CSOP-CSON

voltage divided by the minimum sense resistor. This can be calculated for ISL6252A with Equation 7:

$$\text{ISL6252A}$$
$$I_{CHG,MAX} = (CHLIM \bullet 50.28 + 2.4)/R_{1MIN}$$
$$I_{CHG,MIN} = (CHLIM \bullet 49.72 - 2.4)/R_{1MAX} \quad \text{(EQ. 7)}$$

Maximum charge current can be calculated for ISL6252 with Equation 8:

$$\text{ISL6252}$$
$$I_{CHG,MAX} = (CHLIM \bullet 50 + 5)/R_{1MIN}$$
$$I_{CHG,MIN} = (CHLIM \bullet 50 - 5)/R_{1MAX} \quad \text{(EQ. 8)}$$

With CHLIM = 0.7V and R_1 = 0.02Ω, 1%:

$$\text{ISL6252A}$$
$$I_{CHG,MAX} = (1.5V \bullet 50.28 + 2.4)/0.0198 = 3930mA$$
$$I_{CHG,MIN} = (1.5V \bullet 49.72 - 2.4)/0.0202 = 3573mA \quad \text{(EQ. 9)}$$

Setting the Input Current Limit

The total input current from an AC adapter, or other DC source, is a function of the system supply current and the battery-charging current. The input current regulator limits the input current by reducing the charging current, when the input current exceeds the input current limit set point. System current normally fluctuates as portions of the system are powered up or down. Without input current regulation, the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using the input current limiter, the current capability of the AC adapter can be lowered, reducing system cost.

The ISL6252 limits the battery charge current when the input current-limit threshold is exceeded, ensuring the battery charger does not load down the AC adapter voltage. This constant input current regulation allows the adapter to fully power the system and prevent the AC adapter from overloading and crashing the system bus.

An internal amplifier gm3 compares the voltage between CSIP and CSIN to the input current limit threshold voltage set by ACLIM. Connect ACLIM to REF, Float and GND for the full-scale input current limit threshold voltage of 100mV, 75mV and 50mV, respectively, or use a resistor divider from VREF to ground to set the input current limit as Equation 10:

$$I_{INPUT} = \frac{1}{R_2} \cdot \left(\frac{0.05}{VREF} \cdot V_{ACLIM} + 0.05\right) \quad \text{(EQ. 10)}$$

An external resistor divider from VREF sets the voltage at ACLIM according to Equation 11:

$$V_{ACLIM} = VREF \cdot \left(\frac{R_{bot,ACLIM} \parallel 152k\Omega}{R_{top,ACLIM} \parallel 152k\Omega + R_{bot,ACLIM} \parallel 152k\Omega}\right) \quad \text{(EQ. 11)}$$

where R_{bot_ACLIM} and R_{top_ACLIM} are external resistors at ACLIM.

To minimize accuracy loss due to interaction with ACLIM's internal resistor divider, ensure the AC resistance looking back into the resistor divider is less than 25k.

When choosing the current sense resistor, note that the voltage drop across this resistor causes further power dissipation, reducing efficiency. The AC adapter current sense accuracy is very important. Use a 1% tolerance current-sense resistor. The highest accuracy of ±3% is achieved with 100mV current-sense threshold voltage for ACLIM = VREF, but it has the highest power dissipation. For example, it has 400mW power dissipation for rated 4A AC adapter and 1Ω sensing resistor may have to be used. ±4% and ±6% accuracy can be achieved with 75mV and 50mV current-sense threshold voltage for ACLIM = Floating and ACLIM = GND, respectively.

A low pass filter is suggested to eliminate the switching noise. Connect the resistor to CSIN pin instead of CSIP pin because CSIN pin has lower bias current and less influence on the current-sense accuracy.

AC Adapter Detection

Connect the AC adapter voltage through a resistor divider to ACSET to detect when AC power is available, as shown in Figure 2. ACPRN is an open-drain output and is high when ACSET is less than $V_{th,rise}$, and active low when ACSET is above $V_{th,fall}$. $V_{th,rise}$ and $V_{th,fall}$ are given by Equation 12 and Equation 13:

$$V_{th,rise} = \left(\frac{R_8}{R_9} + 1\right) \cdot V_{ACSET} \quad \text{(EQ. 12)}$$

$$V_{th,fall} = \left(\frac{R_8}{R_9} + 1\right) \cdot V_{ACSET} - I_{hys} \cdot R_8 \quad \text{(EQ. 13)}$$

where:

- I_{hys} is the ACSET input bias current hysteresis, and
- V_{ACSET} = 1.24V (min), 1.26V (typ) and 1.28V (max).

The hysteresis is $I_{hys}R_8$, where I_{hys} = 2.2µA (min), 3.4µA (typ) and 4.4µA (max).

Current Measurement

Use ICM to monitor the input current being sensed across CSIP and CSIN. The output voltage range is 0V to 2.5V. The voltage of ICM is proportional to the voltage drop across CSIP and CSIN, and is given by Equation 14:

$$ICM = 19.9 \bullet I_{INPUT} \bullet R_2 \quad \text{(EQ. 14)}$$

where I_{INPUT} is the DC current drawn from the AC adapter. ICM has ±3% accuracy. It is recommended to have an RC filter at the ICM output for minimizing the switching noise.

LDO Regulator

VDD provides a 5.0V supply voltage from the internal LDO regulator from DCIN and can deliver up to 30mA of current. The MOSFET drivers are powered by VDDP, which must be connected to VDDP as shown in Figure 2. VDDP connects to VDD through an external low pass filter. Bypass VDDP and VDD with a 1µF capacitor.

Shutdown

The ISL6252 features a low-power shutdown mode. Driving EN low shuts down the ISL6252. In shutdown, the DC/DC converter is disabled, and VCOMP and ICOMP are pulled to ground. The ICM, ACPRN output continue to function.

EN can be driven by a thermistor to allow automatic shutdown of the ISL6252 when the battery pack is hot. Often a NTC thermistor is included inside the battery pack to measure its temperature. When connected to the charger, the thermistor forms a voltage divider with a resistive pull-up to the VREF. The threshold voltage of EN is 1.0V with 60mV hysteresis. The thermistor can be selected to have a resistance vs temperature characteristic that abruptly decreases above a critical temperature. This arrangement automatically shuts down the ISL6252 when the battery pack is above a critical temperature.

Another method for inhibiting charging is to force CHLIM below 85mV (typ).

Short Circuit Protection and 0V Battery Charging

Since the battery charger will regulate the charge current to the limit set by CHLIM, it automatically has short circuit protection and is able to provide the charge current to wake up an extremely discharged battery.

Over-Temperature Protection

If the die temp exceeds +150°C, it stops charging. Once the die temp drops below +125°C, charging will start up again.

Overvoltage Protection

ISL6252 has an Overvoltage Protection circuit that limits the output voltage when the battery is removed or disconnected by a pulse charging circuit. If CSON exceeds the output voltage set point by more than V_{OVP} an internal comparator pulls VCOMP down and turns off both upper and lower FETs of the buck as in Figure 17. The trip point for Overvoltage Protection is always above the nominal output voltage and can be calculated from Equation 15:

$$V_{OVP} = V_{OUT,NOM} + N_{CELLS} \times \left(42.2mV - 22.2mV \times \frac{V_{ADJ}}{2.39V}\right) \quad \text{(EQ. 15)}$$

For example, if the CELLS pin is connected to ground (N_{CELLS} = 3) and V_{ADJ} is floating (V_{ADJ} = 1.195V) then $V_{OUT,NOM}$ = 12.6V and V_{OVP}=12.693V or $V_{OUT,NOM}$ + 93mV.

There is a delay of approximately 400nsec between V_{OUT} exceeding the OVP trip point and pulling VCOMP, LGATE and UGATE low.

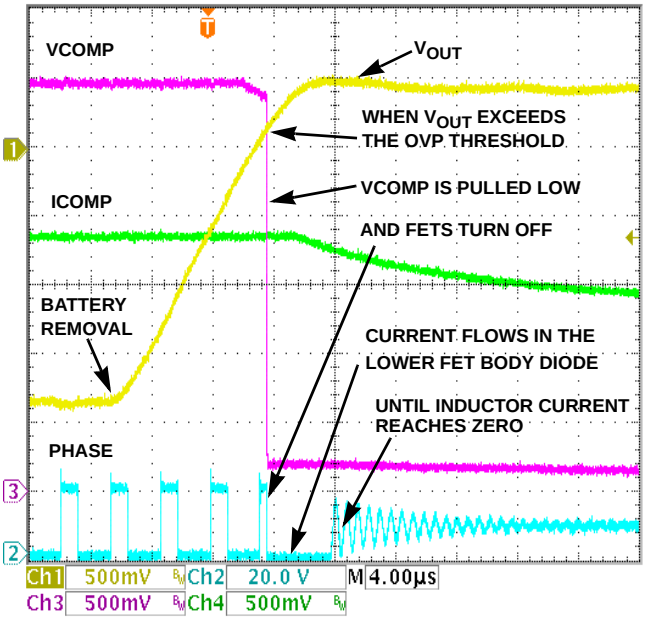


FIGURE 17. OVERVOLTAGE PROTECTION IN ISL6252

Application Information

The following battery charger design refers to the typical application circuit in Figure 2, where typical battery configuration of 4S2P is used. This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFETs, and current sensing resistors.

Inductor Selection

The inductor selection has trade-offs between cost, size, cross over frequency and efficiency. For example, the lower the inductance, the smaller the size, but ripple current is higher. This also results in higher AC losses in the magnetic core and the windings, which decrease the system efficiency. On the other hand, the higher inductance results in lower ripple current and smaller output filter capacitors, but it has higher DCR (DC resistance of the inductor) loss, lower saturation current and has slower transient response. So, the practical inductor design is based on the inductor ripple current being ±15% to ±20% of the maximum operating DC current at maximum input voltage. Maximum ripple is at 50% duty cycle or $V_{BAT} = V_{IN,MAX}/2$. The required inductance can be calculated from Equation 16:

$$L = \frac{V_{IN,MAX}}{4 \cdot f_{SW} \cdot I_{RIPPLE}} \quad \text{(EQ. 16)}$$

Where $V_{IN,MAX}$ and f_{SW} are the maximum input voltage, and switching frequency, respectively.

The inductor ripple current ΔI is found from Equation 17:

$$I_{RIPPLE} = 0.3 \cdot I_{L,MAX} \quad \text{(EQ. 17)}$$

where the maximum peak-to-peak ripple current is 30% of the maximum charge current is used.

For $V_{IN,MAX}$ = 19V, V_{BAT} = 16.8V, $I_{BAT,MAX}$ = 2.6A, and f_S = 300kHz, the calculated inductance is 8.3µH. Choosing the closest standard value gives L = 10µH. Ferrite cores are often the best choice since they are optimized at 300kHz to 600kHz operation with low core loss. The core must be large enough not to saturate at the peak inductor current I_{Peak} in Equation 18:

$$I_{PEAK} = I_{L,MAX} + \frac{1}{2} \cdot I_{RIPPLE} \quad \text{(EQ. 18)}$$

Inductor saturation can lead to cascade failures due to very high currents. Conservative design limits the peak and RMS current in the inductor to less than 90% of the rated saturation current.

Cross over frequency is heavily dependant on the inductor value. f_{CO} should be less than 20% of the switching frequency and a conservative design has f_{CO} less than 10% of the switching frequency. The highest f_{CO} is in voltage control mode with the battery removed and may be calculated (approximately) from Equation 19:

$$f_{CO} = \frac{5 \cdot 11 \cdot R_{SENSE}}{2\pi \cdot L} \quad \text{(EQ. 19)}$$

Output Capacitor Selection

The output capacitor in parallel with the battery is used to absorb the high frequency switching ripple current and smooth the output voltage. The RMS value of the output ripple current I_{rms} is given by Equation 20:

$$I_{RMS} = \frac{V_{IN,MAX}}{\sqrt{12} \cdot L \cdot F_{SW}} \cdot D \cdot (1 - D) \quad \text{(EQ. 20)}$$

where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for continuous conduction mode which is typical operation for the battery charger. During the battery charge period, the output voltage varies from its initial battery voltage to the rated battery voltage. So, the duty cycle change can be in the range of between 0.53 and 0.88 for the minimum battery voltage of 10V (2.5V/Cell) and the maximum battery voltage of 16.8V. The maximum RMS value of the output ripple current occurs at the duty cycle of 0.5 and is expressed as Equation 21:

$$I_{RMS} = \frac{V_{IN,MAX}}{4 \cdot \sqrt{12} \cdot L \cdot f_{SW}} \quad \text{(EQ. 21)}$$

For $V_{IN,MAX}$ = 19V, VBAT = 16.8V, L = 10µH, and f_S = 300kHz, the maximum RMS current is 0.19A. A typical 10F ceramic capacitor is a good choice to absorb this current and also has very small size. Organic polymer capacitors have high capacitance with small size and have a significant equivalent series resistance (ESR). Although ESR adds to ripple voltage, it also creates a high frequency zero that helps the closed loop operation of the buck regulator.

EMI considerations usually make it desirable to minimize ripple current in the battery leads. Beads may be added in series with the battery pack to increase the battery impedance at 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and battery impedance. If the ESR of the output capacitor is 10mΩ and battery impedance is raised to 2Ω with a bead, then only 0.5% of the ripple current will flow in the battery.

MOSFET Selection

The Notebook battery charger synchronous buck converter has the input voltage from the AC adapter output. The maximum AC adapter output voltage does not exceed 25V. Therefore, 30V logic MOSFET should be used.

The high side MOSFET must be able to dissipate the conduction losses plus the switching losses. For the battery charger application, the input voltage of the synchronous buck converter is equal to the AC adapter output voltage, which is relatively constant. The maximum efficiency is achieved by selecting a high side MOSFET that has the conduction losses equal to the switching losses. Switching losses in the low-side FET are very small. The choice of low-side FET is a trade off between conduction losses ($r_{DS(ON)}$) and cost. A good rule of thumb for the $r_{DS(ON)}$ of the low-side FET is 2X the $r_{DS(ON)}$ of the high-side FET.

The LGATE gate driver can drive sufficient gate current to switch most MOSFETs efficiently. However, some FETs may exhibit cross conduction (or shoot through) due to current injected into the drain-to-source parasitic capacitor (C_{gd}) by the high dV/dt rising edge at the phase node when the high-side MOSFET turns on. Although LGATE sink current (1.8A typical) is more than enough to switch the FET off quickly, voltage drops across parasitic impedances between LGATE and the MOSFET can allow the gate to rise during the fast rising edge of voltage on the drain. MOSFETs with low threshold voltage (<1.5V) and low ratio of C_{gs}/C_{gd} (<5) and high gate resistance (>4Ω) may be turned on for a few ns by the high dV/dt (rising edge) on their drain. This can be avoided with higher threshold voltage and C_{gs}/C_{gd} ratio. Another way to avoid cross conduction is slowing the turn-on speed of the high-side MOSFET by connecting a resistor between the BOOT pin and the boot strap cap.

For the high-side MOSFET, the worst-case conduction losses occur at the minimum input voltage as shown in Equation 22:

$$P_{Q1,conduction} = \frac{V_{OUT}}{V_{IN}} \cdot I_{BAT}^2 \cdot r_{DS(ON)} \quad \text{(EQ. 22)}$$

The optimum efficiency occurs when the switching losses equal the conduction losses. However, it is difficult to

calculate the switching losses in the high-side MOSFET since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the MOSFET internal gate resistance, gate charge, threshold voltage, stray inductance, pull-up and pull-down resistance of the gate driver.

The following switching loss calculation (Equation 23) provides a rough estimate.

$$P_{Q1,\,Switching} = \frac{1}{2}V_{IN}I_{LV}f_{sw}\left(\frac{Q_{gd}}{I_{g,\,source}}\right) + \frac{1}{2}V_{IN}I_{LP}f_{sw}\left(\frac{Q_{gd}}{I_{g,\,sink}}\right) + Q_{rr}V_{IN}f_{sw} \quad \text{(EQ. 23)}$$

where the following are the peak gate-drive source/sink current of Q_1, respectively:

- Q_{gd}: drain-to-gate charge
- Q_{rr}: total reverse recovery charge of the body-diode in low-side MOSFET
- I_{LV}: inductor valley current
- I_{LP}: Inductor peak current
- $I_{g,sink}$
- $I_{g,source}$

Low switching loss requires low drain-to-gate charge Q_{gd}. Generally, the lower the drain-to-gate charge, the higher the ON-resistance. Therefore, there is a trade-off between the ON-resistance and drain-to-gate charge. Good MOSFET selection is based on the figure of Merit (FOM), which is a product of the total gate charge and ON-resistance. Usually, the smaller the value of FOM, the higher the efficiency for the same application.

For the low-side MOSFET, the worst-case power dissipation occurs at minimum battery voltage and maximum input voltage (Equation 24):

$$P_{Q2} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot I_{BAT}^{2} \cdot r_{DS(ON)} \quad \text{(EQ. 24)}$$

Choose a low-side MOSFET that has the lowest possible ON-resistance with a moderate-sized package like the SO-8 and is reasonably priced. The switching losses are not an issue for the low-side MOSFET because it operates at zero-voltage-switching.

Choose a Schottky diode in parallel with low-side MOSFET Q_2 with a forward voltage drop low enough to prevent the low-side MOSFET Q2 body-diode from turning on during the dead time. This also reduces the power loss in the high-side MOSFET associated with the reverse recovery of the low-side MOSFET Q_2 body diode.

As a general rule, select a diode with DC current rating equal to one-third of the load current. One option is to choose a combined MOSFET with the Schottky diode in a single package. The integrated packages may work better in practice because there is less stray inductance due to a short connection. This Schottky diode is optional and may be removed if efficiency loss can be tolerated. In addition, ensure that the required total gate drive current for the selected MOSFETs should be less than 24mA. So, the total gate charge for the high-side and low-side MOSFETs is limited by Equation 25:

$$Q_{GATE} \leq \frac{1_{GATE}}{f_{sw}} \quad \text{(EQ. 25)}$$

Where I_{GATE} is the total gate drive current and should be less than 24mA. Substituting I_{GATE} = 24mA and f_S = 300kHz into Equation 25 yields that the total gate charge should be less than 80nC. Therefore, the ISL6252 easily drives the battery charge current up to 10A.

Snubber Design

ISL6252's buck regulator operates in discontinuous current mode (DCM) when the load current is less than half the peak-to-peak current in the inductor. After the low-side FET turns off, the phase voltage rings due to the high impedance with both FETs off. This can be seen in Figure 9. Adding a snubber (resistor in series with a capacitor) from the phase node to ground can greatly reduce the ringing. In some situations a snubber can improve output ripple and regulation.

The snubber capacitor should be approximately twice the parasitic capacitance on the phase node. This can be estimated by operating at very low load current (100mA) and measuring the ringing frequency.

CSNUB and RSNUB can be calculated from Equations 26 and 27:

$$C_{SNUB} = \frac{2}{(2\pi F_{ring})^{2} \cdot L} \quad \text{(EQ. 26)}$$

$$R_{SNUB} = \sqrt{\frac{2 \cdot L}{C_{SNUB}}} \quad \text{(EQ. 27)}$$

Input Capacitor Selection

The input capacitor absorbs the ripple current from the synchronous buck converter, which is given by Equation 28:

$$I_{RMS} = I_{BAT}\frac{\sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(EQ. 28)}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC adapter is plugged into the battery charger. For Notebook battery charger applications, it is recommended that ceramic capacitors or polymer capacitors from Sanyo be used due to their small size and reasonable cost.

Table 2 shows the component lists for the typical application circuit in Figure 2.

TABLE 2. COMPONENT LIST

PARTS	PART NUMBERS AND MANUFACTURER
C_1, C_{10}	10µF/25V ceramic capacitor, Taiyo Yuden TMK325 MJ106MY X5R (3.2mmx2.5mmx1.9mm)
C_2, C_4, C_8	0.1µF/50V ceramic capacitor
C_3, C_7, C_9	1µF/10V ceramic capacitor, Taiyo Yuden LMK212BJ105MG
C_5	10nF ceramic capacitor
C_6	6.8nF ceramic capacitor
C_{11}	3300pF ceramic capacitor
D_1	30V/3A Schottky diode, EC31QS03L (optional)
D_2	100mA/30V Schottky Diode, Central Semiconductor
L	10µH/3.8A/26mΩ, Sumida, CDRH104R-100
Q_1, Q_2	30V/35mΩ, FDS6912A, Fairchild
Q_6	Signal N-Channel MOSFET, 2N7002
R_1	40mΩ, ±1%, LRC-LR2512-01-R040-F, IRC
R_2	20mΩ, ±1%, LRC-LR2010-01-R020-F, IRC
R_3	18Ω, ±5%, (0805)
R_4	2.2Ω, ±5%, (0805)
R_5	100kΩ, ±5%, (0805)
R_6	4.7k, ±5%, (0805)
R_7	100Ω, ±5%, (0805)
R_8, R_{11}	130k, ±1%, (0805)
R_9	10.2kΩ, ±1%, (0805)
R_{10}	4.7Ω, ±5%, (0805)
R_{12}	20kΩ, ±1%, (0805)
R_{13}	1.87kΩ, ±1%, (0805)

Loop Compensation Design

ISL6252 has three closed loop control modes. One controls the output voltage when the battery is fully charged or absent. A second controls the current into the battery when charging and the third limits current drawn from the adapter. The charge current and input current control loops are compensated by a single capacitor on the ICOMP pin. The voltage control loop is compensated by a network on the VCOMP pin. Descriptions of these control loops and guidelines for selecting compensation components will be given in the following sections. Which loop controls the output is determined by the minimum current buffer and the minimum voltage buffer shown in Figure 1. These three loops will be described separately.

TRANSCONDUCTANCE AMPLIFIERS GM1, GM2 AND GM3

ISL6252 uses several transconductance amplifiers (also known as gm amps). Most commercially available op amps are voltage controlled voltage sources with gain expressed as $A = V_{OUT}/V_{IN}$.gm amps are voltage controlled current sources with gain expressed as $gm = I_{OUT}/V_{IN}$.gm will appear in some of the equations for poles and zeros in the compensation.

PWM GAIN F_M

The Pulse Width Modulator in the ISL6252 converts voltage at VCOMP to a duty cycle by comparing VCOMP to a triangle wave (duty = $VCOMP/V_{PP\ RAMP}$). The low-pass filter formed by L and C_O convert the duty cycle to a DC output voltage ($Vo = V_{DCIN}$*duty). In ISL6252, the triangle wave amplitude is proportional to V_{DCIN}. Making the ramp amplitude proportional to DCIN makes the gain from VCOMP to the PHASE output a constant 11 and is independent of DCIN. For small signal AC analysis, the battery is modeled by it's internal resistance. The total output resistance is the sum of the sense resistor and the internal resistance of the MOSFETs, inductor and capacitor. Figure 18 shows the small signal model of the pulse width modulator (PWM), power stage, output filter and battery.

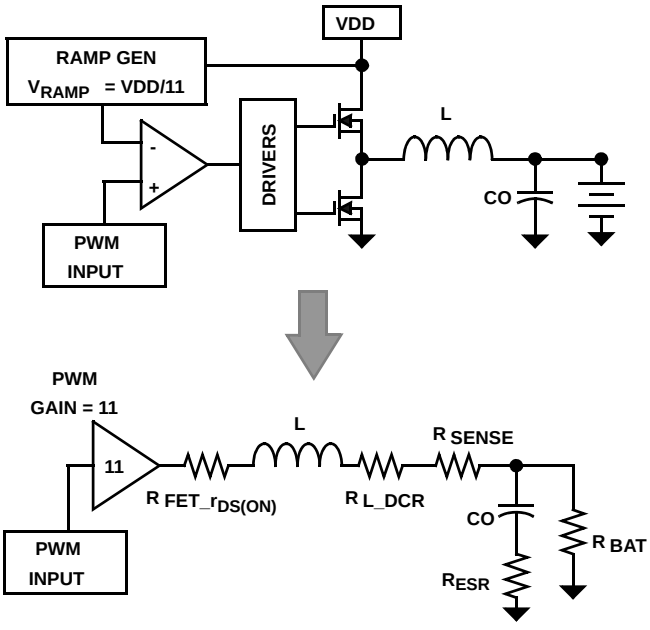


FIGURE 18. SMALL SIGNAL AC MODEL

In most cases the Battery resistance is very small (<200mΩ) resulting in a very low Q in the output filter. This results in a frequency response from the input of the PWM to the inductor current with a single pole at the frequency calculated in Equation 29:

$$f_{POLE1} = \frac{(R_{SENSE} + r_{DS(ON)} + R_{DCR} + R_{BAT})}{2\pi \cdot L} \quad \text{(EQ. 29)}$$

The output capacitor creates a pole at a very high frequency due to the small resistance in parallel with it. The frequency of this pole is calculated in Equation 30:

$$f_{POLE2} = \frac{1}{2\pi \cdot C_o \cdot R_{BAT}} \quad \text{(EQ. 30)}$$

CHARGE CURRENT CONTROL LOOP

When the battery voltage is less than the fully charged voltage, the voltage error amplifier goes to it's maximum output (limited to 1.2V above ICOMP) and the ICOMP voltage controls the loop through the minimum voltage buffer. Figure 19 shows the charge current control loop.

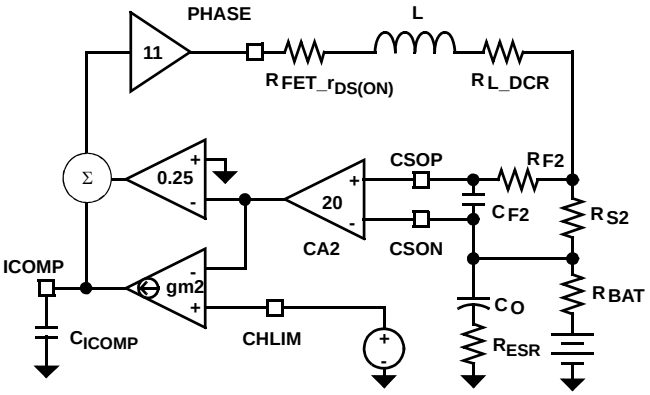


FIGURE 19. CHARGE CURRENT LIMIT LOOP

The compensation capacitor (C_{ICOMP}) gives the error amplifier (GMI) a pole at a very low frequency (<<1Hz) and a a zero at f_{Z1}. f_{Z1} is created by the 0.25*CA2 output added to ICOMP. The frequency of can be calculated from Equation 31:

$$f_{ZERO} = \frac{4 \cdot gm2}{(2\pi \cdot C_{ICOMP})} \qquad gm2 = \frac{50\mu A}{V} \quad \text{(EQ. 31)}$$

Placing this zero at a frequency equal to the pole calculated in Equation 29 will result in maximum gain at low frequencies and phase margin near 90°. If the zero is at a higher frequency (smaller C_{ICOMP}), the DC gain will be higher but the phase margin will be lower. Use a capacitor on ICOMP that is equal to or greater than the value calculated in Equation 32:

$$C_{ICOMP} = \frac{4 \cdot (50\mu A/V)}{(R_{S2} + r_{DS(ON)} + R_{DCR} + R_{BAT})} \quad \text{(EQ. 32)}$$

A filter should be added between R_{S2} and CSOP and CSON to reduce switching noise. The filter roll off frequency should be between the cross over frequency and the switching frequency (~100kHz). R_{F2} should be small (<10Ω) to minimize offsets due to leakage current into CSOP. The filter cut off frequency is calculated using Equation 33:

$$f_{FILTER} = \frac{1}{(2\pi \cdot C_{F2} \cdot R_{F2})} \quad \text{(EQ. 33)}$$

The cross over frequency is determined by the DC gain of the modulator and output filter and the pole in Equation 23.

The DC gain is calculated in Equation 34 and the cross over frequency is calculated with Equation 35.

$$A_{DC} = \frac{11 \cdot R_{S2}}{(R_{S2} + r_{DS(ON)} + R_{DCR} + R_{BATTERY})} \quad \text{(EQ. 34)}$$

$$f_{CO} = A_{DC} \cdot f_{POLE} = \frac{11 \cdot R_{S2}}{2\pi \cdot L} \quad \text{(EQ. 35)}$$

The bode plot of the loop gain, the compensator gain and the power stage gain is shown in Figure 20:

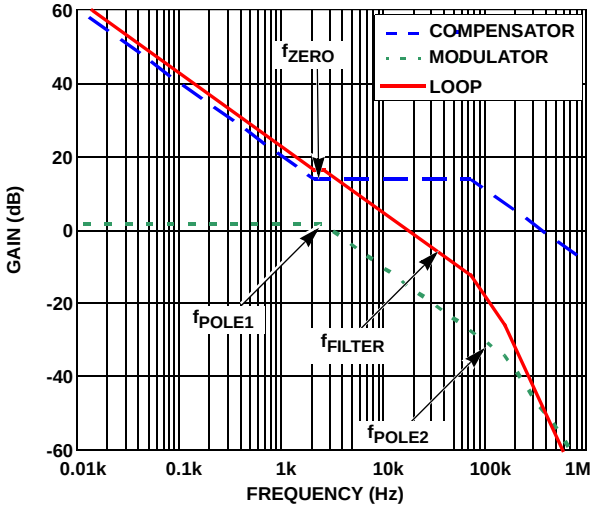


FIGURE 20. CHARGE CURRENT LOOP BODE PLOTS

Adapter Current Limit Control Loop

If the combined battery charge current and system load current draws current that equals the adapter current limit set by the ACLIM pin, ISL6252 will reduce the current to the battery and/or reduce the output voltage to hold the adapter current at the limit. Above the adapter current limit, the minimum current buffer equals the output of gm3 and ICOMP controls the charger output. Figure 21 shows the adapter current limit control loop.

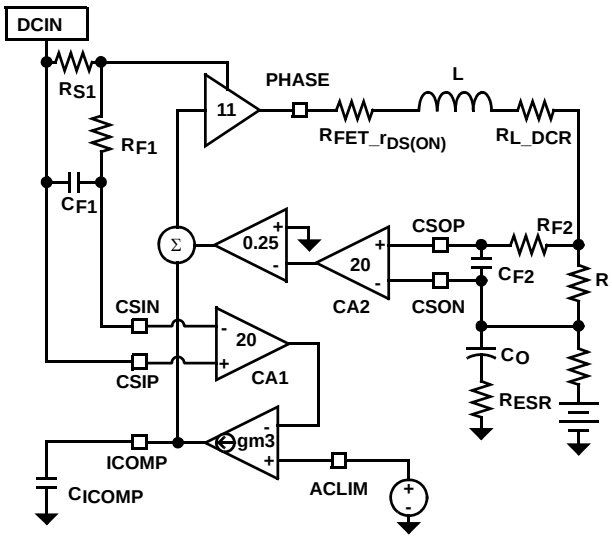


FIGURE 21. ADAPTER CURRENT LIMIT LOOP

The loop response equations, bode plots and the selection of C_{ICOMP} are the same as the charge current control loop with loop gain reduced by the duty cycle and the ratio of R_{S1}/R_{S2}. In other words, if $R_{S1}= R_{S2}$ and the duty cycle D = 50%, the loop gain will be 6dB lower than the loop gain in Figure 20. This gives lower cross over frequency and higher phase margin in this mode. If $R_{S1}/R_{S2} = 2$ and the duty cycle is 50% then the adapter current loop gain will be identical to the gain in Figure 20.

A filter should be added between R_{S1} and CSIP and CSIN to reduce switching noise. The filter roll off frequency should be between the cross over frequency and the switching frequency (~100kHz).

Voltage Control Loop

When the battery is charged to the voltage set by CELLS and VADJ the voltage error amplifier (gm1) takes control of the output (assuming that the adapter current is below the limit set by ACLIM). The voltage error amplifier (gm1) discharges the cap on VCOMP to limit the output voltage. The current to the battery decreases as the cells charge to the fixed voltage and the voltage across the internal battery resistance decreases. As battery current decreases the 2 current error amplifiers (gm2 and gm3) output their maximum current and charge the capacitor on ICOMP to its maximum voltage (limited to 1.2V above VCOMP). With high voltage on ICOMP, the minimum voltage buffer output equals the voltage on VCOMP. The voltage control loop is shown in Figure 22.

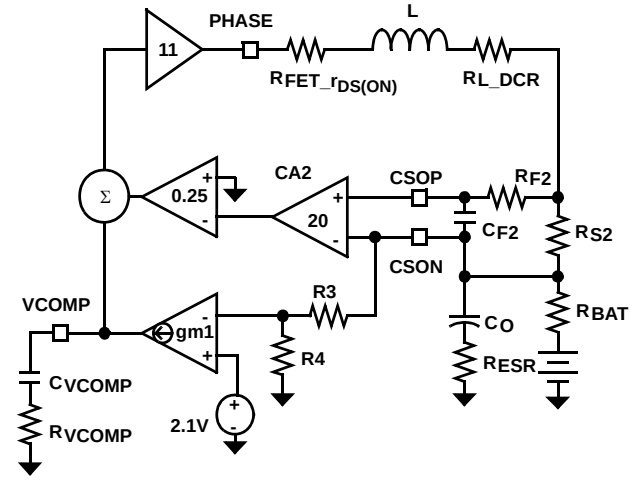


FIGURE 22. VOLTAGE CONTROL LOOP

Output LC Filter Transfer Functions

The gain from the phase node to the system output and battery depend entirely on external components. Typical output LC filter response is shown in Figure 23. Transfer function $A_{LC}(s)$ is shown in Equation 36:

$$A_{LC} = \frac{\left(1 - \frac{s}{\omega_{ESR}}\right)}{\left(\frac{s^2}{\omega_{DP}} + \frac{s}{(\omega_{LC} \cdot Q)} + 1\right)} \quad \text{(EQ. 36)}$$

$$\omega_{ESR} = \frac{1}{(R_{ESR} \cdot C_o)} \qquad \omega_{LC} = \frac{1}{(\sqrt{L \cdot C_o})} \qquad Q = R_o \cdot \sqrt{\frac{L}{C_o}}$$

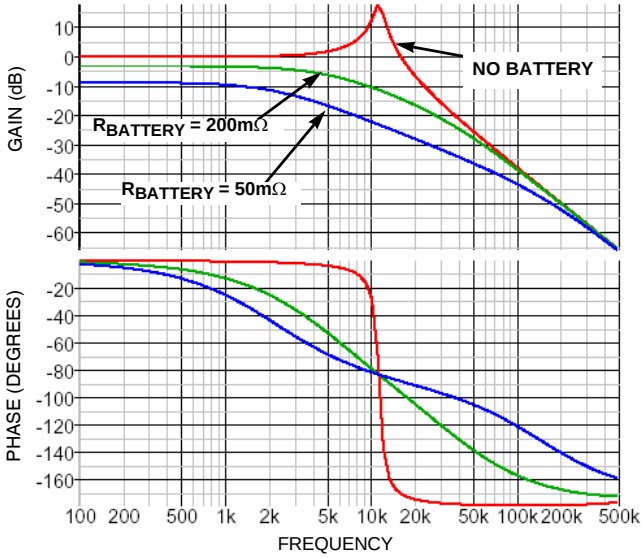


FIGURE 23. FREQUENCY RESPONSE OF THE LC OUTPUT FILTER

The resistance R_O is a combination of MOSFET $r_{DS(ON)}$, inductor DCR, R_{SENSE} and the internal resistance of the battery (normally between 50mΩ and 200mΩ). The worst case for voltage mode control is when the battery is absent. This results in the highest Q of the LC filter and the lowest phase margin.

The compensation network consists of the voltage error amplifier gm1 and the compensation network R_{VCOMP}, C_{VCOMP}, which give the loop very high DC gain, a very low frequency pole and a zero at f_{ZERO1}. Inductor current information is added to the feedback to create a second zero, f_{ZERO2}. The low pass filter R_{F2}, C_{F2} between R_{SENSE} and ISL6252 add a pole at f_{FILTER}. R_3 and R_4 are internal divider resistors that set the DC output voltage. For a 3-cell battery, R_3 = 320kΩ and R_4 = 64kΩ. Equations 37, 38, 39, 40, 41 and 42 relate the compensation network's poles, zeros and gain to the components in Figure 22. Figure 24 shows an asymptotic bode plot of the DC/DC converter's gain vs frequency. It is strongly recommended that f_{ZERO1} is approximately 30% of f_{LC} and f_{ZERO2} is approximately 70% of f_{LC}.

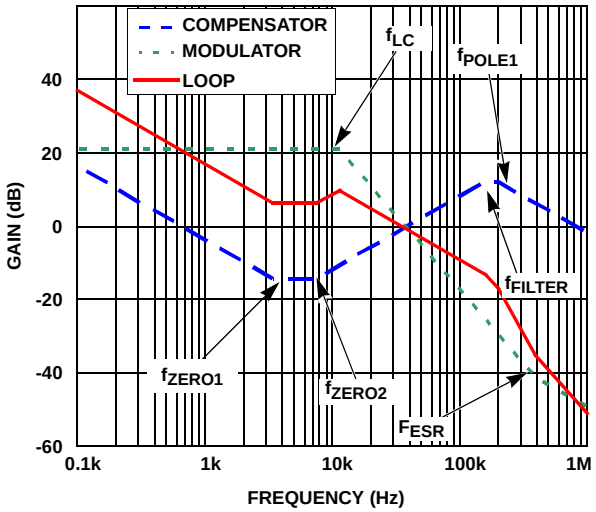


FIGURE 24. ASYMPTOTIC BODE PLOT OF THE VOLTAGE CONTROL LOOP GAIN

COMPENSATION BREAK FREQUENCY EQUATIONS

$$f_{ZERO1} = \frac{1}{(2\pi \cdot C_{VCOMP} \cdot R_{1COMP})} \quad \text{(EQ. 37)}$$

$$f_{ZERO2} = \left(\frac{R_{VCOMP}}{2\pi \cdot R_{SENSE} \cdot C_{OUT}}\right) \cdot \left(\frac{R_4}{R_4 + R_3}\right) \cdot \left(\frac{gm1}{5}\right) \quad \text{(EQ. 38)}$$

$$f_{LC} = \frac{1}{(2\pi \sqrt{L \cdot C_o})} \quad \text{(EQ. 39)}$$

$$f_{FILTER} = \frac{1}{(2\pi \cdot R_{F2} \cdot C_{F2})} \quad \text{(EQ. 40)}$$

$$f_{POLE1} = \frac{1}{(2\pi \cdot R_{SENSE} \cdot C_o)} \quad \text{(EQ. 41)}$$

$$f_{ESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 42)}$$

TABLE 3.

CELLS	R_3	R_4
2	288kΩ	48kΩ
3	320kΩ	64kΩ
4	336kΩ	96kΩ

Choose R_{VCOMP} equal or lower than the value calculated from Equation 43:

$$R_{VCOMP} = (0.7 \cdot f_{LC}) \cdot (2\pi \cdot C_o \cdot R_{SENSE}) \cdot \left(\frac{5}{gm1}\right) \cdot \left(\frac{R_3 + R_4}{R_4}\right) \quad \text{(EQ. 43)}$$

Next, choose C_{VCOMP} equal or higher than the value calculated from Equation 44:

$$C_{VCOMP} = \frac{1}{(0.3 \cdot f_{LC}) \cdot (2\pi \cdot R_{VCOMP})} \quad \text{(EQ. 44)}$$

PCB Layout Considerations

Power and Signal Layers Placement on the PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with signal layers on the opposite side of the board. As an example, layer arrangement on a 4-layer board is shown below:

1. Top Layer: signal lines, or half board for signal lines and the other half board for power lines
2. Signal Ground
3. Power Layers: Power Ground
4. Bottom Layer: Power MOSFET, Inductors and other Power traces

Separate the power voltage and current flowing path from the control and logic level signal path. The controller IC will stay on the signal layer, which is isolated by the signal ground to the power signal traces.

Component Placement

The power MOSFET should be close to the IC so that the gate drive signal, the LGATE, UGATE, PHASE, and BOOT, traces can be short.

Place the components in such a way that the area under the IC has less noise traces with high dv/dt and di/dt, such as gate signals and phase node signals.

Signal Ground and Power Ground Connection

At minimum, a reasonably large area of copper, which will shield other noise couplings through the IC, should be used as signal ground beneath the IC. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each side, where there is little noise; a noisy trace beneath the IC is not recommended.

GND and VDD Pin

At least one high quality ceramic decoupling cap should be used to cross these two pins. The decoupling cap can be put close to the IC.

LGATE Pin

This is the gate drive signal for the bottom MOSFET of the buck converter. The signal going through this trace has both high dv/dt and high di/dt, and the peak charging and discharging current is very high. These two traces should be short, wide, and away from other traces. There should be no other traces in parallel with these traces on any layer.

PGND Pin

PGND pin should be laid out to the negative side of the relevant output cap with separate traces.The negative side of the output capacitor must be close to the source node of the bottom MOSFET. This trace is the return path of LGATE.

PHASE Pin

This trace should be short, and positioned away from other weak signal traces. This node has a very high dv/dt with a

voltage swing from the input voltage to ground. No trace should be in parallel with it. This trace is also the return path for UGATE. Connect this pin to the high-side MOSFET source.

UGATE Pin

This pin has a square shape waveform with high dv/dt. It provides the gate drive current to charge and discharge the top MOSFET with high di/dt. This trace should be wide, short, and away from other traces similar to the LGATE.

BOOT Pin

This pin's di/dt is as high as the UGATE; therefore, this trace should be as short as possible.

CSOP, CSON, CSIP and CSIN Pins

Accurate charge current and adapter current sensing is critical for good performance. The current sense resistor connects to the CSON and the CSOP pins through a low pass filter with the filter cap very near the IC (see Figure 2). Traces from the sense resistor should start at the pads of the sense resistor and should be routed close together, throughout the low pass filter and to the CSON and CSON pins (see Figure 25). The CSON pin is also used as the battery voltage feedback. The traces should be routed away from the high dv/dt and di/dt pins like PHASE, BOOT pins. In general, the current sense resistor should be close to the IC. These guidelines should also be followed for the adapter current sense resistor and CSIP and CSIN. Other layout arrangements should be adjusted accordingly.

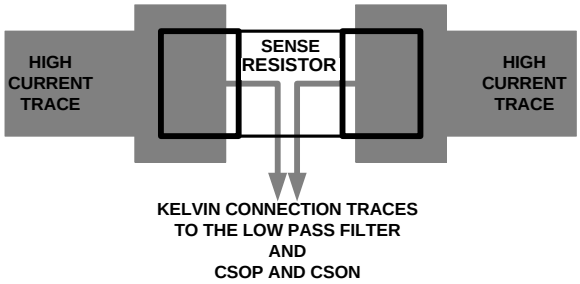


FIGURE 25. CURRENT SENSE RESISTOR LAYOUT

EN Pin

This pin stays high at enable mode and low at idle mode and is relatively robust. Enable signals should refer to the signal ground.

DCIN Pin

This pin connects to AC adapter output voltage, and should be less noise sensitive.

Copper Size for the Phase Node

The capacitance of PHASE should be kept very low to minimize ringing. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

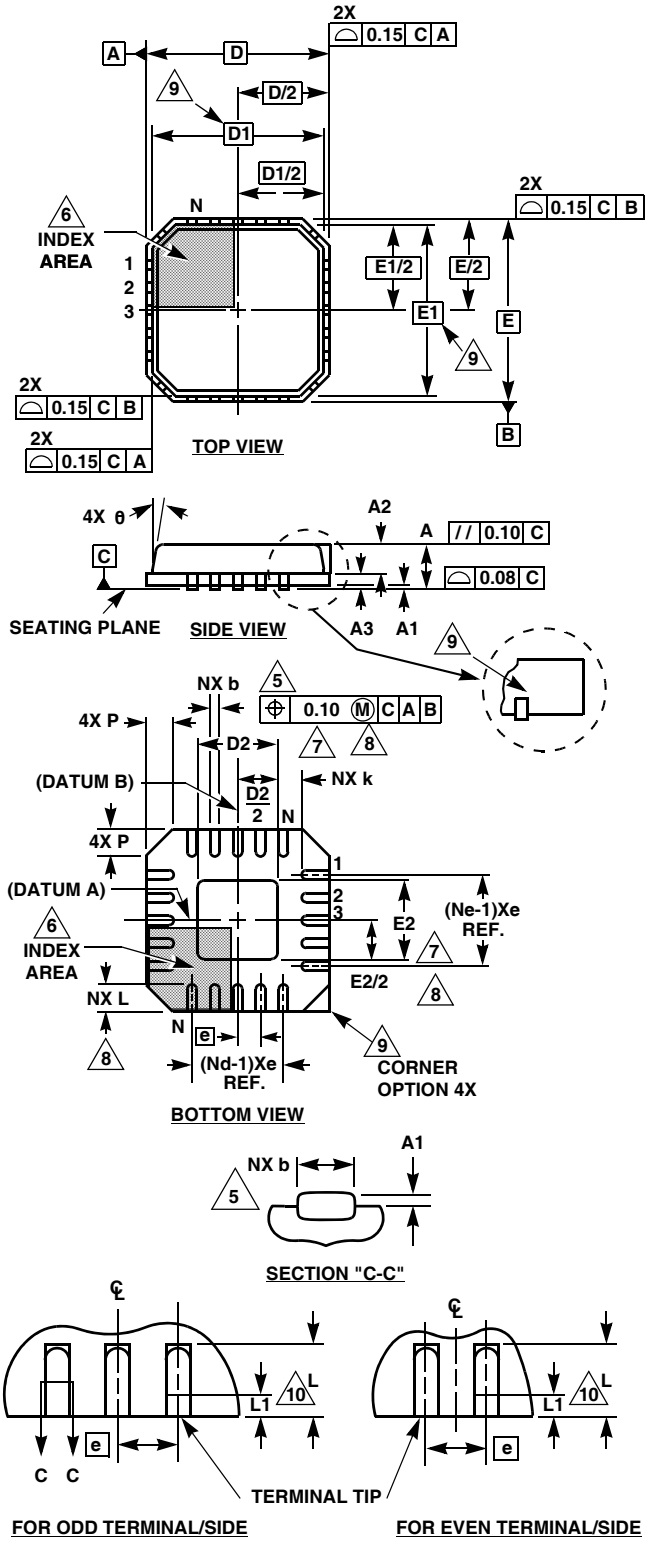
Identify the Power and Signal Ground

The input and output capacitors of the converters, the source terminal of the bottom switching MOSFET PGND should connect to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at one point.

Clamping Capacitor for Switching MOSFET

It is recommended that ceramic caps be used closely connected to the drain of the high-side MOSFET, and the source of the low-side MOSFET. This capacitor reduces the noise and the power loss of the MOSFET.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.5x5

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-1 ISSUE I)

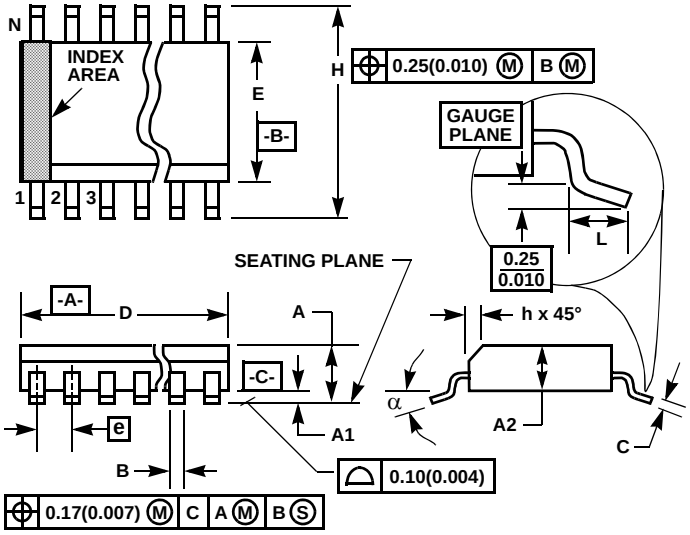
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.50	0.60	0.75	8
N		28		2
Nd		7		3
Ne		7		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M24.15

24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.55	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 2 6/04

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com