

32-bit RISC Microcontroller

CMOS

FR30 Series MB91121

MB91121

■ DESCRIPTION

The MB91121 is a microcontroller with a 32-bit RISC CPU (FR family *) as the core, incorporating a variety of I/O resources, a bus control facility, and a multiplier-accumulator (simplified DSP) with internal program RAM for built-in control applications which require advanced, high-speed CPU processing.

While being based on external bus access for supporting a vast address space accessed by the 32-bit CPU, it contains 1 K bytes of instruction cache memory and 4 K bytes of RAM (8 K bytes when the DSP is not used) for speeding up the execution of instructions by the CPU.

In this way, the device is designed for built-in applications which require high performance and processing power of the CPU, such as digital camera, navigation system, and high-performance FAX, and printer controls.

* : FR Family stands for FUJITSU RISC controller.

■ FEATURES

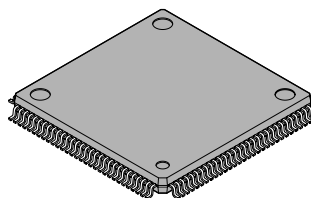
1. FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency : Internal 50 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
- General purpose registers : 32 bits × 16
- 16-bit fixed length instructions (basic instructions) , 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing : Optimized for embedded applications

(Continued)

■ PACKAGE

120-pin plastic LQFP



(FPT-120P-M21)

(Continued)

- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages
- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots : Reduced overhead time in branch executions
- Internal multiplier/supported at instruction level
 - Signed 32-bit multiplication : 5 cycles
 - Signed 16-bit multiplication : 3 cycles
- Interrupt (push PC and PS) : 6 cycles, 16 priority levels

2. Bus interface

- Clock doubler : Internal 50 MHz, external bus 25 MHz operation
- 25-bit address bus (32 Mbytes memory space)
- 8/16-bit data bus
- Basic external bus cycle : 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 Kbytes : 6
- Interface supported for various memory technologies
 - DRAM interface (area 4 and 5)
- Automatic wait cycle insertion : Flexible setting, from 0 to 7 for each area
- Unused data/address pins can be configured as input/output ports.
- Little endian mode supported (Select 1 area from area 1 to 5)

3. DRAM interface

- 2 banks independent control (area 4 and 5)
- Double CAS DRAM (Normal DRAM I/F) /Single CAS DRAM/Hyper DRAM
- Basic bus cycle : Normally 5 cycles, 2-cycle access possible in high-speed page mode
- Programmable waveform : Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
 - CBR refresh (interval time configurable by 6-bit timer)
 - Self-refresh mode
- Supports 8/9/10/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

4. DSP Macros (Simplified DSP)

- High-speed multiply-accumulate operation (1 machine cycle)
- Data format : 16-bit fixed-point ($16 \times 16 + 40$ bits)
- Instruction area : 256 words \times 16 bits
- Data area : 64 words \times 16 bits \times 1 set, 1024 words \times 16 bits \times 2 sets (banks)
- Capable of rounding and saturation processing
- Number of terms in addition : Up to 32 terms
- Instructions : MAC, STR, and JMP instructions
- Delay processing : Capable of free transfer within 32 words
- Fixed-point system : Capable of selection from among Q12 to Q15
- Program execution control : Capable of externally selecting eight calculation programs
- Variable monitoring : Capable of monitoring calculation results of up to 4 words without stopping the program
- Efficient data variable areas : Two banks of data variable areas provided, enabling the CPU to execute a DSP calculation program using one bank while accessing a data variable in the other.

5. Cache memory

- 1 K-byte instruction cache
- 2-way set-associative configuration
- 32 blocks/way, 4 entries (4 words) /block

(Continued)

- Lock feature: Keeping a specific program code resident in the cache

6. DMAC (DMA Controller)

- 8 channels
- Transfer incident/external pins/UART interrupt requests/DSP Macros/Software start
- Transfer sequence : Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length : 8 bits/16 bits/32 bits selective
- Interrupt request enables temporary stop operation

7. UART

- 3 independent channels
- Full-duplex double buffer
- Data length : 7 bits to 9 bits (non-parity) , 6 bits to 8 bits (parity)
- Asynchronous (start-stop system) , CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator : Generates any given baud rate
- Use external clock can be used as a transfer clock
- Error detection : Parity, frame, overrun

8. A/D converter (successive approximation conversion type)

- 10-bit resolution, 8 channels
- Successive approximation type : Conversion time of 5.6 μ s at 25 MHz
- Internal sample and hold circuit
- Conversion mode : Single conversion/scanning conversion/repeated conversion selective
- Start : Software/external trigger/internal timer selective

9. Reload timer

- 16-bit timer : 3 channels
- Internal clock : 2 clock cycle resolution, divide by 2/8/32 selective

10. Other interval timers

- 16-bit timer : 3 channels (U-TIMER)
- PWM timer : 4 channels
- Watchdog timer : 1 channel

11. Bit search module

- First bit transition "1" or "0" from MSB can be detected in 1 cycle

12. Interrupt controller

- External interrupt input : Non-maskable interrupt ($\overline{\text{NMI}}$) , normal interrupt $\times 8$ (INT0 to INT7)
- Internal interrupt incident : UART, DMA controller (DMAC) , A/D converter, U-TIMER, delayed interrupt module and DSP Macros
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 steps) .

Others

1. Reset cause

- Power-on reset/watchdog timer/software reset/external reset

2. Low-power consumption mode

- Sleep mode/stop mode

3. Clock control

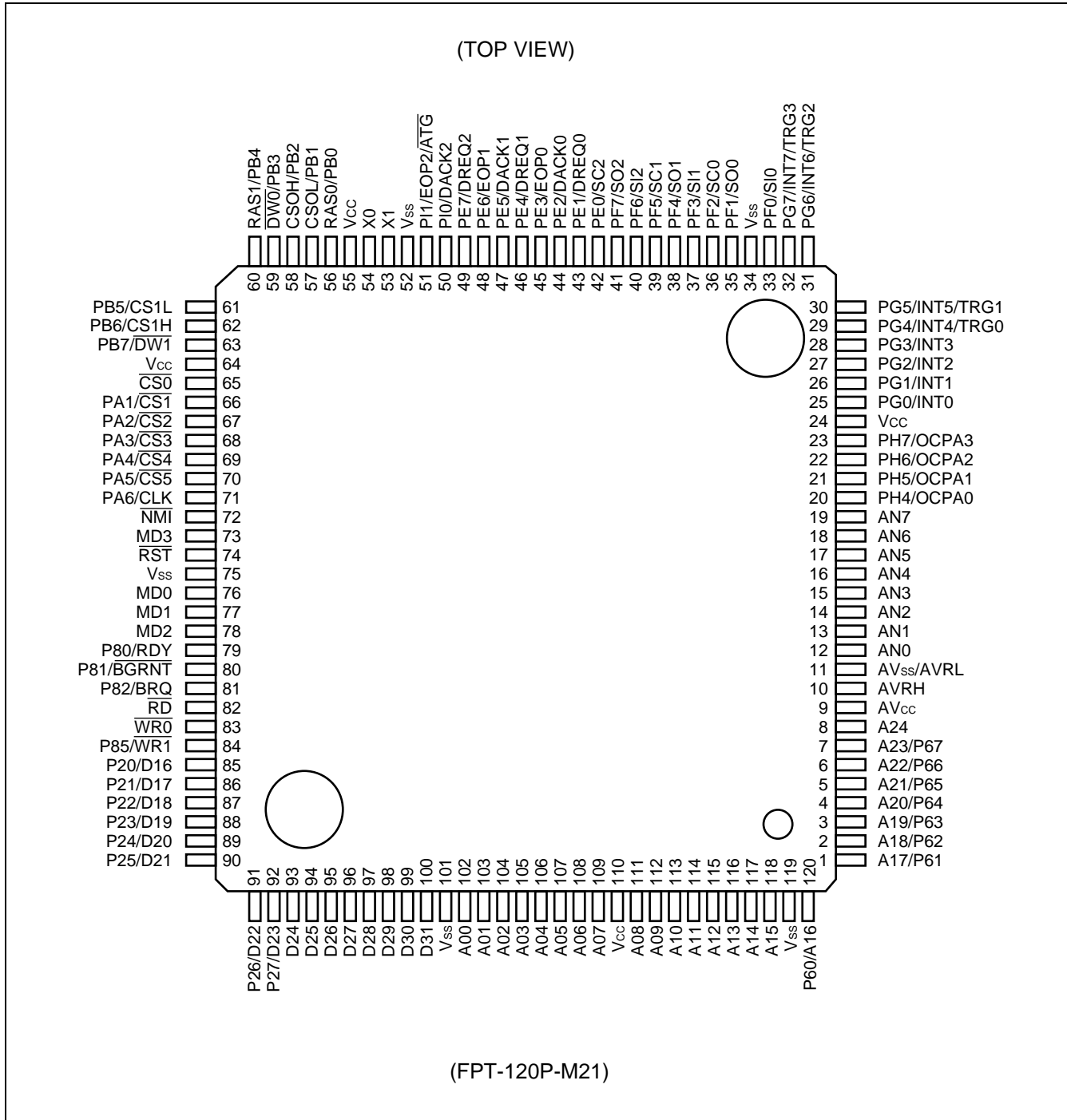
- Gear function : Operating clocks for CPU and peripherals are independently selective
Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16)
However, operating frequency for peripherals is less than 25 MHz.

MB91121

(Continued)

4. Packages : LQFP-120
5. CMOS technology (0.35 μm)
6. Power supply voltage 3.3 V \pm 0.3 V

PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function	
1 2 3 4 5 6 7	A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66 A23/P67	F	Bits 16 to 23 for the external address bus. When not used for the address bus, these pins serve as ports (P60 to P67) .	
8	A24	M	Bit 24 for the external address bus	
9	AV _{CC}	—	A/D converter V _{CC} power supply	
10	AVRH	—	A/D converter reference voltage (high potential side) The V _{CC} pin must be applied with voltage equal to or higher than the voltage at this pin (AVRH) when the AVRH pin is turned on or off.	
11	AV _{SS} /AVRL	—	A/D converter V _{SS} power supply or reference voltage (low potential side)	
12 to 19	AN0 to AN7	N	[AN0 to AN7] A/D converter analog input. This function is enabled with the AIC register set for the analog input.	
20 to 23	OCPA0/PH4 OCPA1/PH5 OCPA2/PH6 OCPA3/PH7	F	[OCPA0 to OCPA3] PWM timer output. This function is enabled with the PWM timer output flag set to "Enabled".	
			[PH4 to PH7] General-purpose I/O port	
25 to 32	INT0/PG0 INT1/PG1 INT2/PG2 INT3/PG3 INT4/PG4/TRG0 INT5/PG5/TRG1 INT6/PG6/TRG2 INT7/PG7/TRG3	F	[INT0 to INT7] External interrupt request input	Since these inputs are used during their respective input operations, the output by the other function must remain off unless used intentionally.
			[TRG0 to TRG3] PWM timer external trigger input	
			[PG0 to PG7] General-purpose I/O port	
33	SI0/PF0	F	[SI0] UART0 data input. Since this input is used whenever UART0 is in input operation, the output by the other function must remain off unless used intentionally.	
			[PF0] General-purpose I/O port	
35	SO0/PF1	F	[SO0] UART0 data output. This function is enabled with the UART0 data output flag set to "Enabled".	
			[PF1] General-purpose I/O port. This function is enabled with the UART0 data output flag set to "Disabled".	
36	SC0/PF2	F	[SC0] UART0 clock input/output. The clock output is enabled with the UART0 clock output flag set to "Enabled".	
			[PF2] General-purpose I/O port. This function is enabled with the UART0 clock output flag set to "Disabled".	

(Continued)

(Continued)

Pin no.	Pin name	Circuit type	Function
37	SI1/PF3	F	[SI1] UART1 data input. Since this input is used whenever UART1 is in input operation, the output by the other function must remain off unless used intentionally.
			[PF3] General-purpose I/O port
38	SO1/PF4	F	[SO1] UART1 data output. This function is enabled with the UART1 data output flag set to "Enabled".
			[PF4] General-purpose I/O port. This function is enabled with the UART1 data output flag set to "Disabled".
39	SC1/PF5	F	[SC1] UART1 clock input/output. The clock output is enabled with the UART1 clock output flag set to "Enabled".
			[PF5] General-purpose I/O port. This function is enabled with the UART1 clock output flag set to "Disabled".
40	SI2/PF6	F	[SI2] UART2 data input. Since this input is used whenever UART2 is in input operation, the output by the other function must remain off unless used intentionally.
			[PF6] General-purpose I/O port
41	SO2/PF7	F	[SO2] UART2 data output. This function is enabled with the UART2 data output flag set to "Enabled".
			[PF7] General-purpose I/O port. This function is enabled with the UART2 data output flag set to "Disabled".
42	SC2/PE0	F	[SC2] UART2 clock input/output. The clock output is enabled with the UART2 clock output flag set to "Enabled".
			[PE0] General-purpose I/O port. This function is enabled with the UART2 clock output flag set to "Disabled".
43	DREQ0/PE1	F	[DREQ0] DMA external transfer request input (ch0) . Since this input is used whenever the DMA external transfer request has been selected as a DMA transfer trigger event, the output by the other function must remain off unless used intentionally.
			[PE1] General-purpose I/O port
44	DACK0/PE2	F	[DACK0] DMAC external transfer request acknowledge output (ch0) . This function is enabled with the DMAC transfer request acknowledge output flag set to "Enabled".
			[PE2] General-purpose I/O port. This function is enabled with the DMAC transfer request acknowledge output flag or DACK0 output flag set to "Disabled".
45	EOP0/PE3	F	[EOP0] DMAC EOP output (ch0) . This function is enabled with the EOP output flag set to "Enabled".
			[PE3] General-purpose I/O port
46	DREQ1/PE4	F	[DREQ1] DMA external transfer request input (ch1) . Since this input is used whenever the DMA external transfer request has been selected as a DMA transfer trigger event, the output by the other function must remain off unless used intentionally.
			[PE4] General-purpose I/O port

(Continued)

MB91121

(Continued)

Pin no.	Pin name	Circuit type	Function
47	DACK1/PE5	F	[DACK1] DMAC external transfer request acknowledge output (ch1) . This function is enabled with the DMAC transfer request acknowledge output flag set to "Enabled".
			[PE5] General-purpose I/O port. This function is enabled with the DMAC transfer request acknowledge output flag or DACK0 output flag set to "Disabled".
48	EOP1/PE6	F	[EOP1] DMAC EOP output (ch1) . This function is enabled with the EOP output flag set to "Enabled".
			[PE6] General-purpose I/O port
49	DREQ2/PE7	F	[DREQ2] DMA external transfer request input (ch2) . Since this input is used whenever the DMA external transfer request has been selected as a DMA transfer trigger event, the output by the other function must remain off unless used intentionally.
			[PE7] General-purpose I/O port
50	DACK2/PI0	F	[DACK2] DMAC external transfer request acknowledge output (ch2) . This function is enabled with the DMAC transfer request acknowledge output flag set to "Enabled".
			[PI0] General-purpose I/O port. This function is enabled with the DMAC transfer request acknowledge output flag or DACK0 output flag set to "Disabled".
51	EOP2/ $\overline{\text{ATG}}$ /PI1	F	[EOP2] DMAC EOP output (ch2) . This function is enabled with the EOP output flag set to "Enabled".
			$\overline{\text{ATG}}$ A/D converter external trigger input. Since this input is used whenever the A/D converter external trigger signal has been selected as an A/D trigger event, the output by the other function must remain off unless used intentionally.
			[PI1] General-purpose I/O port. This function is enabled with the DMAC transfer termination signal output flag set to "Disabled".
53 54	X1 X0	A	Clock (oscillation) output. Clock (oscillation) input.
56 57 58 59 60	RAS0/PB0 CSOL/PB1 CSOH/PB2 $\overline{\text{DW0}}$ /PB3 RAS1/PB4	F	RAS output of DRAM bank 0 CASL output of DRAM bank 0 CASH output of DRAM bank 0 $\overline{\text{WE}}$ output of DRAM bank 0 (Low active) RAS output of DRAM bank 1 [PB0 to PB3] Can serve as a port when not used for signal output.
61 62 63	CS1L/PB5 CS1H/PB6 $\overline{\text{DW1}}$ /PB7	F	CASL output of DRAM bank 1 CASH output of DRAM bank 1 $\overline{\text{WE}}$ output of DRAM bank 1 (Low active) [PB5 to PB7] Can serve as a port when not used for signal output.
65	$\overline{\text{CS0}}$	M	Chip select 0 output (Low active) .

(Continued)

(Continued)

Pin no.	Pin name	Circuit type	Function									
66 67 68 69 70	$\overline{CS1}/PA1$ $\overline{CS2}/PA2$ $\overline{CS3}/PA3$ $\overline{CS4}/PA4$ $\overline{CS5}/PA5$	F	Chip select 1 output (Low active) . Chip select 2 output (Low active) . Chip select 3 output (Low active) . Chip select 4 output (Low active) . Chip select 5 output (Low active) . [PA1 to PA5] Can serve as a port when not used for signal output.									
71	CLK/PA6	F	System clock output. This pin outputs the same clock frequency as the external bus operating frequency. [PA6] Can serve as a port when not used for signal output.									
72	\overline{NMI}	H	NMI (Non Maskable Interrupt) input (Low active) .									
73	MD3	G	Mode pin 3. Connect this pin directly to the V_{CC} or V_{SS} pin.									
74	\overline{RST}	B	External reset input.									
76 77 78	MD0 MD1 MD2	G	Mode pins 0 to 2. These pins are set to MCU basic operation modes. Connect this pin directly to the V_{CC} or V_{SS} pin.									
79	RDY/P80	C	External ready signal input. This pin inputs 0 when the bus cycle being executed is not completed. It can serve as a port when not used for that input.									
80	$\overline{BGRNT}/P81$	F	External bus release request acknowledge output. This pin outputs the L signal when the external bus has been released. The pin can serve as a port when not used for that output.									
81	BRQ/P82	C	External bus release request input. Input 1 to this pin to release the external bus. The pin can serve as a port when not used for that input.									
82	\overline{RD}	M	External bus read strobe.									
83	$\overline{WR0}$	M	External bus write strobe. The control signals and data bus byte locations have the following relationships.									
84	$\overline{WR1}/P85$	F	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>16-bit bus width</th> <th>8-bit bus width</th> </tr> </thead> <tbody> <tr> <td>D31 to D24</td> <td>$\overline{WR0}$</td> <td>$\overline{WR0}$</td> </tr> <tr> <td>D23 to D16</td> <td>$\overline{WR1}$</td> <td>(Usable as port)</td> </tr> </tbody> </table> <p>Note : $\overline{WR1}$ remains in the Hi-Z state during a reset. For use with a 16-bit bus width, add an external pull-up resistor.</p>		16-bit bus width	8-bit bus width	D31 to D24	$\overline{WR0}$	$\overline{WR0}$	D23 to D16	$\overline{WR1}$	(Usable as port)
	16-bit bus width	8-bit bus width										
D31 to D24	$\overline{WR0}$	$\overline{WR0}$										
D23 to D16	$\overline{WR1}$	(Usable as port)										
85 86 87 88 89 90 91 92	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	C	External data bus bits 16 to 23. These pins can be used as ports (P20 to P27) when the external bus width has been set to 8 bits.									

(Continued)

MB91121

(Continued)

Pin no.	Pin name	Circuit type	Function
93 94 95 96 97 98 99 100	D24 D25 D26 D27 D28 D29 D30 D31	C	External data bus bits 24 to 31.
102 103 104 105 106 107 108 109 111 112 113 114 115 116 117 118	A00 A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13 A14 A15	F	External address bus bits 00 to 15.
120	A16/P60		External address bus bit 16. This pin can serve as a port (P60) when not used as the address bus.
24 55 64 110	V _{CC}	—	Power supply pin for digital circuit.
34 52 75 101 119	V _{SS}	—	Earth level for digital circuit.

Note : In most of the above pins, I/O port and resource I/O are multiplexed xxxx/Pxx. In case of conflict between output of I/O port and resource I/O, priority is always given to the output of resource I/O.

■ DRAM CONTROL PIN

Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode	—	
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of “L” “H” to lower address 1 bit (A0) in data bus 16-bit mode “L” : “0” “H” : “1” CASL : CAS which A0 corresponds to “0” area CASH : CAS which A0 corresponds to “1” area WEL : \overline{WE} which A0 corresponds to “0” area WEH : \overline{WE} which A0 corresponds to “1” area
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	
CS0H	Area 4 CASH	Area 4 \overline{WEL}	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	
CS1H	Area 5 CASH	Area 5 \overline{WEL}	Area 5 CAS	
$\overline{DW0}$	Area 4 \overline{WE}	Area 4 \overline{WEH}	Area 4 \overline{WE}	
$\overline{DW1}$	Area 5 \overline{WE}	Area 5 \overline{WEH}	Area 5 \overline{WE}	

■ I/O CIRCUIT TYPE

Circuit Type	Circuit	Remarks
A		<ul style="list-style-type: none"> • Oscillation feedback resistance 1 MΩ approx.
B		<ul style="list-style-type: none"> • CMOS level Hysteresis input Without standby control With pull-up resistance
C		<ul style="list-style-type: none"> • CMOS level I/O With standby control
N		<ul style="list-style-type: none"> • Analog input

(Continued)

(Continued)

Circuit Type	Circuit	Remarks
F		<ul style="list-style-type: none"> • CMOS level output • CMOS level Hysteresis input With standby control
G		<ul style="list-style-type: none"> • CMOS level input Without standby control
H		<ul style="list-style-type: none"> • CMOS level Hysteresis input Without standby control
M		<ul style="list-style-type: none"> • CMOS level output

■ HANDLING DEVICES

• Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

Take care that the analog power supply (AV_{CC} AVR) and the analog input do not exceed the digital power supply (V_{CC}) when the analog power supply turned on or off.

• Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

• External Reset Input

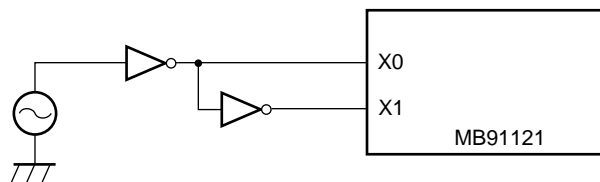
It takes at least 5 machine cycle to input "L" level to the \overline{RST} pin and to ensure inner reset operation properly.

• Remarks for External Clock Operation

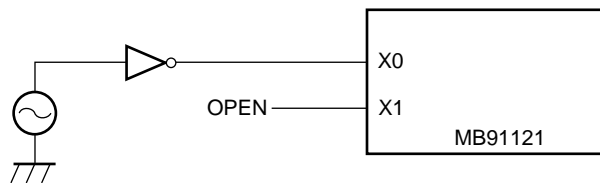
When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at "H" output in stop mode) .

And can be used to supply only to X0 pin with 5 V power supply at 12.5 MHz and less than.

• Using an external clock



Using an external clock (normal)
Note: Can not be used stop mode (oscillation stop mode).



Using an external clock (can be used at 12.5 MHz and less than.)

• Power Supply Pins

When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.

It is preferred to connect V_{CC} and V_{SS} of MB91121 to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} at a position as close as possible to MB91121.

- **Crystal Oscillator Circuit**

Noises around X0 and X1 pins may cause malfunctions of MB91121. In designing the PC board, layout X0, X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

- **Treatment of N.C. Pins**

Make sure to leave N.C. pins open.

- **Mode Setting Pins (MD0 to MD3)**

Connect mode setting pins (MD0 to MD3) directly to V_{CC} or V_{SS} .

Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

- **Turning on the Power Supply**

When turning on the power supply, never fail to start from setting the \overline{RST} pin to "L" level. And after the power supply voltage goes to V_{CC} level, at least after ensuring the time for 5 machine cycle, then set to "H" level.

- **Pin Condition at Turning on the Power Supply**

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation becomes stable.

- **Source Oscillation Input at Turning on the Power Supply**

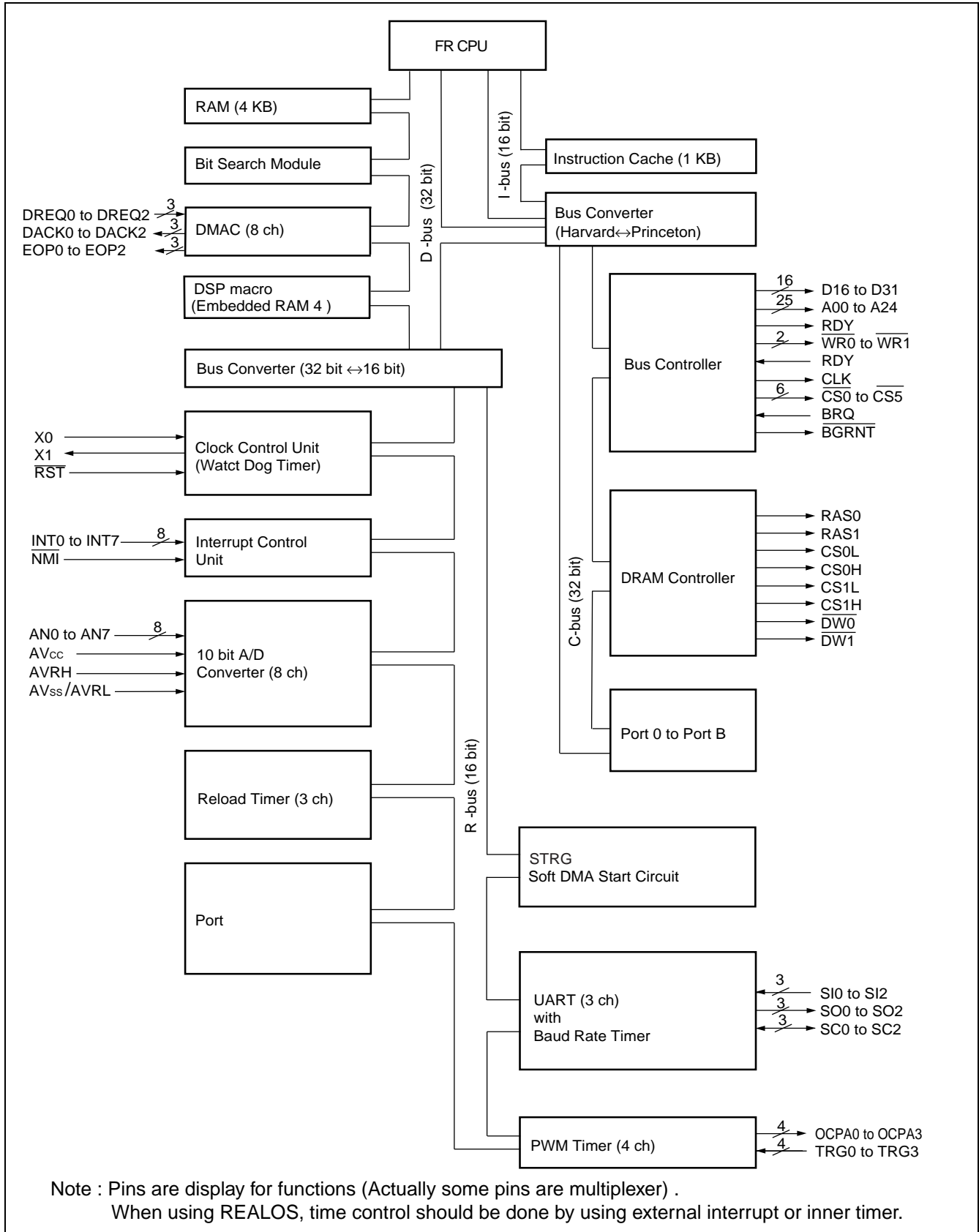
At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

- The device contains registers which are initialized only at a power-on reset. When it is expected to initialize them, recycle the power to execute a power-on reset.
- Even when the A/D converter is not used, make the connections : $AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$.

- **Caution on operations during PLL clock mode**

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

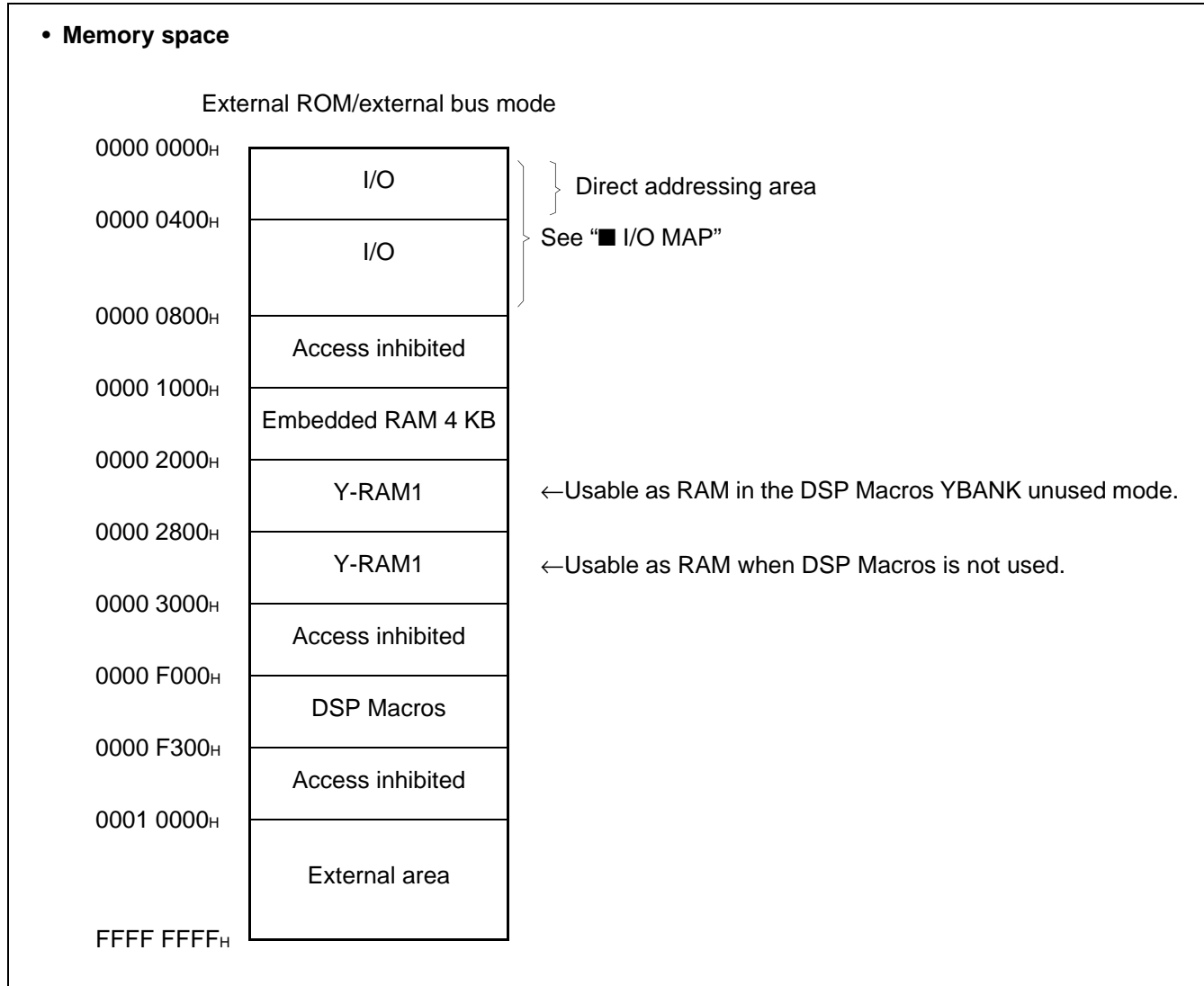
■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.



• Direct addressing area

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consist of the following areas dependent on accessible data sizes.

Byte data access : 000_H to 0FF_H

Half word data access : 000_H to 1FF_H

Word data access : 000_H to 3FF_H

2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

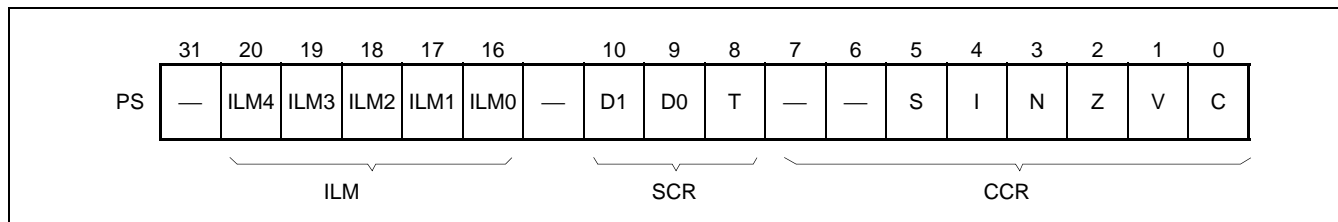
• Dedicated registers

- Program counter (PC) : 32-bit length, indicates the location of the instruction to be executed.
- Program status (PS) : 32-bit length, register for storing register pointer or condition codes
- Table base register (TBR) : Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
- Return pointer (RP) : Holds address to resume operation after returning from a subroutine.
- System stack pointer (SSP) : Indicates system stack space.
- User's stack pointer (USP) : Indicates user's stack space.
- Multiplication/division result register (MDH/MDL) : 32-bit length, register for multiplication/division

Register Name	Description	Initial value
PC	Program counter	XXXX XXXXH Indeterminate
PS	Program status	
TBR	Table base register	000F FC00H
RP	Return pointer	XXXX XXXXH Indeterminate
SSP	System stack pointer	0000 0000H
USP	User's stack pointer	XXXX XXXXH Indeterminate
MDH	Multiplication/division result register	XXXX XXXXH Indeterminate
MDL		XXXX XXXXH Indeterminate

• Program status (PS)

The PS register is for holding program status and consists of a condition code register (CCR) , a system condition code register (SCR) and a interrupt level mask register (ILM) .



- **Condition code register (CCR)**

S-flag : Specifies a stack pointer used as R15.

I-flag : Controls user interrupt request enable/disable.

N-flag : Indicates sign bit when division result is assumed to be in the 2's complement format.

Z-flag : Indicates whether or not the result of division was "0".

V-flag : Assumes the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.

C-flag : Indicates if a carry or borrow from the MSB has occurred.

- **System condition code register (SCR)**

T-flag : Specifies whether or not to enable step trace trap.

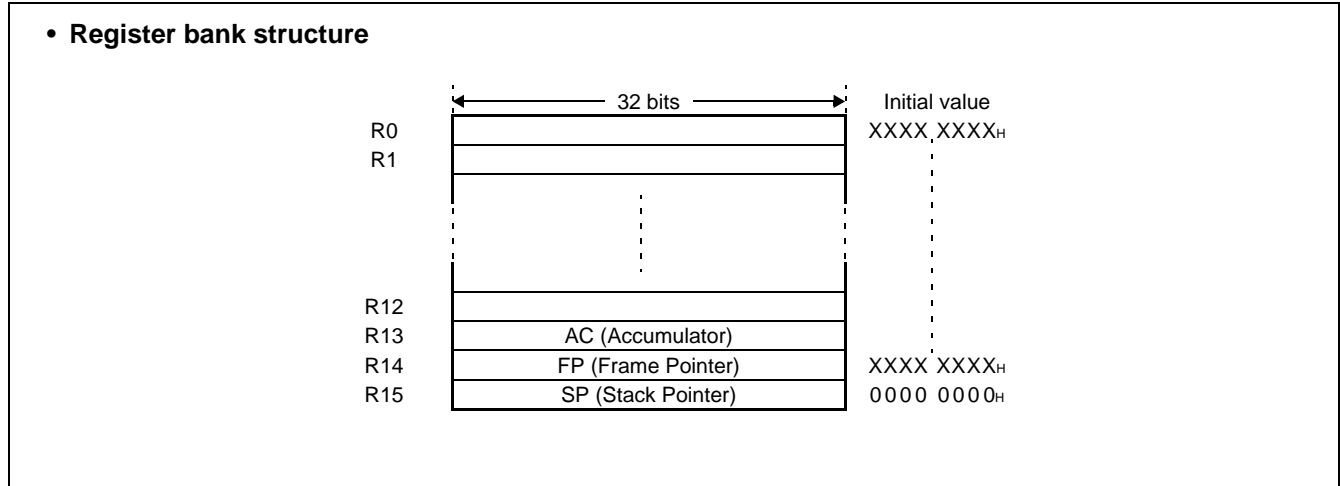
- **Interrupt level mask register (ILM)**

ILM4 to ILM0 : Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High ↑ ↓ Low
:					:	
0	1	0	0	0	15	
:					:	
1	1	1	1	1	31	

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address) .



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

- R13 : Virtual accumulator (AC)
- R14 : Frame pointer (FP)
- R15 : Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000_H (SSP value) .

■ SETTING MODE

1. Pin

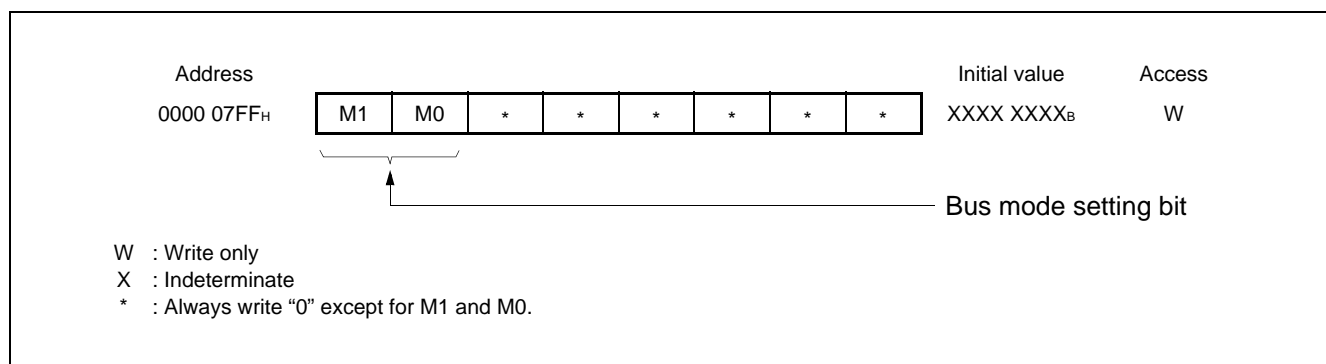
• Mode setting pins and modes

Mode setting pins				Mode name	Reset vector access area	External data bus width	Bus mode
MD3	MD2	MD1	MD0				
1	0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
1	0	0	1	External vector mode 1	External	16 bits	
1	0	1	0	—	—	—	Inhibited
1	0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	1	—	—	—	—	—	Inhibited
0	—	—	—	—	—	—	Inhibited

* : MB91121 does not support single-chip mode.

2. Registers

• Mode setting registers (MODR) and modes



• Bus mode setting bits and functions

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	
1	0	External ROM/external bus mode	
1	1	—	Inhibited

Note : Because of without internal ROM, MB91121 allows "10_B" setting value only.

MB91121

■ I/O MAP

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0000 _H	(Vacancy)			
0001 _H	PDR2	Port 2 data register	R/W	XXXXXXXX _B
0002 _H to 0004 _H	(Vacancy)			
0005 _H	PDR6	Port 6 data register	R/W	XXXXXXXX _B
0006 _H 0007 _H	(Vacancy)			
0008 _H	PDRB	Port B data register	R/W	XXXXXXXX _B
0009 _H	PDRA	Port A data register	R/W	-XXXXXX- _B
000A _H	(Vacancy)			
000B _H	PDR8	Port 8 data register	R/W	--X--XX _B
000C _H to 0011 _H	(Vacancy)			
0012 _H	PDRE	Port E data register	R/W	XXXXXXXX _B
0013 _H	PDRF	Port F data register	R/W	XXXXXXXX _B
0014 _H	PDRG	Port G data register	R/W	XXXXXXXX _B
0015 _H	PDRH	Port H data register	R/W	XXXX---- _B
0016 _H	PDRI	Port I data register	R/W	-----XX _B
0017 _H to 001B _H	(Vacancy)			
001C _H	SSR0	Serial status register 0	R/W	00001-00 _B
001D _H	SIDR0/SODR0	Serial input register 0/serial output register 0	R/W	XXXXXXXX _B
001E _H	SCR0	Serial control register 0	R/W	00000100 _B
001F _H	SMR0	Serial mode register 0	R/W	00--0-00 _B
0020 _H	SSR1	Serial status register 1	R/W	00001-00 _B
0021 _H	SIDR1/SODR1	Serial input register 1/serial output register 1	R/W	XXXXXXXX _B
0022 _H	SCR1	Serial control register 1	R/W	00000100 _B
0023 _H	SMR1	Serial mode register 1	R/W	00--0-00 _B
0024 _H	SSR2	Serial status register 2	R/W	00001-00 _B
0025 _H	SIDR2/SODR2	Serial input register 2/serial output register 2	R/W	XXXXXXXX _B
0026 _H	SCR2	Serial control register 2	R/W	00000100 _B
0027 _H	SMR2	Serial mode register 2	R/W	00--0-00 _B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0028 _H	TMRLR0	16-bit reload register ch. 0	W	XXXXXXXX _B
0029 _H				XXXXXXXX _B
002A _H	TMR0	16-bit timer register ch. 0	R	XXXXXXXX _B
002B _H				XXXXXXXX _B
002C _H	(Vacancy)			
002D _H	(Vacancy)			
002E _H	TMCSR0	16-bit reload timer control status register ch. 0	R/W	----0000 _B
002F _H				00000000 _B
0030 _H	TMRLR1	16-bit reload register ch. 1	W	XXXXXXXX _B
0031 _H				XXXXXXXX _B
0032 _H	TMR1	16-bit timer register ch. 1	R	XXXXXXXX _B
0033 _H				XXXXXXXX _B
0034 _H	(Vacancy)			
0035 _H	(Vacancy)			
0036 _H	TMCSR1	16-bit reload timer control status register ch. 1	R/W	----0000 _B
0037 _H				00000000 _B
0038 _H	ADCR	A/D converter data register	R	-----XX _B
0039 _H				XXXXXXXX _B
003A _H	ADCS	A/D converter control status register	R/W	00000000 _B
003B _H				00000000 _B
003C _H	TMRLR2	16-bit reload register ch. 2	W	XXXXXXXX _B
003D _H				XXXXXXXX _B
003E _H	TMR2	16-bit timer register ch. 2	R	XXXXXXXX _B
003F _H				XXXXXXXX _B
0040 _H	(Vacancy)			
0041 _H	(Vacancy)			
0042 _H	TMCSR2	16-bit reload timer control status register ch. 2	R/W	----0000 _B
0043 _H				00000000 _B
0044 _H to 004F _H	(Vacancy)			
0050 _H	STRG	Soft DMA Start	R/W	-----00 _B
0051 _H to 0077 _H	(Vacancy)			

(Continued)

MB91121

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0078 _H	UTIM0/UTIMR0	U-TIMER register ch. 0/reload register ch. 0	R/W	00000000 _B
0079 _H				00000000 _B
007A _H	(Vacancy)			
007B _H	UTIMC0	U-TIMER control register ch. 0	R/W	0--00001 _B
007C _H	UTIM1/UTIMR1	U-TIMER register ch. 1/reload register ch. 1	R/W	00000000 _B
007D _H				00000000 _B
007E _H	(Vacancy)			
007F _H	UTIMC1	U-TIMER control register ch. 1	R/W	0--00001 _B
0080 _H	UTIM2/UTIMR2	U-TIMER register ch. 2/reload register ch. 2	R/W	00000000 _B
0081 _H				00000000 _B
0082 _H	(Vacancy)			
0083 _H	UTIMC2	U-TIMER control register ch. 2	R/W	0--00001 _B
0084 _H to 0093 _H	(Vacancy)			
0094 _H	EIRR	External interrupt cause register	R/W	00000000 _B
0095 _H	ENIR	Interrupt enable register	R/W	00000000 _B
0096 _H to 0097 _H	(Vacancy)			
0098 _H	ELVR	External interrupt request level setting register		
0099 _H			R/W	00000000 _B
009A _H to 00D1 _H	(Vacancy)			
00D2 _H	DDRE	Port E data direction register	W	00000000 _B
00D3 _H	DDRF	Port F data direction register	W	00000000 _B
00D4 _H	DDRG	Port G data direction register	W	00000000 _B
00D5 _H	DDRH	Port H data direction register	W	0000---- _B
00D6 _H	DDRI	Port I data direction register	W	-----0 _B
00D7 _H to 00DB _H	(Vacancy)			
00DC _H	GCN1	General control register 1	R/W	00110010 _B
00DD _H				00010000 _B
00DE _H	(Vacancy)			
00DF _H	GCN2	General control register 2	R/W	00000000 _B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
00E0 _H	PTMR0	PWM timer register	R	11111111 _B
00E1 _H				11111111 _B
00E2 _H	PCSR0	PWM cycle setting register	W	XXXXXXXX _B
00E3 _H				XXXXXXXX _B
00E4 _H	PDUT0	PWM duty setting register	W	XXXXXXXX _B
00E5 _H				XXXXXXXX _B
00E6 _H	PCNH0	PWM control status register H	R/W	0000000- _B
00E7 _H	PCNL0	PWM control status register L	R/W	00000000 _B
00E8 _H	PTMR1	PWM timer register	R	11111111 _B
00E9 _H				11111111 _B
00EA _H	PCSR1	PWM cycle setting register	W	XXXXXXXX _B
00EB _H				XXXXXXXX _B
00EC _H	PDUT1	PWM duty setting register	W	XXXXXXXX _B
00ED _H				XXXXXXXX _B
00EE _H	PCNH1	PWM control status register H	R/W	0000000- _B
00EF _H	PCNL1	PWM control status register L	R/W	00000000 _B
00F0 _H	PTMR2	PWM timer register	R	11111111 _B
00F1 _H				11111111 _B
00F2 _H	PCSR2	PWM cycle setting register	W	XXXXXXXX _B
00F3 _H				XXXXXXXX _B
00F4 _H	PDUT2	PWM duty setting register	W	XXXXXXXX _B
00F5 _H				XXXXXXXX _B
00F6 _H	PCNH2	PWM control status register H	R/W	0000000- _B
00F7 _H	PCNL2	PWM control status register L	R/W	00000000 _B
00F8 _H	PTMR3	PWM timer register	R	11111111 _B
00F9 _H				11111111 _B
00FA _H	PCSR3	PWM cycle setting register	W	XXXXXXXX _B
00FB _H				XXXXXXXX _B
00FC _H	PDUT3	PWM duty setting register	W	XXXXXXXX _B
00FD _H				XXXXXXXX _B
00FE _H	PCNH3	PWM control status register H	R/W	0000000- _B
00FF _H	PCNL3	PWM control status register L	R/W	00000000 _B
0100 _H to 01FF _H	(Vacancy)			

(Continued)

MB91121

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0200 _H	DPDP	DMAC parameter descriptor pointer	R/W	XXXXXXXX _B
0201 _H				XXXXXXXX _B
0202 _H				XXXXXXXX _B
0203 _H				X0000000 _B
0204 _H	DACSR	DMAC control status register	R/W	00000000 _B
0205 _H				00000000 _B
0206 _H				00000000 _B
0207 _H				00000000 _B
0208 _H	DATCR	DMAC pin control register	R/W	XXXXXXXX _B
0209 _H				XXXX0000 _B
020A _H				XXXX0000 _B
020B _H				XXXX0000 _B
020C _H to 020F _H	(Vacancy)			
0210 _H	OFAS	DSP macro register	R/W	----0000 _B
0211 _H				00000000 _B
0212 _H	STRS			----0000 _B
0213 _H				00000000 _B
0214 _H	OFSC	0000---0 _B		
0215 _H	(Vacancy)			
0216 _H	OFSS	DSP macro register	R/W	00000000 _B
0217 _H	Y-BANKC		R/W	0--0000 _B
0218 _H	OFSD		R/W	00000000 _B
0219 _H				00000000 _B
021A _H	DSP-PC		R/W	XXXXXXXX _B
021B _H	DSP-CSR		R/W	00000000 _B
021C _H	DSP-LY		R/W	XXXXXXXX _B
021D _H				XXXXXXXX _B
021E _H	DSP-OT0		R	XXXXXXXX _B
021F _H				XXXXXXXX _B
0220 _H	DSP-OT1		R	XXXXXXXX _B
0221 _H				XXXXXXXX _B
0222 _H	DSP-OT2		R	XXXXXXXX _B
0223 _H				XXXXXXXX _B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0224 _H	DSP-OT3	DSP macro register	R	XXXXXXXX _B
0225 _H				XXXXXXXX _B
0226 _H to 03E3 _H	(Vacancy)			
03E4 _H	ICHCR	Instruction cache control register	R/W	----- _B
03E5 _H				----- _B
03E6 _H				----- _B
03E7 _H				--00000 _B
03E8 _H to 03EF _H	(Vacancy)			
03F0 _H	BSD0	Bit search module 0-detection data register	W	XXXXXXXX _B
03F1 _H				XXXXXXXX _B
03F2 _H				XXXXXXXX _B
03F3 _H				XXXXXXXX _B
03F4 _H	BSD1	Bit search module 1-detection data register	R/W	XXXXXXXX _B
03F5 _H				XXXXXXXX _B
03F6 _H				XXXXXXXX _B
03F7 _H				XXXXXXXX _B
03F8 _H	BSDC	Bit search module transition-detection data register	W	XXXXXXXX _B
03F9 _H				XXXXXXXX _B
03FA _H				XXXXXXXX _B
03FB _H				XXXXXXXX _B
03FC _H	BSRR	Bit search module detection result register	R	XXXXXXXX _B
03FD _H				XXXXXXXX _B
03FE _H				XXXXXXXX _B
03FF _H				XXXXXXXX _B
0400 _H	ICR00	Interrupt control register 0	R/W	---1111 _B
0401 _H	ICR01	Interrupt control register 1	R/W	---1111 _B
0402 _H	ICR02	Interrupt control register 2	R/W	---1111 _B
0403 _H	ICR03	Interrupt control register 3	R/W	---1111 _B
0404 _H	ICR04	Interrupt control register 4	R/W	---1111 _B
0405 _H	ICR05	Interrupt control register 5	R/W	---1111 _B
0406 _H	ICR06	Interrupt control register 6	R/W	---1111 _B
0407 _H	ICR07	Interrupt control register 7	R/W	---1111 _B

(Continued)

MB91121

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0408 _H	ICR08	Interrupt control register 8	R/W	---11111 _B
0409 _H	ICR09	Interrupt control register 9	R/W	---11111 _B
040A _H	ICR10	Interrupt control register 10	R/W	---11111 _B
040B _H	ICR11	Interrupt control register 11	R/W	---11111 _B
040C _H	ICR12	Interrupt control register 12	R/W	---11111 _B
040D _H	ICR13	Interrupt control register 13	R/W	---11111 _B
040E _H	ICR14	Interrupt control register 14	R/W	---11111 _B
040F _H	ICR15	Interrupt control register 15	R/W	---11111 _B
0410 _H	ICR16	Interrupt control register 16	R/W	---11111 _B
0411 _H	ICR17	Interrupt control register 17	R/W	---11111 _B
0412 _H	ICR18	Interrupt control register 18	R/W	---11111 _B
0413 _H	ICR19	Interrupt control register 19	R/W	---11111 _B
0414 _H	ICR20	Interrupt control register 20	R/W	---11111 _B
0415 _H	ICR21	Interrupt control register 21	R/W	---11111 _B
0416 _H	ICR22	Interrupt control register 22	R/W	---11111 _B
0417 _H	ICR23	Interrupt control register 23	R/W	---11111 _B
0418 _H	ICR24	Interrupt control register 24	R/W	---11111 _B
0419 _H	ICR25	Interrupt control register 25	R/W	---11111 _B
041A _H	ICR26	Interrupt control register 26	R/W	---11111 _B
041B _H	ICR27	Interrupt control register 27	R/W	---11111 _B
041C _H	ICR28	Interrupt control register 28	R/W	---11111 _B
041D _H	ICR29	Interrupt control register 29	R/W	---11111 _B
041E _H	ICR30	Interrupt control register 30	R/W	---11111 _B
041F _H	ICR31	Interrupt control register 31	R/W	---11111 _B
0420 _H to 042E _H	ICR32 to ICR46	Interrupt control register 32 to 46	R/W	---11111 _B
042F _H	ICR47	Interrupt control register 47	R/W	---11111 _B
0430 _H	DICR	Delayed interrupt control register	R/W	-----0 _B
0431 _H	HRCL	Hold request cancel request level setting register	R/W	---11111 _B
0432 _H to 047F _H	(Vacancy)			
0480 _H	RSRR/WTCR	Reset cause register/ watchdog peripheral control register	R/W	1XXXX-00 _B
0481 _H	STCR	Standby control register	R/W	000111-- _B
0482 _H	PDRR	DMA controller request squelch register	R/W	----0000 _B

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
0483 _H	CTBR	Timebase timer clear register	W	XXXXXXXX _B
0484 _H	GCR	Gear control register	R/W	110011-1 _B
0485 _H	WPR	Watchdog reset occurrence postpone register	W	XXXXXXXX _B
0486 _H	(Vacancy)			
0487 _H				
0488 _H	PCTR	PLL control register	R/W	00--0--- _B
0489 _H to 0600 _H	(Vacancy)			
0601 _H	DDR2	Port 2 data direction register	W	00000000 _B
0602 _H to 0604 _H	(Vacancy)			
0605 _H	DDR6	Port 6 data direction register	W	00000000 _B
0606 _H	(Vacancy)			
0607 _H				
0608 _H	DDRB	Port B data direction register	W	00000000 _B
0609 _H	DDRA	Port A data direction register	W	-000000- _B
060A _H	(Vacancy)			
060B _H	DDR8	Port 8 data direction register	W	--0--000 _B
060C _H	ASR1	Area select register 1	W	00000000 _B
060D _H				00000001 _B
060E _H	AMR1	Area mask register 1	W	00000000 _B
060F _H				00000000 _B
0610 _H	ASR2	Area select register 2	W	00000000 _B
0611 _H				00000010 _B
0612 _H	AMR2	Area mask register 2	W	00000000 _B
0613 _H				00000000 _B
0614 _H	ASR3	Area select register 3	W	00000000 _B
0615 _H				00000011 _B
0616 _H	AMR3	Area mask register 3	W	00000000 _B
0617 _H				00000000 _B
0618 _H	ASR4	Area select register 4	W	00000000 _B
0619 _H				00000100 _B
061A _H	AMR4	Area mask register 4	W	00000000 _B
061B _H				00000000 _B

(Continued)

MB91121

(Continued)

Address	Register name (abbreviated)	Register name	Read/write	Initial value
061C _H	ASR5	Area select register 5	W	00000000 _B
061D _H				00000101 _B
061E _H	AMR5	Area mask register 5	W	00000000 _B
061F _H				00000000 _B
0620 _H	AMD0	Area mode register 0	R/W	---00111 _B
0621 _H	AMD1	Area mode register 1	R/W	0--00000 _B
0622 _H	AMD32	Area mode register 32	R/W	00000000 _B
0623 _H	AMD4	Area mode register 4	R/W	0--00000 _B
0624 _H	AMD5	Area mode register 5	R/W	0--00000 _B
0625 _H	DSCR	DRAM signal control register	W	00000000 _B
0626 _H	RFCR	Refresh control register	R/W	--XXXXXX _B
0627 _H				00---000 _B
0628 _H	EPCR0	External pin control register 0	W	----1100 _B
0629 _H				-1111111 _B
062A _H	(Vacancy)			
062B _H	EPCR1	External pin control register 1	W	11111111 _B
062C _H	DMCR4	DRAM control register 4	R/W	00000000 _B
062D _H				0000000- _B
062E _H	DMCR5	DRAM control register 5	R/W	00000000 _B
062F _H				0000000- _B
0630 _H to 07FD _H	(Vacancy)			
07FE _H	LER	Little endian register	W	-----000 _B
07FF _H	MODR	Mode register	W	XXXXXXXX _B
002000 _H to 002FFF _H	Y-RAM (Variable RAM) 4096 byte (Max.)	DSP macro RAM		
00F000 _H to 00F07F _H	X-RAM (Coefficient RAM) 128 byte			
00F100 _H to 00F2FF _H	I-RAM (Instruction RAM) 512 byte			

Note : Do not use (vacancy) .

■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	3F4 _H	000FFFFC _H
Reserved for system	1	01	—	3F8 _H	000FFFF8 _H
Reserved for system	2	02	—	3F4 _H	000FFFF4 _H
Reserved for system	3	03	—	3F0 _H	000FFFF0 _H
Reserved for system	4	04	—	3EC _H	000FFFECh
Reserved for system	5	05	—	3E8 _H	000FFFE8 _H
Reserved for system	6	06	—	3E4 _H	000FFFE4 _H
Reserved for system	7	07	—	3E0 _H	000FFFE0 _H
Reserved for system	8	08	—	3DC _H	000FFFDCh
Reserved for system	9	09	—	3D8 _H	000FFFD8 _H
Reserved for system	10	0A	—	3D4 _H	000FFFD4 _H
Reserved for system	11	0B	—	3D0 _H	000FFFD0 _H
Reserved for system	12	0C	—	3CC _H	000FFFCCh
Reserved for system	13	0D	—	3C8 _H	000FFFC8 _H
Exception for undefined instruction	14	0E	—	3C4 _H	000FFFC4 _H
NMI request	15	0F	F _H fixed	3C0 _H	000FFFC0 _H
External interrupt 0	16	10	ICR00	3BC _H	000FFFBCh
External interrupt 1	17	11	ICR01	3B8 _H	000FFFB8 _H
External interrupt 2	18	12	ICR02	3B4 _H	000FFFB4 _H
External interrupt 3	19	13	ICR03	3B0 _H	000FFFB0 _H
UART0 receive complete	20	14	ICR04	3AC _H	000FFFACh
UART1 receive complete	21	15	ICR05	3A8 _H	000FFFA8 _H
UART2 receive complete	22	16	ICR06	3A4 _H	000FFFA4 _H
UART0 transmit complete	23	17	ICR07	3A0 _H	000FFFA0 _H
UART1 transmit complete	24	18	ICR08	39C _H	000FFF9Ch
UART2 transmit complete	25	19	ICR09	398 _H	000FFF98 _H
DMAC0 (complete, error)	26	1A	ICR10	394 _H	000FFF94 _H
DMAC1 (complete, error)	27	1B	ICR11	390 _H	000FFF90 _H
DMAC2 (complete, error)	28	1C	ICR12	38C _H	000FFF8Ch
DMAC3 (complete, error)	29	1D	ICR13	388 _H	000FFF88 _H
DMAC4 (complete, error)	30	1E	ICR14	384 _H	000FFF84 _H
DMAC5 (complete, error)	31	1F	ICR15	380 _H	000FFF80 _H
DMAC6 (complete, error)	32	20	ICR16	37C _H	000FFF7Ch

(Continued)

MB91121

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
DMAC7 (complete, error)	33	21	ICR17	378 _H	000FFF78 _H
A/D converter (successive approximation conversion type)	34	22	ICR18	374 _H	000FFF74 _H
16-bit reload timer 0	35	23	ICR19	370 _H	000FFF70 _H
16-bit reload timer 1	36	24	ICR20	36C _H	000FFF6C _H
16-bit reload timer 2	37	25	ICR21	368 _H	000FFF68 _H
PWM 0	38	26	ICR22	364 _H	000FFF64 _H
PWM 1	39	27	ICR23	360 _H	000FFF60 _H
PWM 2	40	28	ICR24	35C _H	000FFF5C _H
PWM 3	41	29	ICR25	358 _H	000FFF58 _H
U-TIMER 0	42	2A	ICR26	354 _H	000FFF54 _H
U-TIMER 1	43	2B	ICR27	350 _H	000FFF50 _H
U-TIMER 2	44	2C	ICR28	34C _H	000FFF4C _H
External interrupt 4	45	2D	ICR29	348 _H	000FFF48 _H
External interrupt 5	46	2E	ICR30	344 _H	000FFF44 _H
External interrupt 6	47	2F	ICR31	340 _H	000FFF40 _H
External interrupt 7	48	30	ICR32	33C _H	000FFF3C _H
DSP Macros soft interrupt	49	31	ICR33	338 _H	000FFF38 _H
DSP Macros offset interrupt	50	32	ICR34	334 _H	000FFF34 _H
Reserved for system	51	33	ICR35	330 _H	000FFF30 _H
Reserved for system	52	34	ICR36	32C _H	000FFF2C _H
Reserved for system	53	35	ICR37	328 _H	000FFF28 _H
Reserved for system	54	36	ICR38	324 _H	000FFF24 _H
Reserved for system	55	37	ICR39	320 _H	000FFF20 _H
Reserved for system	56	38	ICR40	31C _H	000FFF1C _H
Reserved for system	57	39	ICR41	318 _H	000FFF18 _H
Reserved for system	58	3A	ICR42	314 _H	000FFF14 _H
Reserved for system	59	3B	ICR43	310 _H	000FFF10 _H
Reserved for system	60	3C	ICR44	30C _H	000FFF0C _H
Reserved for system	61	3D	ICR45	308 _H	000FFF08 _H
Reserved for system	62	3E	ICR46	304 _H	000FFF04 _H
Delayed interrupt cause bit	63	3F	ICR47	300 _H	000FFF00 _H
Reserved for system (used in REALOS*)	64	40	—	2FC _H	000FFEFC _H
Reserved for system (used in REALOS*)	65	41	—	2F8 _H	000FEF8 _H

(Continued)

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Used in INT instructions	66 to 255	42 to FF	—	2F4 _H to 000 _H	000FFE4 _H to 000FFC0 _H

* : When using in REALOS/FR, interrupt 0x40, 0x41 for system code.

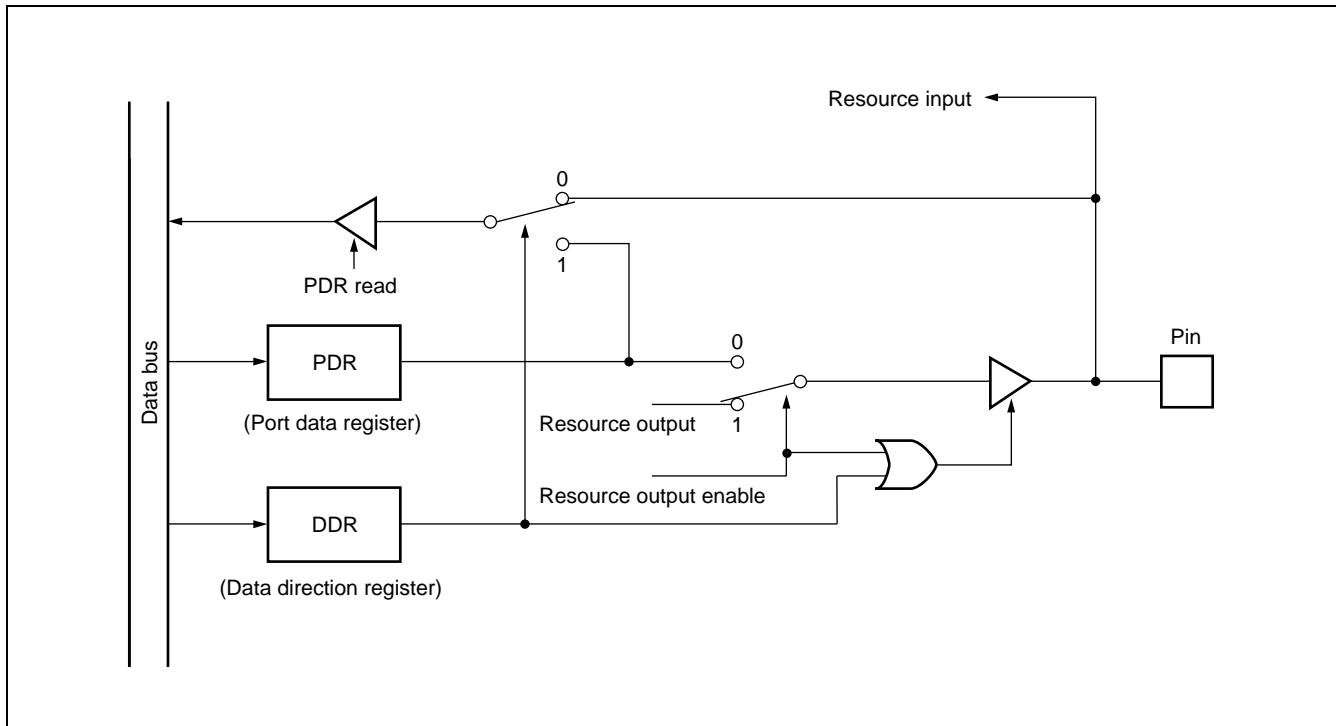
■ PERIPHERAL RESOURCES

1. I/O Ports

There are 2 types of I/O port register structure; port data register (PDR2, 6, 8, A, B, E to I) and data direction register (DDR2, 6, 8, A, B, E to I), where bits PDR2, 6, 8, A, B, E to I and bits DDR2, 6, 8, A, B, E to I corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit "0" specifies input and "1" specifies output.

- For input (DDR = "0") setting;
PDR reading operation : reads level of corresponding external pin.
PDR writing operation : writes set value to PDR.
- For output (DDR = "1") setting;
PDR reading operation : reads PDR value.
PDR writing operation : outputs PDR value to corresponding external pin.

• Block diagram



- Register explanation

- Port Data Register (PDR)

PDR2 Address: 000001 _H	7	6	5	4	3	2	1	0	Initial value XXXXXXXX _B	Access R/W
	P27	P26	P25	P24	P23	P22	P21	P20		
PDR6 Address: 000005 _H	7	6	5	4	3	2	1	0	Initial value XXXXXXXX _B	Access R/W
	P67	P66	P65	P64	P63	P62	P61	P60		
PDR8 Address: 00000B _H	7	6	5	4	3	2	1	0	Initial value --X--XX _B	Access R/W
	—	—	P85	—	—	P82	P81	P80		
PDRA Address: 000009 _H	7	6	5	4	3	2	1	0	Initial value -XXXXXX- _B	Access R/W
	—	PA6	PA5	PA4	PA3	PA2	PA1	—		
PDRB Address: 000008 _H	7	6	5	4	3	2	1	0	Initial value XXXXXXXX _B	Access R/W
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0		
PDRE Address: 000012 _H	7	6	5	4	3	2	1	0	Initial value XXXXXXXX _B	Access R/W
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
PDRF Address: 000013 _H	7	6	5	4	3	2	1	0	Initial value XXXXXXXX _B	Access R/W
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		
PDRG Address: 000014 _H	7	6	5	4	3	2	1	0	Initial value XXXXXXXX _B	Access R/W
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0		
PDRH Address: 000015 _H	7	6	5	4	3	2	1	0	Initial value XXX---- _B	Access R/W
	PH7	PH6	PH5	PH4	—	—	—	—		
PDRI Address: 000016 _H	7	6	5	4	3	2	1	0	Initial value -----X _B	Access R/W
	—	—	—	—	—	—	PI1	PI0		

PDR2 to PDRI is the I/O port input/output data register.
The associated register, DDR2 to DDRI, controls the input/output.

• Data Direction Register (DDR)

DDR2 Address: 000601 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 0 0 0 _B	Access W
	P27	P26	P25	P24	P23	P22	P21	P20		
DDR6 Address: 000605 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 0 0 0 _B	Access W
	P67	P66	P65	P64	P63	P62	P61	P60		
DDR8 Address: 00060B _H	7	6	5	4	3	2	1	0	Initial value --0--00 _B	Access W
	—	—	P85	—	—	P82	P81	P80		
DDRA Address: 000609 _H	7	6	5	4	3	2	1	0	Initial value -00000- _B	Access W
	—	PA6	PA5	PA4	PA3	PA2	PA1	—		
DDRB Address: 000608 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 0 0 0 _B	Access W
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0		
DDRE Address: 0000D2 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 0 0 0 _B	Access W
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0		
DDRF Address: 0000D3 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 0 0 0 _B	Access W
	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0		
DDRG Address: 0000D4 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 0 0 0 _B	Access W
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0		
DDRH Address: 0000D5 _H	7	6	5	4	3	2	1	0	Initial value 0 0 0 0 ---- _B	Access W
	PH7	PH6	PH5	PH4	—	—	—	—		
DDRI Address: 0000D6 _H	7	6	5	4	3	2	1	0	Initial value -----0 _B	Access W
	—	—	—	—	—	—	PI1	PI0		

DDR2 to DDRI controls the I/O port input/output direction bit by bit.

- 0 : Input
- 1 : Output

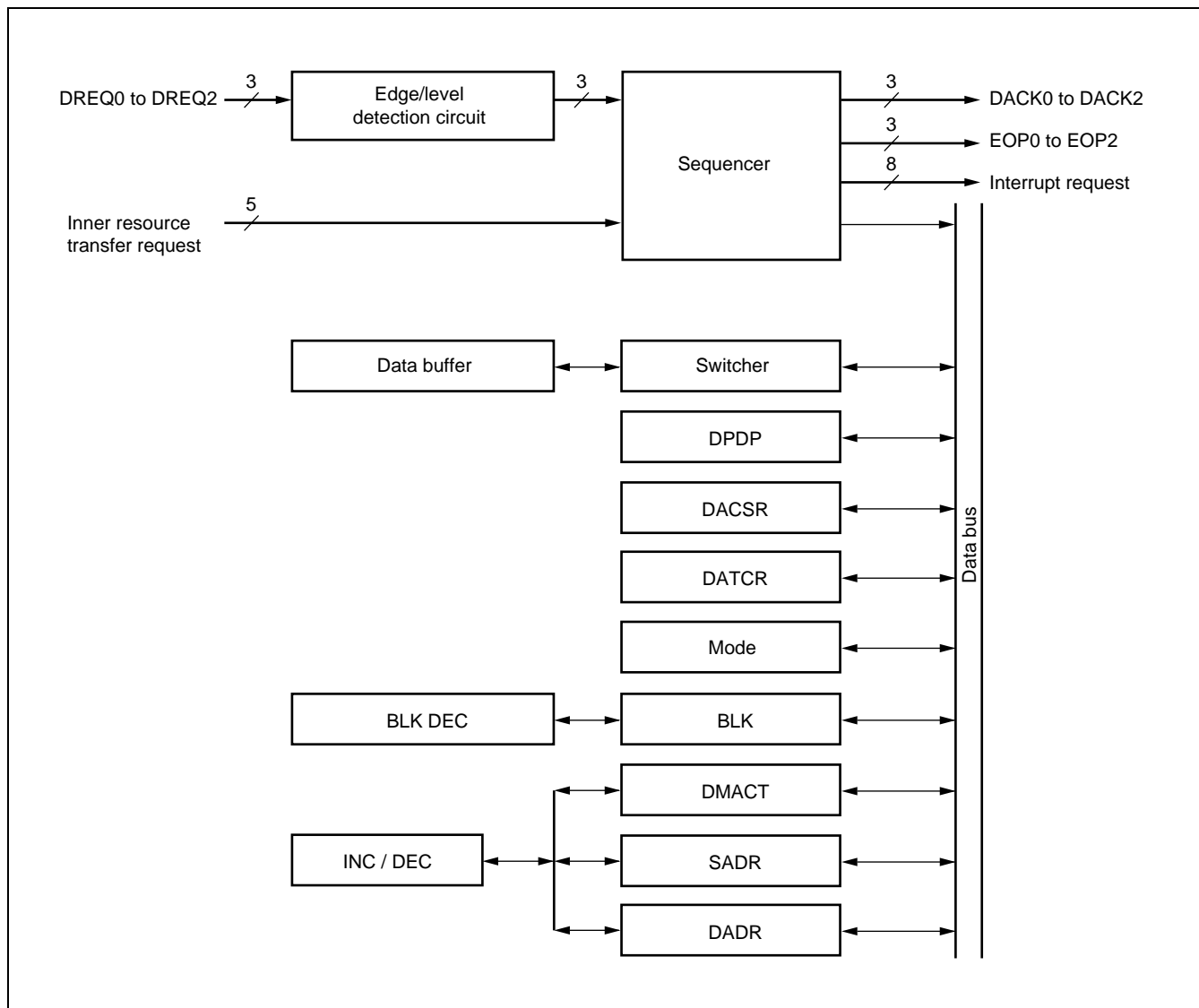
2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

- 8 channels
- Mode : single/block transfer, burst transfer and continuous transfer : 3 kinds of transfer
- Transfer all through the area
- Max. 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

• Block diagram



• Registers (DMAC internal registers)

Address	bit 31	bit 16	bit 0	Initial value	
00000200H	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">DPDP</div> ⋮			XXXXXXXXXB	(R/W)
00000201H				XXXXXXXXXB	
00000202H				XXXXXXXXXB	
00000203H				X0000000B	
00000204H	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">DACSR</div> ⋮			00000000B	(R/W)
00000205H				00000000B	
00000206H				00000000B	
00000207H				00000000B	
00000208H	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;">DATCR</div> ⋮			XXXXXXXXXB	(R/W)
00000209H				XXXX0000B	
0000020AH				XXXX0000B	
0000020BH				XXXX0000B	

() : Access
 R/W : Readable and writable
 X : Indeterminate

• Registers (DMA descriptor)

Address	bit 31	bit 0	
DPDP + 0H	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> ----- ----- ----- </div>		DMA ch.0 Descriptor
DPDP + 0CH			DMA ch.1 Descriptor
⋮			
DPDP + 54H	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> ----- ----- ----- </div>		DMA ch.7 Descriptor

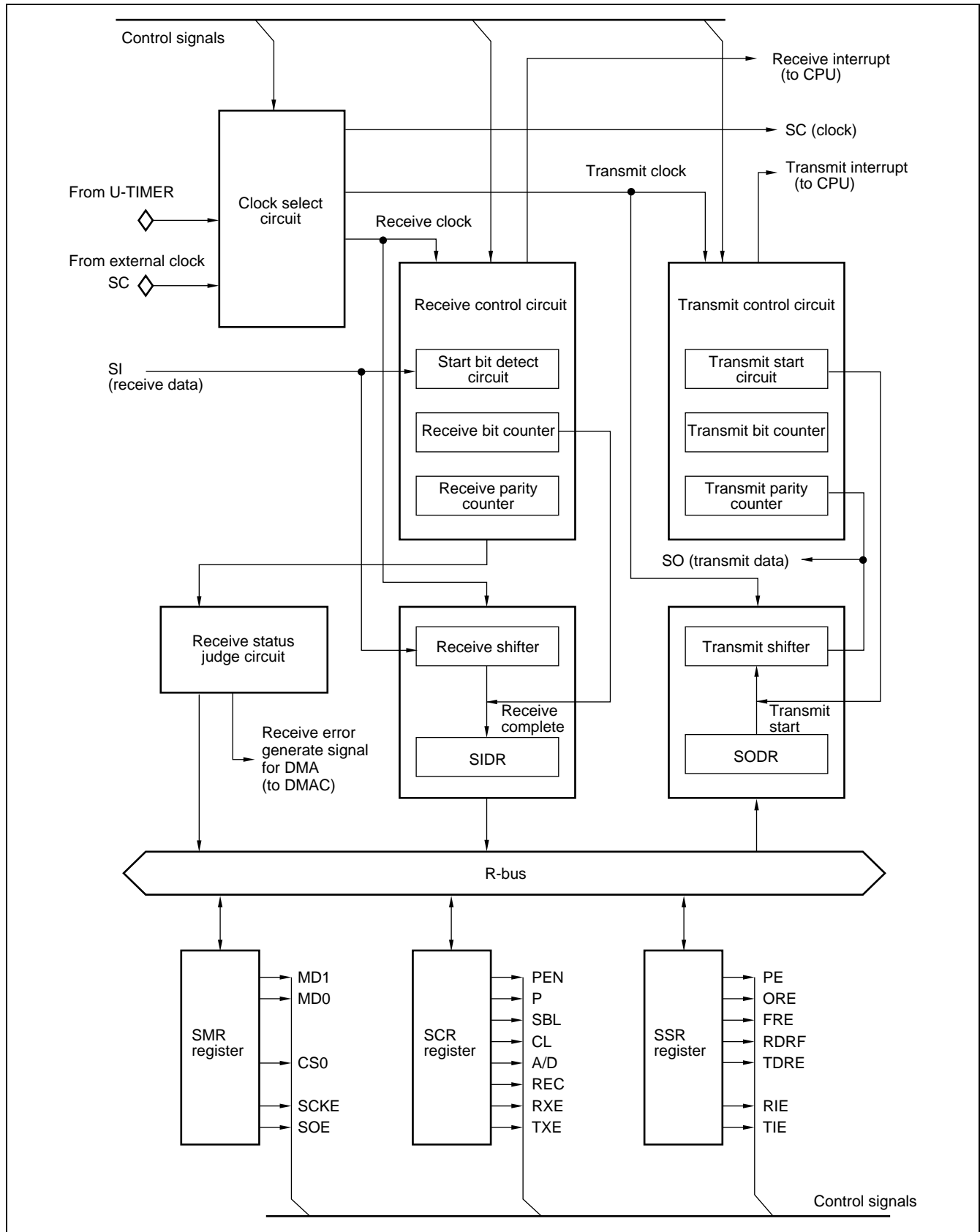
3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication, and it has the following features.

The MB91121 consists of 3 channels of UART.

- Full double double buffer
- Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
- Supporting multi-processor mode
- Perfect programmable baud rate
 - Any baud rate can be set by internal timer (refer to section “4. U-TIMER”).
- Any baud rate can be set by external clock.
- Error checking function (parity, framing and overrun)
- Transfer signal : NRZ code
- Enable DMA transfer start by interrupt.

• Block diagram



• Register configuration

Address	bit 15	bit 8	bit 0	Initial value
0000001E _H	SCR0			00000100 _B (R/W)
00000022 _H	SCR1			00000100 _B (R/W)
00000026 _H	SCR2			00000100 _B (R/W)
0000001F _H		SMR0		00--0-00 _B (R/W)
00000023 _H		SMR1		00--0-00 _B (R/W)
00000027 _H		SMR2		00--0-00 _B (R/W)
0000001C _H	SSR0			00001-00 _B (R/W)
00000020 _H	SSR1			00001-00 _B (R/W)
00000024 _H	SSR2			00001-00 _B (R/W)
0000001D _H		SIDR0/SODR0		XXXXXXXX _B (R/W)
00000021 _H		SIDR1/SIDR1		XXXXXXXX _B (R/W)
00000002 _H		SIDR2/SIDR2		XXXXXXXX _B (R/W)

() : Access
 R/W : Readable and writable
 — : Unused
 X : Indeterminate

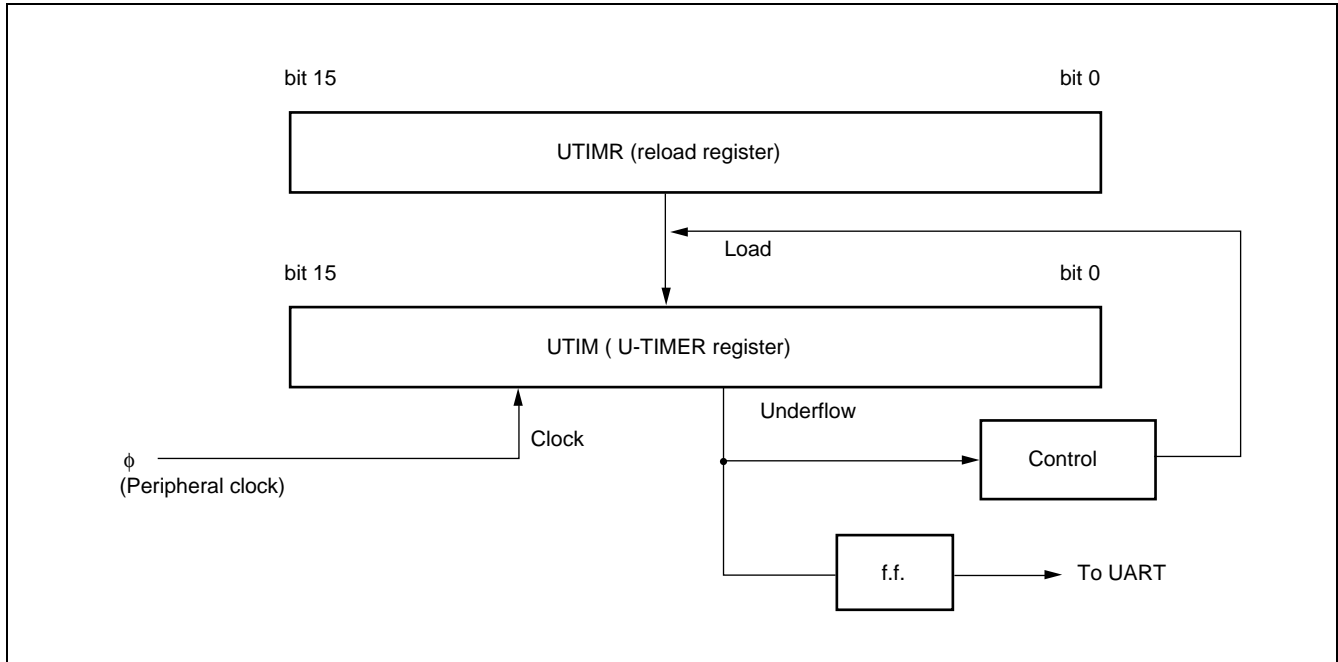
4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91121 has 3 channel U-TIMER embedded on the chip. An interval of up to $2^{16} \times \phi$ can be counted.

• Block diagram



• Register configuration

Address	bit 15	bit 0	Initial value	
00000078H 00000079H	UTIM0/UTIMR0		00000000B 00000000B	(R/W)
⋮				
0000007CH 0000007DH	UTIM1/UTIMR1		00000000B 00000000B	(R/W)
⋮				
00000080H 00000081H	UTIM2/UTIMR2		00000000B 00000000B	(R/W)
0000007BH	UTIMC0		0--00001B	(R/W)
0000007FH	UTIMC1		0--00001B	(R/W)
00000083H	UTIMC2		0--00001B	(R/W)

() : Access
R/W : Readable and writable
— : Unused

5. PWM Timer

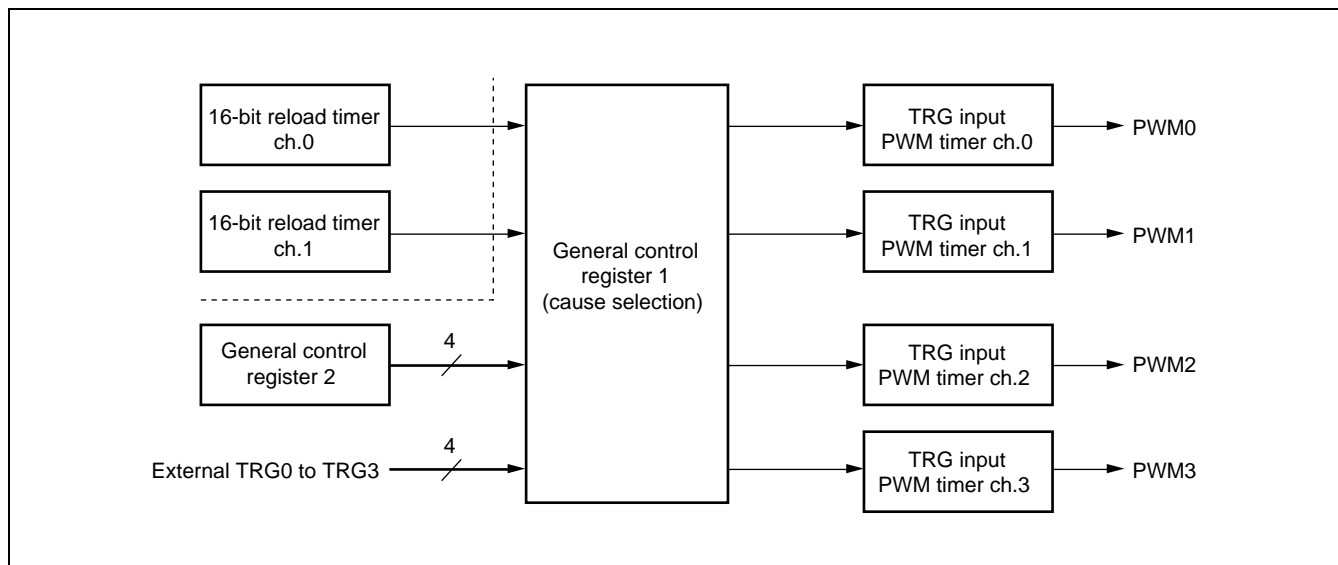
The PWM timer can output high accurate PWM waves efficiently.

MB91121 has inner 4-channel PWM timers, and has the following features.

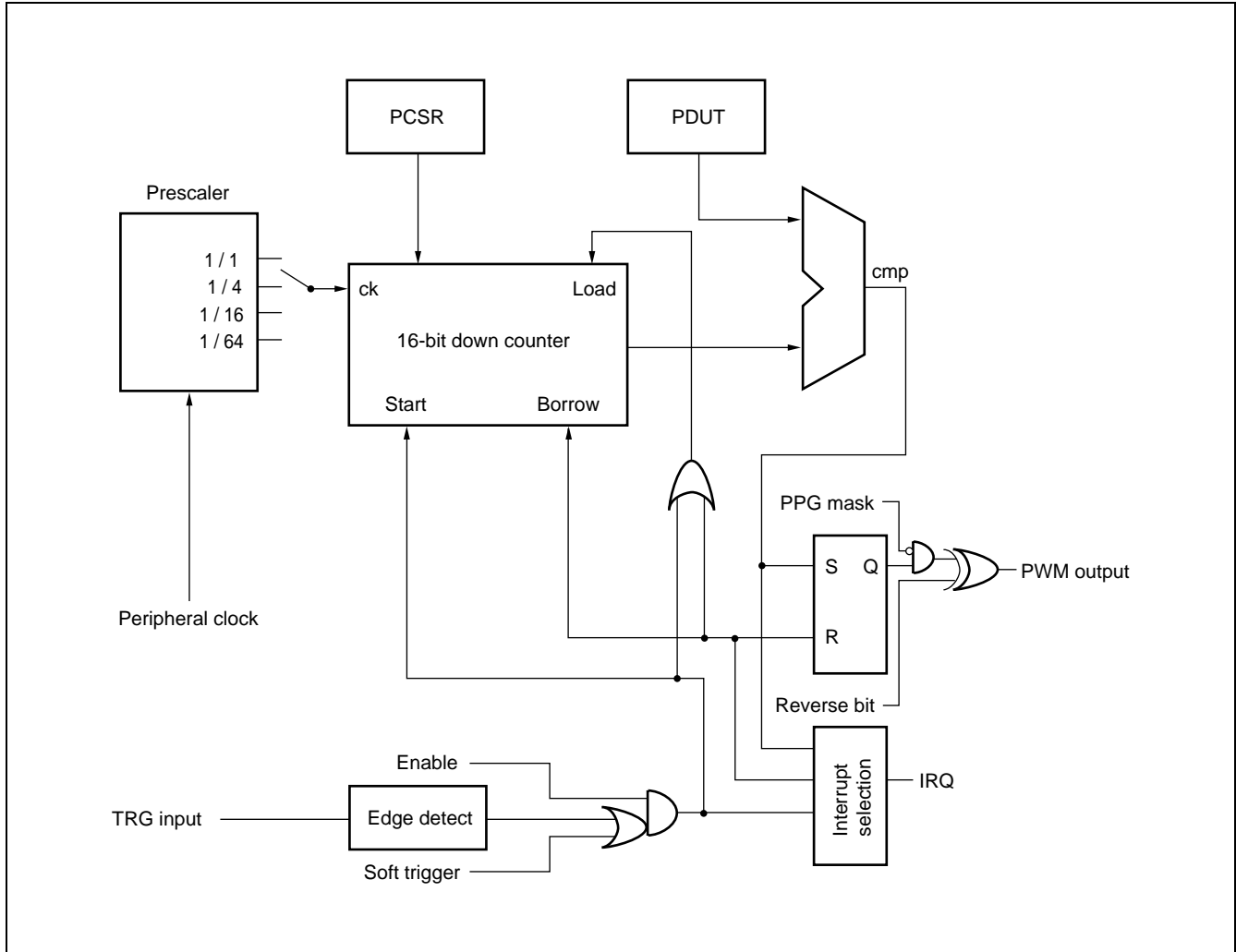
- Each channel consists of a 16-bit down counter, a 16-bit data register with a buffer for cycle setting, a 16-bit compare register with a buffer for duty setting, and a pin controller.
- The count clock of a 16-bit down counter can be selected from the following four inner clocks.
Inner clock ϕ , $\phi/4$, $\phi/16$, $\phi/64$

- The counter value can be initialized “FFFF_H” by the resetting or the counter borrow.
- PWM output (each channel)
- Register description

- **Block diagram (general construction)**



• Block diagram (for one channel)



• Register configuration

Address	bit 15	bit 8	bit 0	Initial value	
000000DC _H 000000DD _H	GCN1			00110010 _B 00010010 _B	(R/W)
000000DF _H		GCN2		00000000 _B	(R/W)
000000E0 _H 000000E1 _H	PTMR0			11111111 _B 11111111 _B	(R)
000000E2 _H 000000E3 _H	PCSR0			XXXXXXXX _B XXXXXXXX _B	(W)
000000E4 _H 000000E5 _H	PDUT0			XXXXXXXX _B XXXXXXXX _B	(W)
000000E6 _H	PCNH0			0000000- _B	(R/W)
000000E7 _H		PCNL0		00000000 _B	(R/W)
000000E8 _H 000000E9 _H	PTMR1			11111111 _B 11111111 _B	(R)
000000EA _H 000000EB _H	PCSR1			XXXXXXXX _B XXXXXXXX _B	(W)
000000EC _H 000000ED _H	PDUT1			XXXXXXXX _B XXXXXXXX _B	(W)
000000EE _H	PCNH1			0000000- _B	(R/W)
000000EF _H		PCNL1		00000000 _B	(R/W)
000000F0 _H 000000F1 _H	PTMR2			11111111 _B 11111111 _B	(R)
000000F2 _H 000000F3 _H	PCSR2			XXXXXXXX _B XXXXXXXX _B	(W)
000000F4 _H 000000F5 _H	PDUT2			XXXXXXXX _B XXXXXXXX _B	(W)
000000F6 _H	PCNH2			0000000- _B	(R/W)
000000F7 _H		PCNL2		00000000 _B	(R/W)
000000F8 _H 000000F9 _H	PTMR3			11111111 _B 11111111 _B	(R)
000000FA _H 000000FB _H	PCSR3			XXXXXXXX _B XXXXXXXX _B	(W)
000000FC _H 000000FD _H	PDUT3			XXXXXXXX _B XXXXXXXX _B	(W)
000000FE _H	PCNH3			0000000- _B	(R/W)
000000FF _H		PCNL3		00000000 _B	(R/W)

() : Access
 R/W : Readable and writable
 R : Read only
 W : Write only
 — : Unused
 X : Indeterminate

6. 16-bit Reload Timer

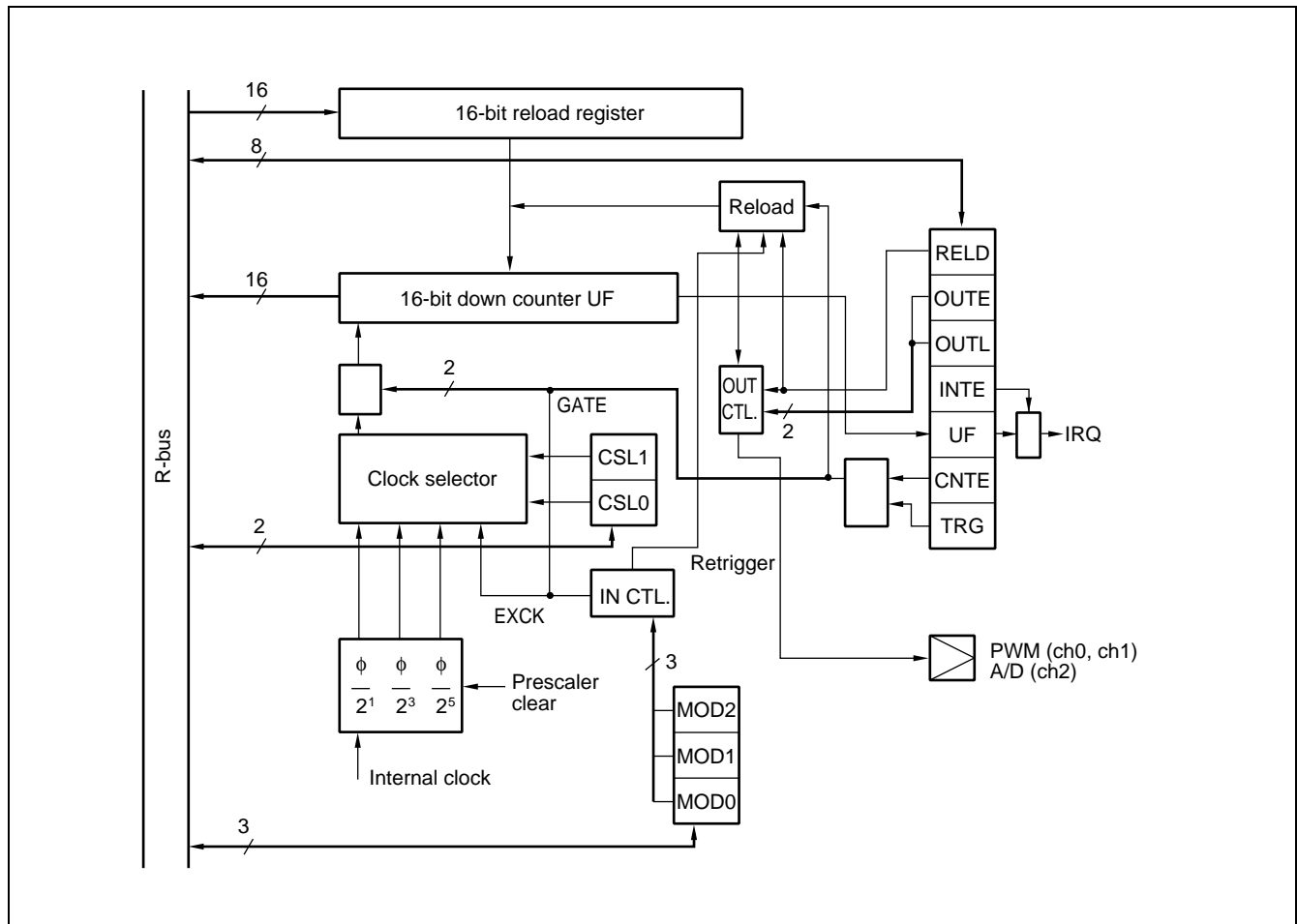
The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock) .

The DMA transfer can be started by the interruption.

The MB91121 consists of 3 channels of the 16-bit reload timer.

• Block diagram



• Register configuration

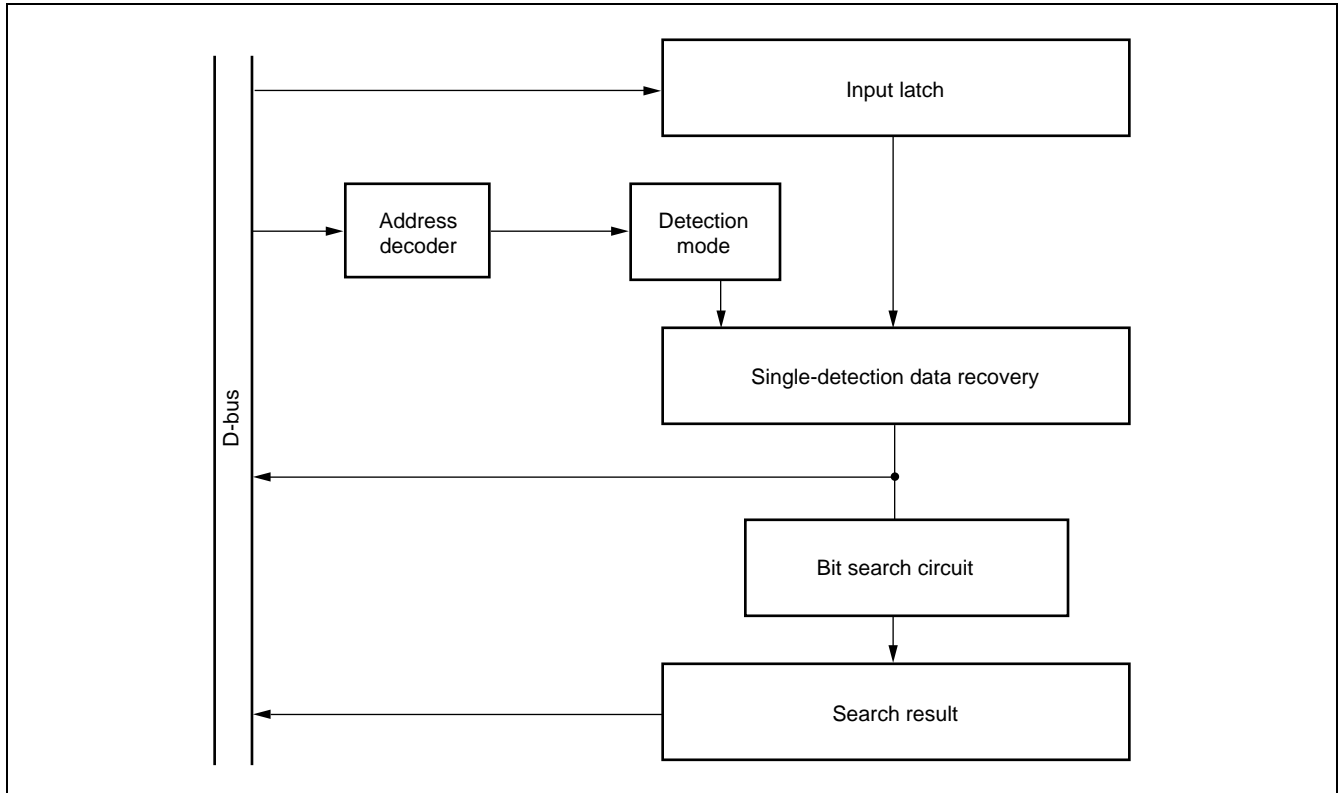
Address	bit 15	bit 0	Initial value	
0000002E _H 0000002F _H	TMCSR0		----0000 _B 00000000 _B	(R/W)
00000036 _H 00000037 _H	TMCSR1		----0000 _B 00000000 _B	(R/W)
00000042 _H 00000043 _H	TMCSR2		----0000 _B 00000000 _B	(R/W)
0000002A _H 0000002B _H	TMR0		XXXXXXXX _B XXXXXXXX _B	(R)
00000032 _H 00000033 _H	TMR1		XXXXXXXX _B XXXXXXXX _B	(R)
0000003E _H 0000003F _H	TMR2		XXXXXXXX _B XXXXXXXX _B	(R)
00000028 _H 00000029 _H	TMRLR0		XXXXXXXX _B XXXXXXXX _B	(W)
00000030 _H 00000031 _H	TMRLR1		XXXXXXXX _B XXXXXXXX _B	(W)
0000003C _H 0000003D _H	TMRLR2		XXXXXXXX _B XXXXXXXX _B	(W)

() : Access
 R/W : Readable and writable
 R : Read only
 W : Write only
 — : Unused
 X : Indeterminate

7. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

• Block diagram



• Register configuration

Address	bit 31	bit 16	bit 0	Initial value	
000003F0 _H	<div style="border: 1px solid black; padding: 2px; text-align: center;">BSD0</div>			XXXXXXXX _B	(W)
000003F1 _H				XXXXXXXX _B	
000003F2 _H				XXXXXXXX _B	
000003F3 _H				XXXXXXXX _B	
000003F4 _H	<div style="border: 1px solid black; padding: 2px; text-align: center;">BSD1</div>			XXXXXXXX _B	(W)
000003F5 _H				XXXXXXXX _B	
000003F6 _H				XXXXXXXX _B	
000003F7 _H				XXXXXXXX _B	
000003F8 _H	<div style="border: 1px solid black; padding: 2px; text-align: center;">BSDC</div>			XXXXXXXX _B	(W)
000003F9 _H				XXXXXXXX _B	
000003FA _H				XXXXXXXX _B	
000003FB _H				XXXXXXXX _B	
000003FC _H	<div style="border: 1px solid black; padding: 2px; text-align: center;">BSRR</div>			XXXXXXXX _B	(W)
000003FE _H				XXXXXXXX _B	
000003FD _H				XXXXXXXX _B	
000003FF _H				XXXXXXXX _B	

() : Access
 R/W : Readable and writable
 R : Read only
 W : Write only
 X : Indeterminate

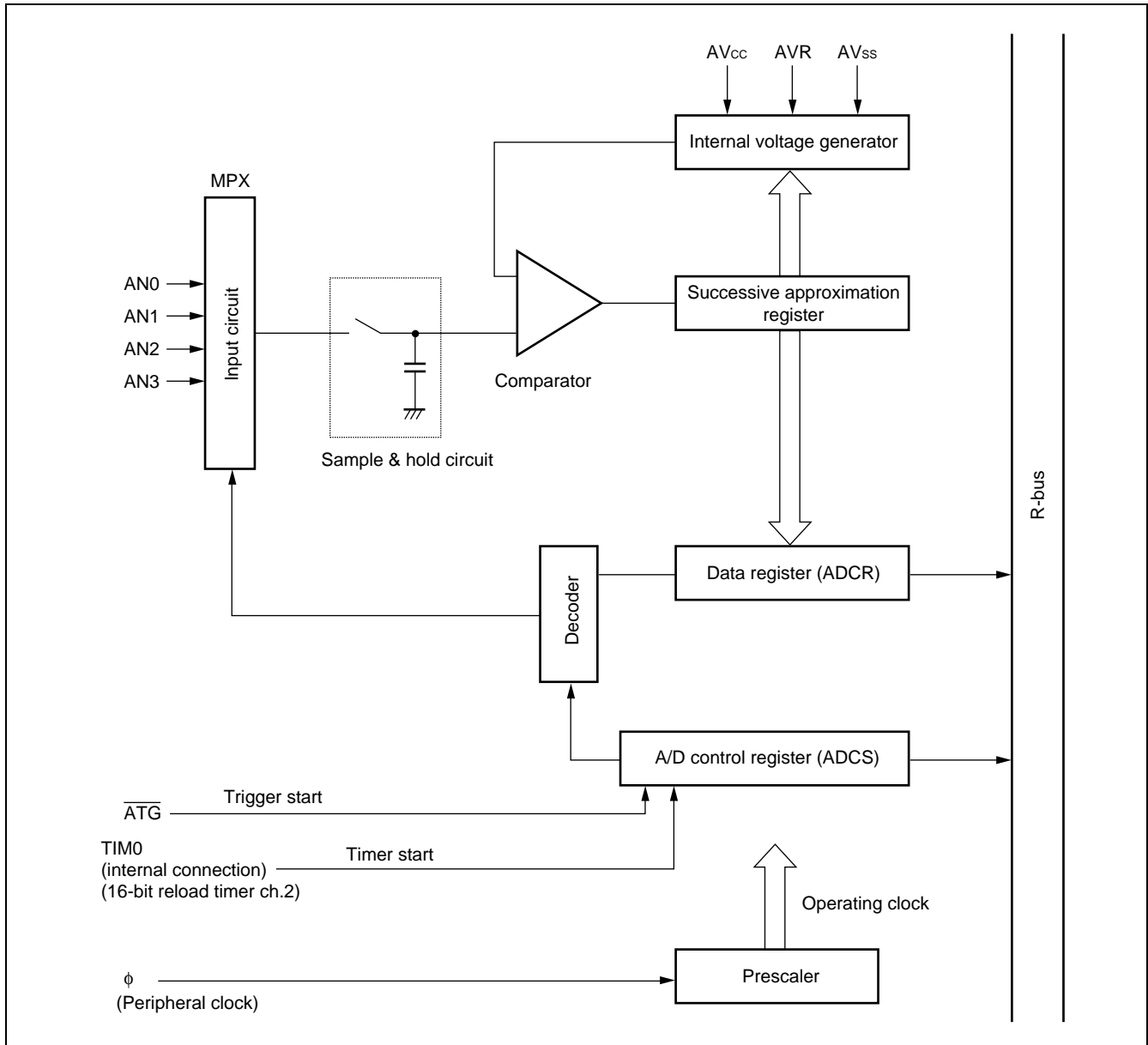
8. 10-bit A/D Converter (Successive Approximation Conversion Type)

The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time : 5.6 μ s/ch. (system clock : 25 MHz)
- Inner sample and hold circuit
- Resolution : 10 bits
- Analog input can be selected from 4 channels by program.
 - Single convert mode : 1 channel is selected and converted.
 - Scan convert mode : Converting continuous channels. Maximum 4 channels are programmable.
 - Continuous convert mode : Converting the specified channel repeatedly.
 - Stop convert mode : After converting one channel then stop and wait till next activation synchronising at the beginning of conversion can be performed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge) , and 16-bit reload timer (rising edge) .

MB91121

• Block diagram



• Register configuration

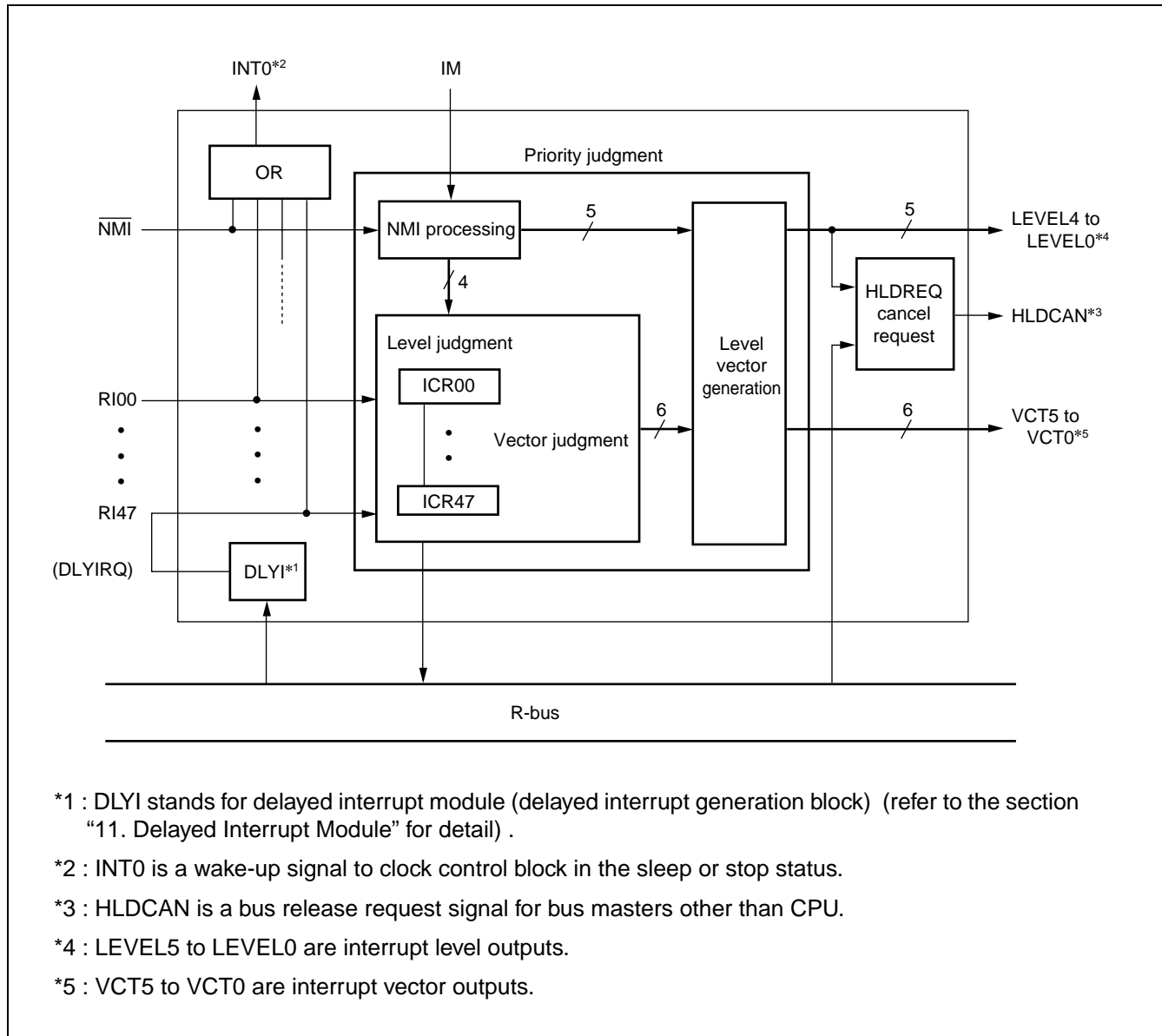
Address	bit 15	bit 0	Initial value
0000003AH 0000003BH	ADCS		00000000 _B 00000000 _B (R/W)
00000038H 00000039H	ADCR		-----XX _B XXXXXXXXXX _B (R)

() : Access
 R/W : Readable and writable
 R : Read only
 — : Unused
 X : Indeterminate

9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

• Block diagram



*1 : DLYI stands for delayed interrupt module (delayed interrupt generation block) (refer to the section "11. Delayed Interrupt Module" for detail) .

*2 : INT0 is a wake-up signal to clock control block in the sleep or stop status.

*3 : HLDCAN is a bus release request signal for bus masters other than CPU.

*4 : LEVEL5 to LEVEL0 are interrupt level outputs.

*5 : VCT5 to VCT0 are interrupt vector outputs.

• Register configuration

Address	bit 7	bit 0	Initial value	Address	bit 7	bit 0	Initial value
00000400 _H	ICR00		--- 1 1 1 1 _B (R/W)	00000411 _H	ICR17		--- 1 1 1 1 _B (R/W)
00000401 _H	ICR01		--- 1 1 1 1 _B (R/W)	00000412 _H	ICR18		--- 1 1 1 1 _B (R/W)
00000402 _H	ICR02		--- 1 1 1 1 _B (R/W)	00000413 _H	ICR19		--- 1 1 1 1 _B (R/W)
00000403 _H	ICR03		--- 1 1 1 1 _B (R/W)	00000414 _H	ICR20		--- 1 1 1 1 _B (R/W)
00000404 _H	ICR04		--- 1 1 1 1 _B (R/W)	00000415 _H	ICR21		--- 1 1 1 1 _B (R/W)
00000405 _H	ICR05		--- 1 1 1 1 _B (R/W)	00000416 _H	ICR22		--- 1 1 1 1 _B (R/W)
00000406 _H	ICR06		--- 1 1 1 1 _B (R/W)	00000417 _H	ICR23		--- 1 1 1 1 _B (R/W)
00000407 _H	ICR07		--- 1 1 1 1 _B (R/W)	00000418 _H	ICR24		--- 1 1 1 1 _B (R/W)
00000408 _H	ICR08		--- 1 1 1 1 _B (R/W)	00000419 _H	ICR25		--- 1 1 1 1 _B (R/W)
00000409 _H	ICR09		--- 1 1 1 1 _B (R/W)	0000041A _H	ICR26		--- 1 1 1 1 _B (R/W)
0000040A _H	ICR10		--- 1 1 1 1 _B (R/W)	0000041B _H	ICR27		--- 1 1 1 1 _B (R/W)
0000040B _H	ICR11		--- 1 1 1 1 _B (R/W)	0000041C _H	ICR28		--- 1 1 1 1 _B (R/W)
0000040C _H	ICR12		--- 1 1 1 1 _B (R/W)	0000041D _H	ICR29		--- 1 1 1 1 _B (R/W)
0000040D _H	ICR13		--- 1 1 1 1 _B (R/W)	0000041E _H	ICR30		--- 1 1 1 1 _B (R/W)
0000040E _H	ICR14		--- 1 1 1 1 _B (R/W)	0000041F _H	ICR31		--- 1 1 1 1 _B (R/W)
0000040F _H	ICR15		--- 1 1 1 1 _B (R/W)	0000042F _H	ICR47		--- 1 1 1 1 _B (R/W)
00000410 _H	ICR16		--- 1 1 1 1 _B (R/W)	00000431 _H	HRCL		--- 1 1 1 1 _B (R/W)
				00000430 _H	DICR		----- 0 _B (R/W)

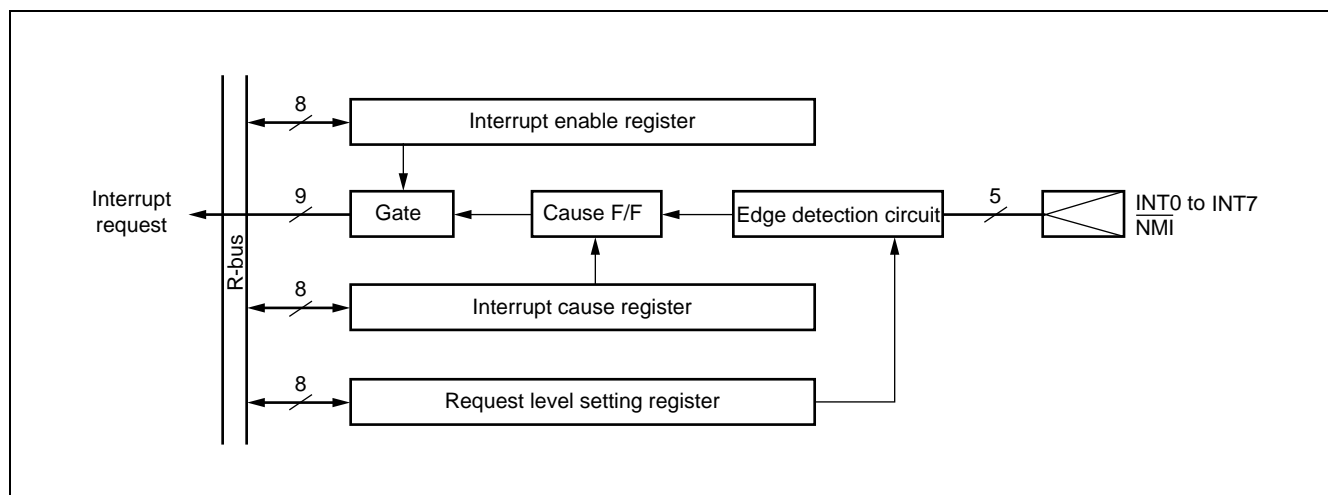
() : Access
R/W : Readable and writable
— : Unused

10. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to $\overline{\text{NMI}}$ pin and INT0 to INT3 pins.

Detecting levels can be selected from "H", "L", rising edge and falling edge (not for $\overline{\text{NMI}}$ pin) .

• Block diagram



• Register configuration

Address	bit 15	bit 8	bit 0	Initial value	
00000095 _H		ENIR		0 0 0 0 0 0 0 0 _B	(R/W)
00000094 _H	EIRR			0 0 0 0 0 0 0 0 _B	(R/W)
00000099 _H	ELVR			0 0 0 0 0 0 0 0 _B	(R/W)

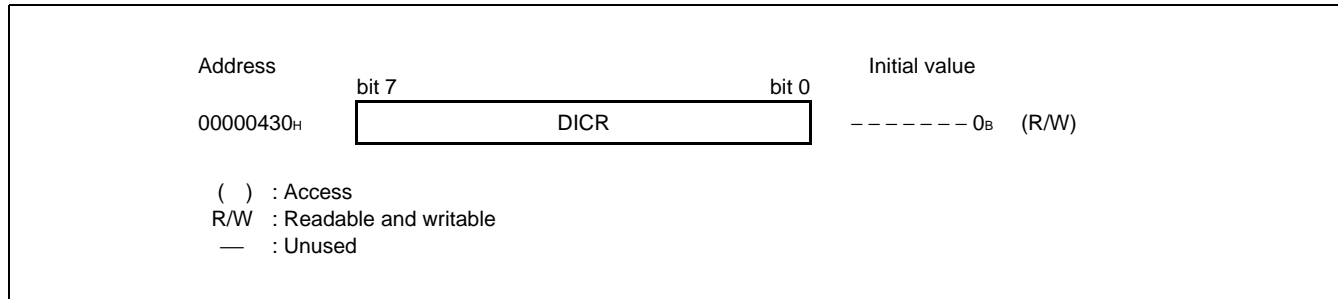
() : Access
R/W : Readable and writable

11. Delayed Interrupt Module

Delayed interrupt module is a module which generates an interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.

Refer to the section "9. Interrupt Controller" for delayed interrupt module block diagram.

- Register configuration



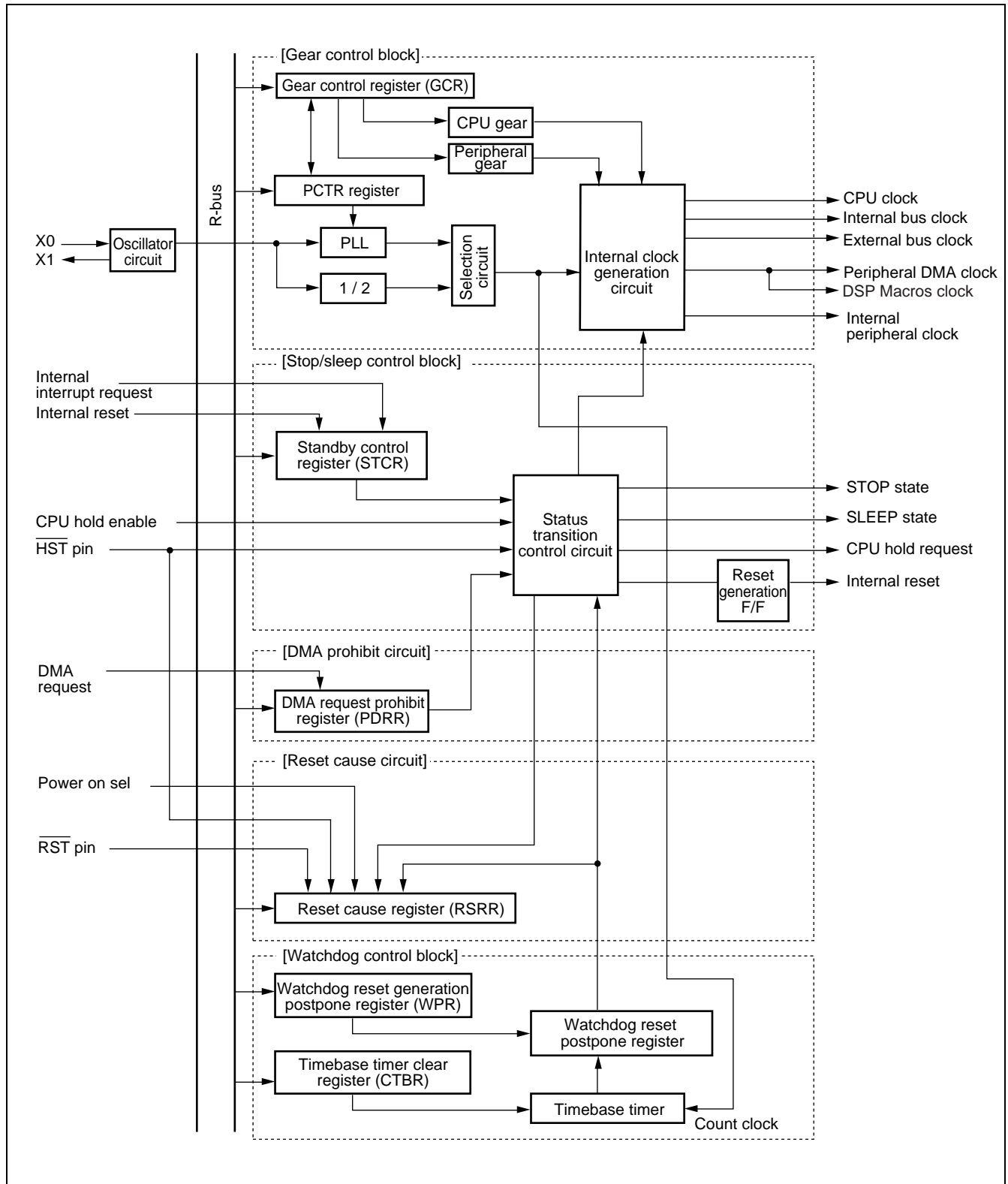
12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function (including hardware standby)
- DMA request prohibit
- PLL (multiplier circuit) embedded

MB91121

• Block diagram



• Register configuration

Address	bit 15	bit 8	bit 0	Initial value
00000480 _H	RSRR/WTCR			1XXXX-00 _B (R/W)
00000481 _H		STCR		000111-- _B (R/W)
00000482 _H	PDRR			----0000 _B (R/W)
00000483 _H		CDBR		XXXXXXXX _B (W)
00000484 _H	GCR			110011-1 _B (R/W)
00000485 _H		WPR		XXXXXXXX _B (W)

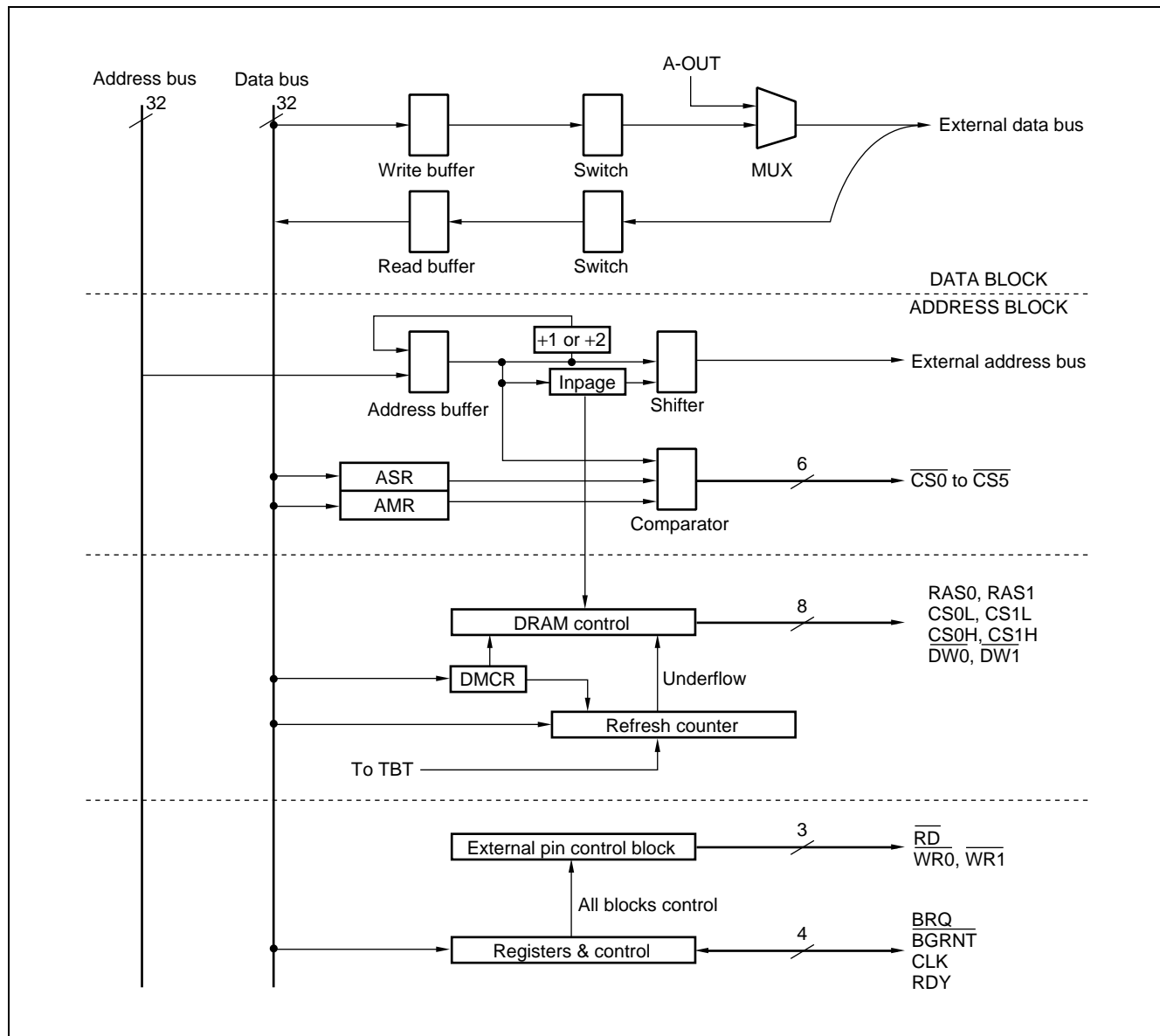
() : Access
 R/W : Readable and writable
 R : Read only
 — : Unused
 X : Indeterminate

13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.
Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.
Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
- Programmable automatic memory wait (Max. for 7 cycles) can be inserted.
- DRAM interface support
Three kinds of DRAM interface : Double CAS DRAM (normally DRAM I/F)
Single CAS DRAM
Hyper DRAM
2 banks independent control (RAS, CAS, etc. control signals)
DRAM select is available from 2CAS/1WE and 1CAS/2WE.
Hi-speed page mode supported
CBR/self refresh supported
Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Clock doublure : Internal bus 50 MHz, external bus 25 MHz

• Block diagram



• Register configuration

Address	bit 31	bit 16	bit 0	Initial value	
0000060C _H 0000060D _H	ASR1			00000000 _B 00000001 _B	(W)
0000060E _H 0000060F _H		AMR1		00000000 _B 00000000 _B	(W)
00000610 _H 00000611 _H	ASR2			00000000 _B 00000010 _B	(W)
00000612 _H 00000613 _H		AMR2		00000000 _B 00000000 _B	(W)
00000614 _H 00000615 _H	ASR3			00000000 _B 00000011 _B	(W)
00000616 _H 00000617 _H		AMR3		00000000 _B 00000000 _B	(W)
00000618 _H 00000619 _H	ASR4			00000000 _B 00000100 _B	(W)
0000061A _H 0000061B _H		AMR4		00000000 _B 00000000 _B	(W)
0000061C _H 0000061D _H	ASR5			00000000 _B 00000101 _B	(W)
0000061E _H 0000061F _H		AMR5		00000000 _B 00000000 _B	(W)
00000620 _H	AMD0			---00111 _B	(R/W)
00000621 _H		AMD1		0--00000 _B	(R/W)
00000622 _H			AMD32	00000000 _B	(R/W)
00000623 _H				AMD4	0--00000 _B (R/W)
00000624 _H	AMD5			0--00000 _B	(R/W)
00000625 _H		DSCR		00000000 _B	(W)
00000626 _H 00000627 _H			RFCR	--XXXXXX _B 00---000 _B	(R/W)
00000628 _H 00000629 _H	EPCR0			---11000 _B -1111111 _B	(W)
0000062B _H			EPCR1	11111111 _B	(W)
0000062C _H 0000062D _H	DMCR4			00000000 _B 0000000- _B	(R/W)
0000062E _H 0000062F _H			DMCR5	00000000 _B 0000000- _B	(R/W)
000007FE _H			LER	-----000 _B	(W)
000007FF _H			MODR	XXXXXXXXXX _B	(W)

() : Access
W : Write only
X : Indeterminate

R/W : Readable and writable
— : Unused

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	
Analog supply voltage	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*1
Analog reference voltage	$AVRH$	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Analog pin input voltage	V_{IA}	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level maximum output current	I_{OL}	—	10	mA	*2
"L" level average output current	I_{OLAV}	—	4	mA	*3
"L" level maximum total output current	ΣI_{OL}	—	100	mA	
"L" level average total output current	ΣI_{OLAV}	—	50	mA	*4
"H" level maximum output current	I_{OH}	—	-10	mA	*2
"H" level average output current	I_{OHAV}	—	-4	mA	*3
"H" level maximum total output current	ΣI_{OH}	—	-50	mA	
"H" level average total output current	ΣI_{OHAV}	—	-20	mA	*4
Power consumption	P_D	—	600	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	T_{stg}	-55	+150	°C	

*1 : Care must be taken that AV_{CC} and $AVRH$ do not exceed $V_{CC} + 0.3\text{ V}$, such as when turning on the device.
Also, care must be taken that $AVRH$ does not exceed AV_{CC} .

*2 : Maximum output current is a peak current value measured at a corresponding pin.

*3 : Average output current is an average current for a 100 ms period at a corresponding pin.

*4 : Average total output current is an average current for a 100 ms period for all corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	3.6	V	
Analog supply voltage	AV_{CC}	$V_{SS} + 0.3$	$V_{SS} + 3.6$	V	
Analog reference voltage	AV_{RH}	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	V_{IH}	Input pin except for hysteresis input	—	$0.65 \times V_{CC}$	—	$V_{CC} + 0.3$	V	*2
	V_{IHS}	*1	—	$0.8 \times V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input*2
“L” level input voltage	V_{IL}	Input pin except for hysteresis input	—	$V_{SS} - 0.3$	—	$0.25 \times V_{CC}$	V	*2
	V_{ILS}	*1	—	$V_{SS} - 0.3$	—	$0.2 \times V_{CC}$	V	Hysteresis input*2
“H” level output voltage	V_{OH}	D16 to D31 A00 to A24 P6 to PF	$V_{CC} = 3.0\text{ V}$ $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	V_{OL}	D16 to D31 A00 to A24 P6 to PF	$V_{CC} = 3.0\text{ V}$ $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	D00 to D31 A00 to A23 P8 to PF	$V_{CC} = 3.6\text{ V}$ $0.45\text{ V} < V_I < V_{CC}$	-5	—	+5	μA	
Pull-up resistance	R_{PULL}	\overline{RST}	$V_{CC} = 3.6\text{ V}$ $V_I = 0.45\text{ V}$	25	50	100	$\text{k}\Omega$	
Power supply current	I_{CC}	V_{CC}	$F_C = 12.5\text{ MHz}$ $V_{CC} = 3.3\text{ V}$	—	130	180	mA	(4 multiplication) Operation at 50 MHz
	I_{CCS}		$F_C = 12.5\text{ MHz}$ $V_{CC} = 3.3\text{ V}$	—	85	120	mA	Sleep mode
	I_{CCH}		$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 3.3\text{ V}$	—	15	150	μA	Stop mode
Input capacitance	C_{IN}	Except for V_{CC} , AV_{CC} , AV_{SS} , V_{SS}	—	—	10	—	pF	

*1 : Hysteresis input pin : \overline{NMI} , \overline{RST} , P60 to P67, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7, PG0 to PG7, PI0, PI1

*2 : $V_{CC3} = 3.3 \pm 0.2\text{ V}$ (internal regulator output voltage) when using 5 V power supply, $V_{CC3} =$ power supply voltage when using 3V power supply (internal regulator unused)

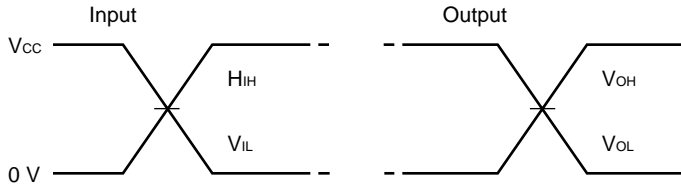
4. AC Characteristics

(1) Measurement Conditions

The following conditions apply to AC characteristics unless otherwise specified.

- **Measurement conditions for AC standards**

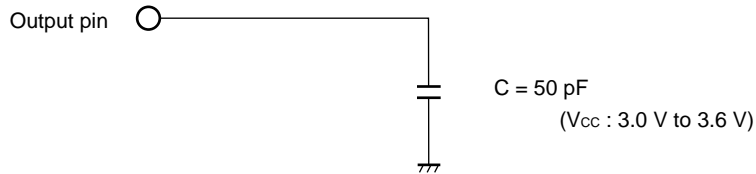
$V_{CC} : 3.0 \text{ V to } 3.6 \text{ V}$



V_{IH}	$1/2 * V_{CC}$	V_{OH}	$1/2 * V_{CC}$
V_{IL}	$1/2 * V_{CC}$	V_{OL}	$1/2 * V_{CC}$

(The input rise/fall time is 10 ns or less.)

- **Load condition**

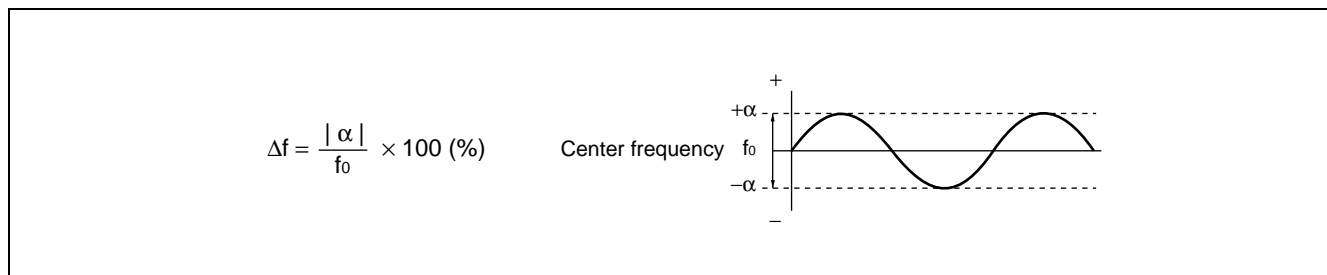


(2) Clock Timing Rating

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency (1)	F _C	X0, X1	—	10	12.5	MHz	When using PLL
Clock cycle time	t _c	X0, X1		80	100	ns	
Frequency shift ratio*1 (when locked)	Δf			—	5	%	
Clock frequency (2)	F _C	X0, X1	—	10	25	MHz	Self-oscillation (divide-by-2 input)
Clock frequency (3)	F _C	X0, X1		10	25	MHz	External clock (divide-by-2 input)
Clock cycle time	t _c	X0, X1		40	100	ns	
Input clock pulse width	P _{WH} , P _{WL}	X0, X1		25	—	ns	Input to X0 only
				10	—	ns	Input to X0, X1
Input clock rising/falling time	t _{CR} , t _{CF}	X0, X1		—	8	ns	(t _{CR} + t _{CF})
Internal operating clock frequency	f _{CP}			0.625*2	50	MHz	CPU system
	f _{CPB}		0.625*2	25*3	MHz	Bus system	
	f _{CPP}		0.625*2	25	MHz	Peripheral system	
Internal operating clock cycle time	t _{CP}		20	1600*2	ns	CPU system	
	t _{CPB}		40*3	1600*2	ns	Bus system	
	t _{CPP}		40	1600*2	ns	Peripheral system	

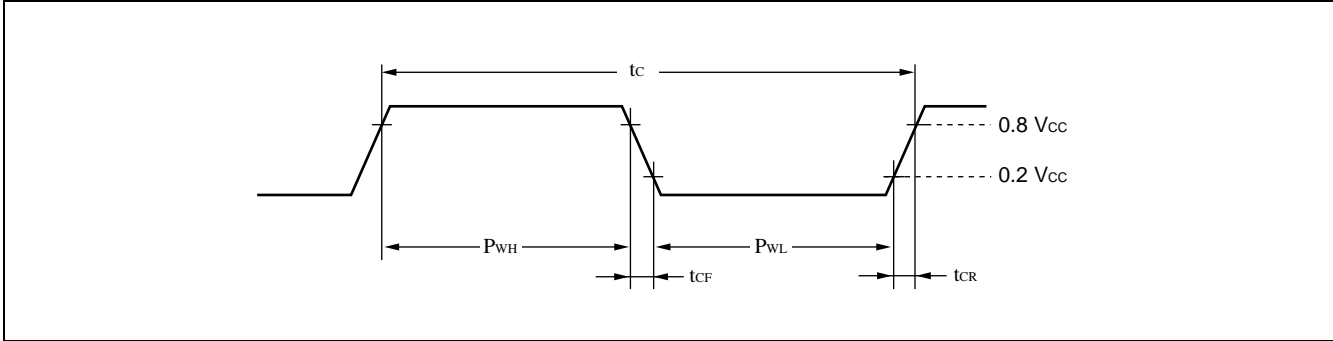
*1 : Frequency shift ratio stands for deviation ratio of the operating clock from the center frequency in the clock multiplication system.



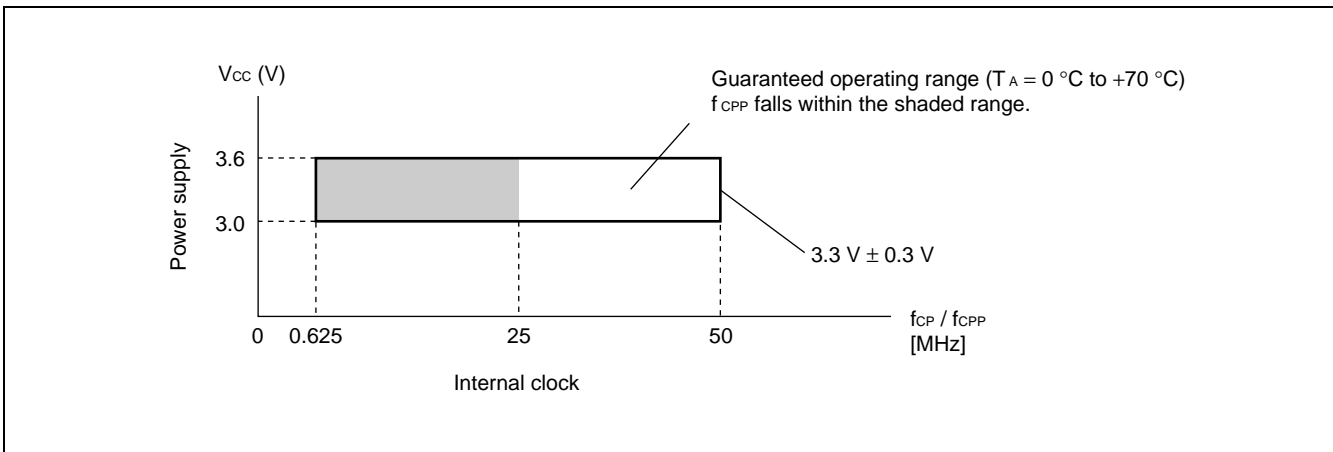
*2 : These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

*3 : Values when using the double and CPU operation at 50 MHz.

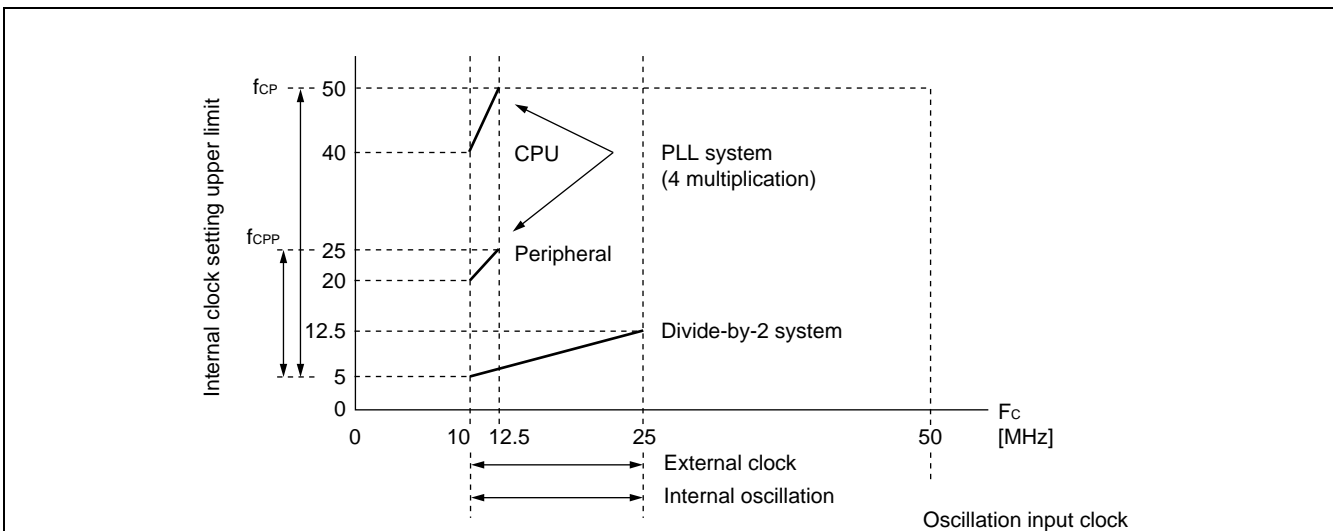
• Clock timing rating measurement conditions



• Guaranteed operating range



• External/internal clock setting range

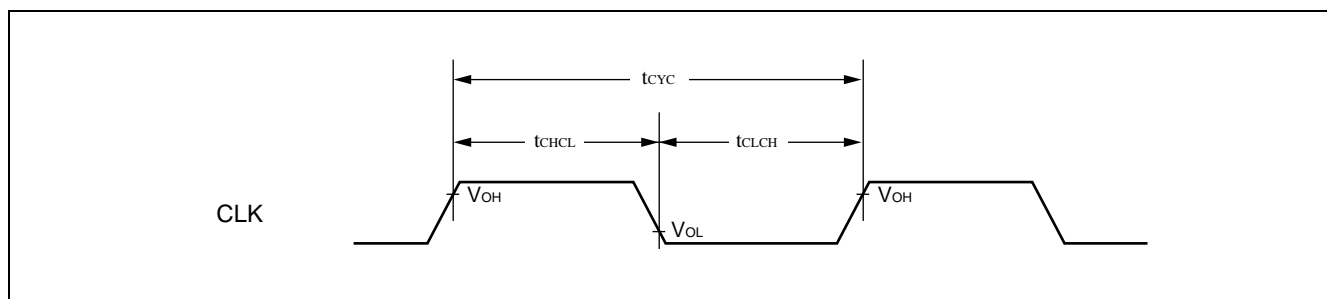


- Note : 1.If the PLL is used, the external clock input should be 10.0 MHz to 12.5 MHz.
 2.The PLL oscillation settling time must be longer than 300 μs .
 3.The internal clock gear setting must fall within the above range.

(3) Clock Output Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
				t_{CPB}	—		Using the doublure
CLK \uparrow \rightarrow CLK \downarrow	t_{CHCL}	CLK	—	$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*2
CLK \downarrow \rightarrow CLK \uparrow	t_{CLCH}	CLK		$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*3



*1 : t_{CYC} is a frequency for 1 clock cycle including a gear cycle.

Use the doublure when CPU frequency is above 25 MHz.

*2 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min. : } (1 - n / 2) \times t_{CYC} - 10$$

$$\text{Max. : } (1 - n / 2) \times t_{CYC} + 10$$

Select a gear cycle of $\times 1$ when using the doublure.

*3 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min. : } n / 2 \times t_{CYC} - 10$$

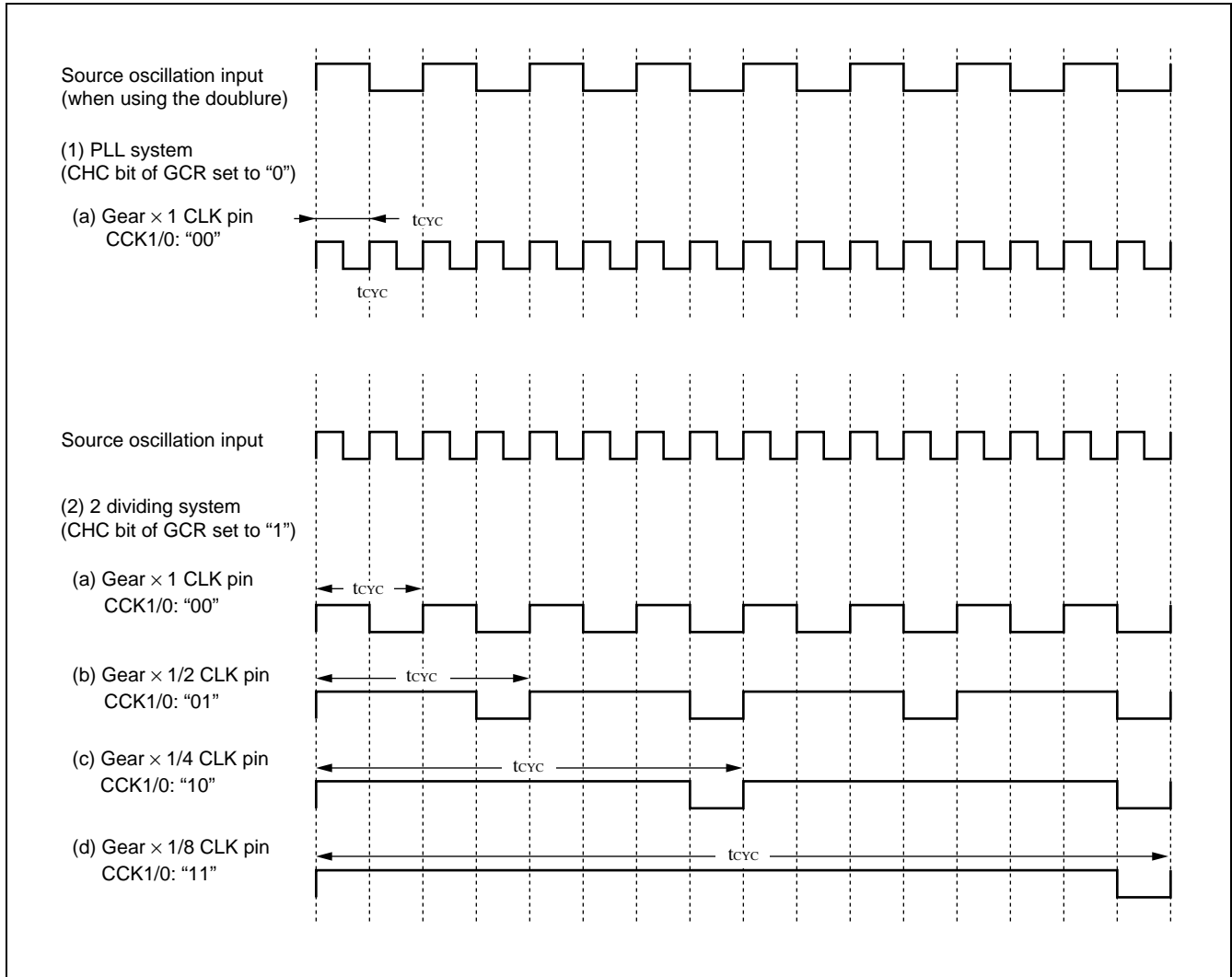
$$\text{Max. : } n / 2 \times t_{CYC} + 10$$

Select a gear cycle of $\times 1$ when using the doublure.

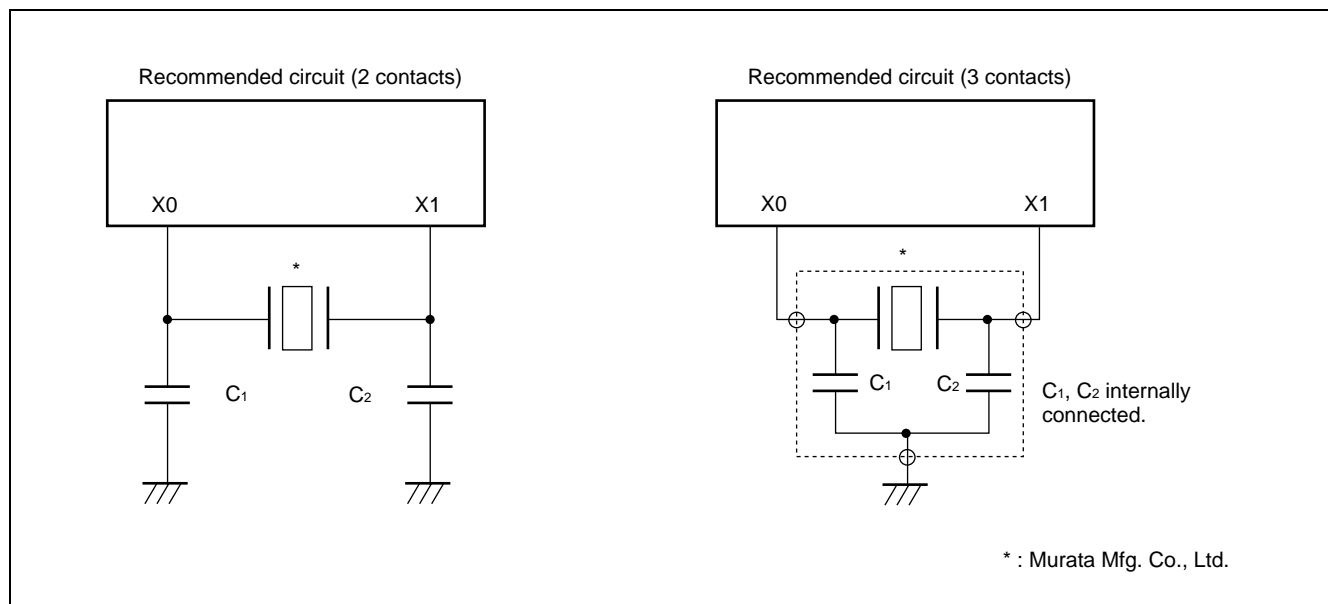
MB91121

The relation between source oscillation input and CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows:

However, in this chart source oscillation input means X0 input clock.



• Ceramc oscillator applications



• Discrete type

Oscillation frequency [MHz]	Model name	Circuit constants				Pin type
		C1[pF]	C1[pF]	Rf[Ω]*1	Rd[Ω]*2	
10.00 to 13.00	CSA□MTZ	30	30	—	0	Two-pin
	CST□MTW	(30)	(30)	—	0	Three-pin
13.01 to 15.99	CSA□MXZ040	15	15	—	0	Two-pin
	CST□MXW0C3	(15)	(15)	—	0	Three-pin
16.00 to 19.99	CSA□MXZ040	(10)	(10)	—	0	Two-pin
	*****	*****	*****	*****	*****	Three-pin
20.00 to 25.00	CSA□MXZ004	None	None	—	0	Two-pin
	*****	*****	*****	*****	*****	Three-pin

*1 : Feedback resistor Rf is built in the LSI.

*2 : No dumping resistor is required.

() : C1 and C2 integrated

MB91121

• SMD type

Oscillation frequency [MHz]	Model name	Circuit constants				Pin type
		C1[pF]	C1[pF]	Rf[Ω]*1	Rd[Ω]*2	
10.00 to 13.00	CSACS□MT	30	30	—	0	Two-pin
	CSTCS□MT	(30)	(30)	—	0	Three-pin
13.01 to 15.99	CSACS□MX040	15	15	—	0	Two-pin
	CSTCS□MX0C3	(15)	(15)	—	0	Three-pin
16.00 to 19.99	CSACS□MX040	10	10	—	0	Two-pin
	CSTCS□MX0C2	(10)	(10)	—	0	Three-pin
20.00 to 25.00	CSACS□MX040	None	None	—	0	Two-pin
	*****	****	****	****	****	Three-pin

*1 : Feedback resistor Rf is built in the LSI.

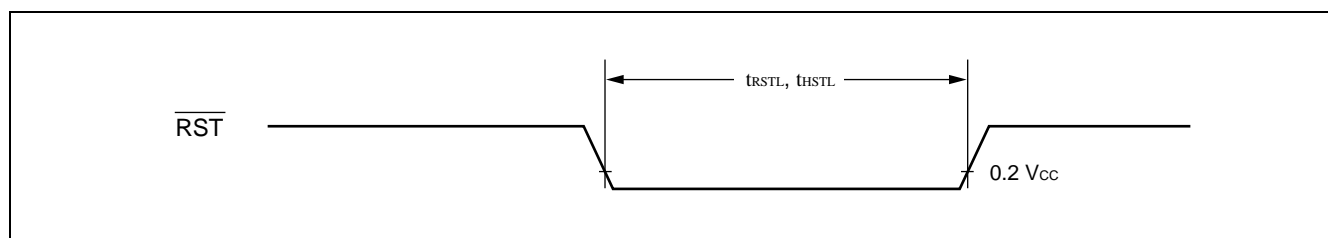
*2 : No dumping resistor is required.

() : C₁ and C₂ integrated

(4) Reset input ratings

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	—	$t_{CP} \times 5$	—	ns	

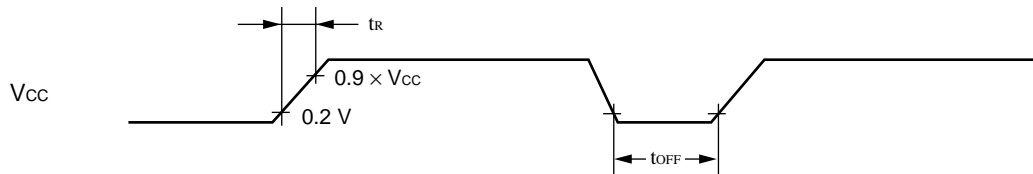


MB91121

(5) Power-on Reset

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$)

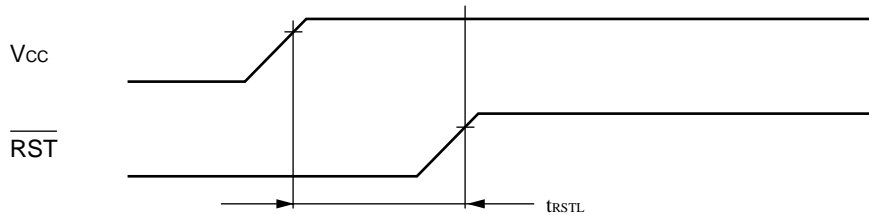
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_r	V_{CC}	$V_{CC} = 3.3\text{ V}$	$50\ \mu\text{s}$	18	ms	$V_{CC} < 0.2\text{ V}$ before the power supply rising
Power supply shut off time	t_{OFF}	V_{CC}	—	1	—	ms	Repeated operations



Note: Sudden change in supply voltage during operation may initiate a power-on sequence. To change supply voltage during operation, it is recommended to smoothly raise the voltage to avoid rapid fluctuations in the supply voltage.



Note: Set $\overline{\text{RST}}$ pin to ÖÖ level when turning on the device, at least the described above duration after the supply voltage reaches V_{CC} is necessary before turning the RST to ÖÖ level.



(6) Normal Bus Access Read/write Operation

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{CS0}$ to $\overline{CS5}$ delay time	t_{CHCSL}	CLK $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	t_{CHCSH}	$\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	t_{CHAV}	CLK A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK D31 to D16		—	15	ns	
\overline{RD} delay time	$t_{CLR L}$	CLK \overline{RD}		—	10	ns	
	$t_{CLR H}$	\overline{RD}		—	10	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK $\overline{WR0}$, $\overline{WR1}$		—	10	ns	
	t_{CLWH}	$\overline{WR0}$, $\overline{WR1}$		—	10	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00 D31 to D16		—	$3 / 2 \times t_{CYC} - 40$	ns	*1 *2
$\overline{RD} \downarrow \rightarrow$ valid data input time	t_{RLDV}			—	$t_{CYC} - 25$	ns	*1
Data set up → $\overline{RD} \uparrow$ time	t_{DSRH}	\overline{RD} D31 to D16	25	—	ns		
$\overline{RD} \uparrow \rightarrow$ data hold time	t_{RHDX}		0	—	ns		

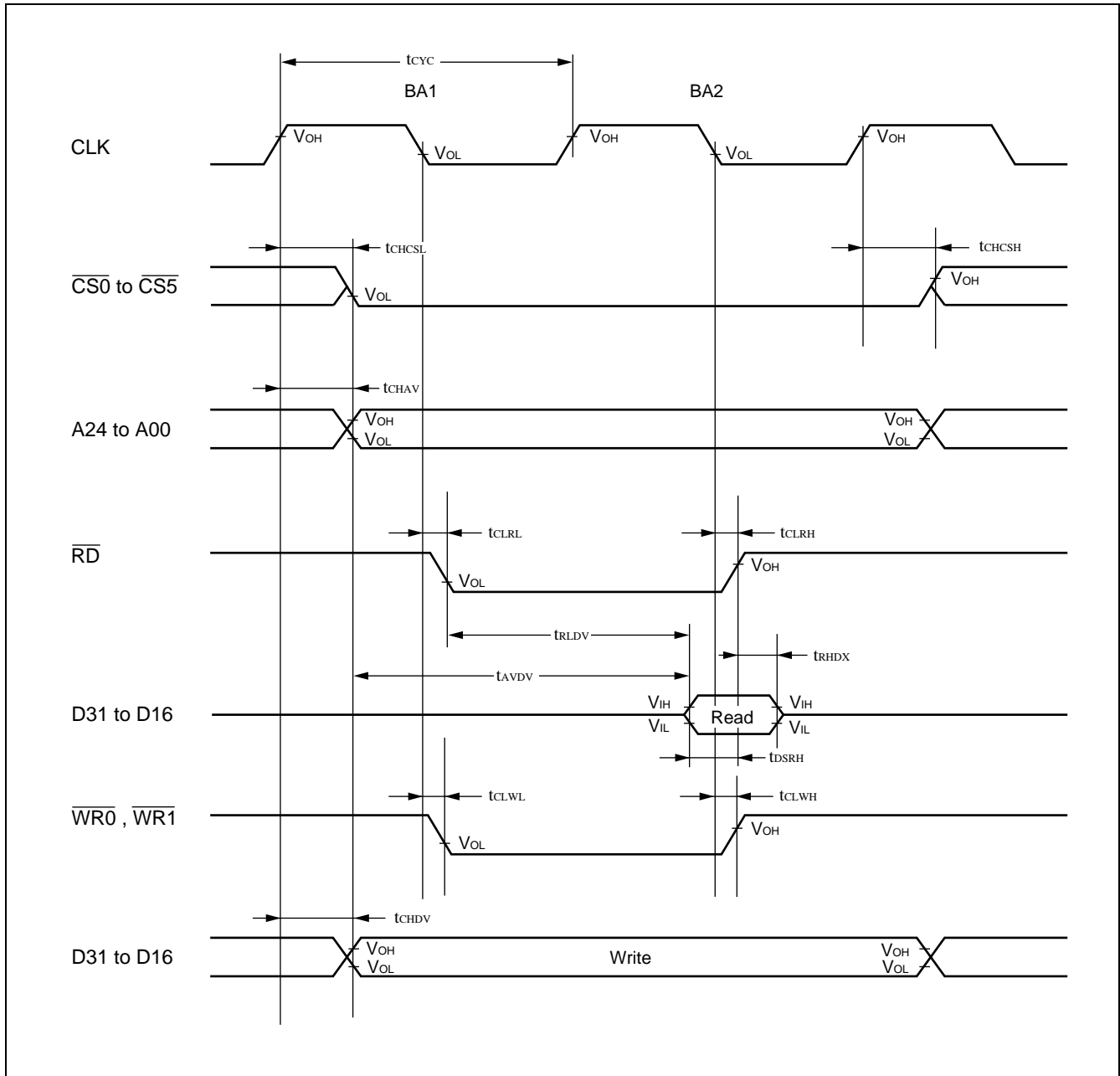
*1 : When bus timing is delayed by automatic wait insertion or RDY input, add ($t_{CYC} \times$ extended cycle number for delay) to this rating.

*2 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

$$\text{Equation : } (2 - n / 2) \times t_{CYC} - 40$$

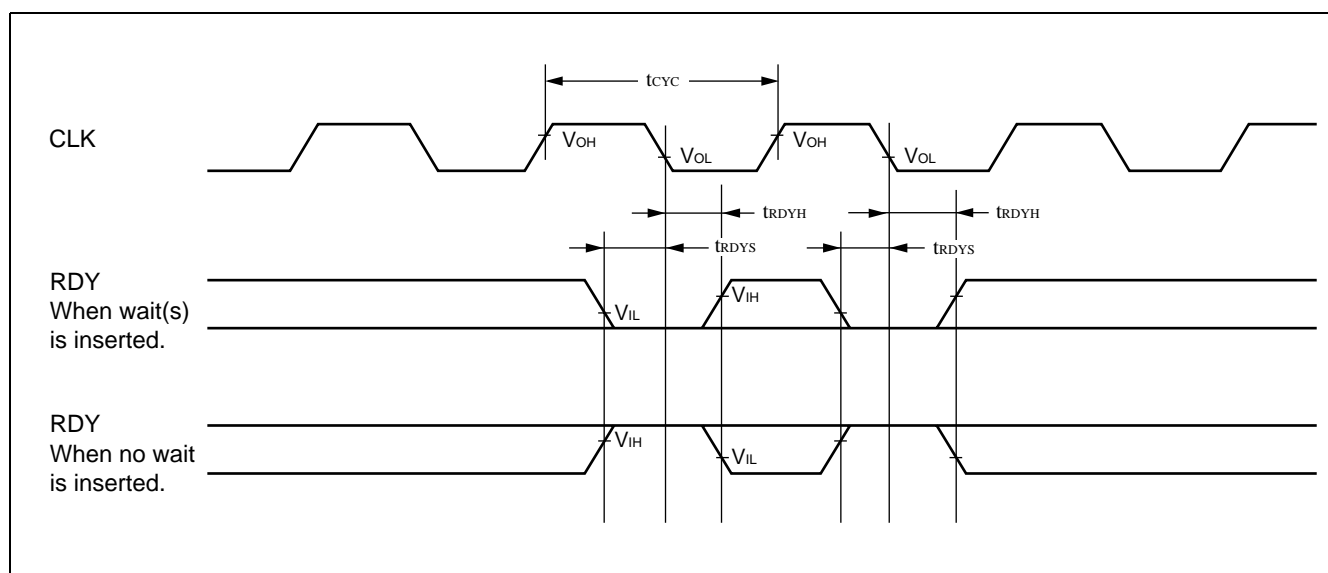
MB91121



(7) Ready Input Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY set up time \rightarrow CLK \downarrow	t_{RDYS}	RDY CLK	—	20	—	ns	
CLK \downarrow \rightarrow RDY hold time	t_{RDYH}	CLK RDY		0	—	ns	



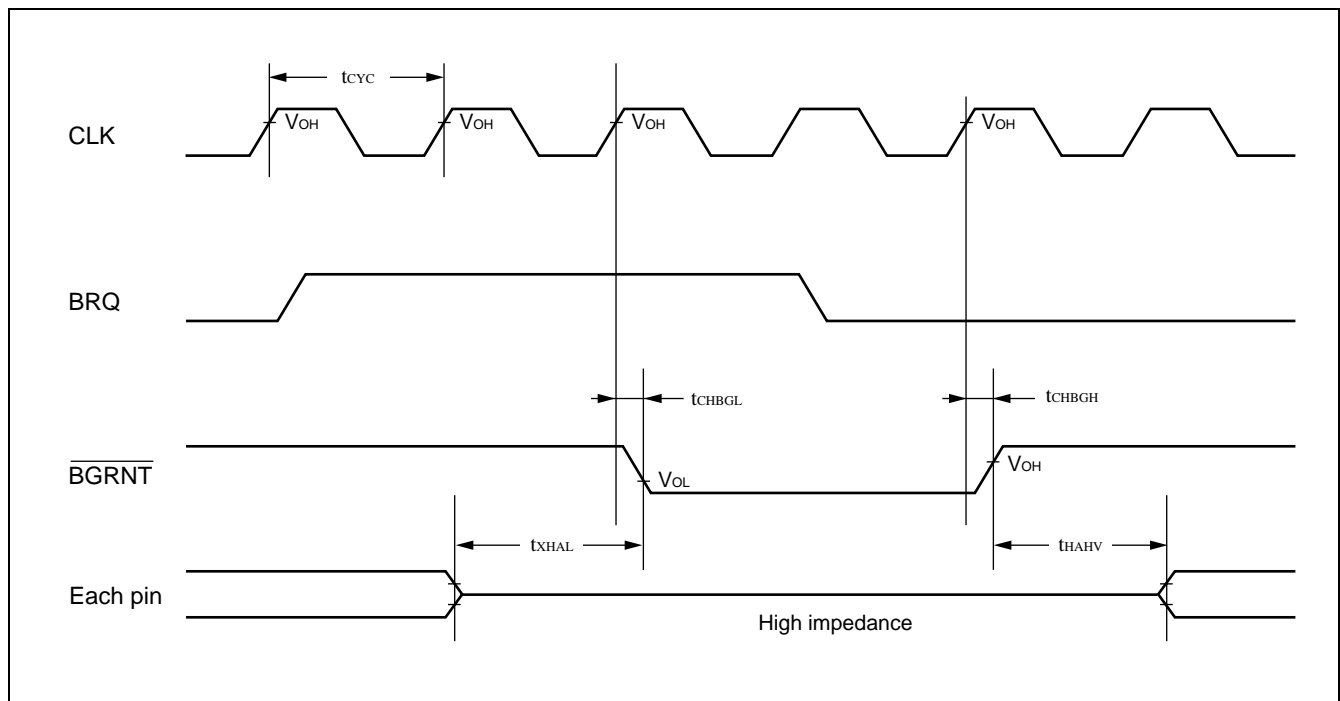
MB91121

(8) Hold Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	CLK	—	—	10	ns	
	t_{CHBGH}	$\overline{\text{BGRNT}}$		—	10	ns	
Pin floating $\rightarrow \overline{\text{BGRNT}}$ \downarrow time	t_{XHAL}	$\overline{\text{BGRNT}}$		$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	
$\overline{\text{BGRNT}}$ $\uparrow \rightarrow$ pin valid time	t_{HAHV}			$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	

Note : There is a delay time of more than 1 cycle from BRQ input to $\overline{\text{BGRNT}}$ change.



(9) Normal DRAM Mode Read/Write Cycle

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK	—	—	10	ns	
	t_{CHRAL}	RAS		—	10	ns	
CAS delay time	t_{CLCASL}	CLK		—	10	ns	
	t_{CLCASH}	CAS		—	10	ns	
ROW address delay time	t_{CHRAV}	CLK		—	15	ns	
COLUMN address delay time	t_{CHCAV}	A24 to A00		—	15	ns	
\overline{DW} delay time	t_{CHDWL}	CLK		—	15	ns	
	t_{CHDWH}	\overline{DW}		—	15	ns	
Output data delay time	t_{CHDV1}	CLK D31 to D16		—	15	ns	
RAS $\downarrow \rightarrow$ valid data input time	t_{RLDV}	RAS D31 to D16		—	$5 / 2 \times t_{CYC}$ – 20	ns	*1 *2
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV}	CAS		—	$t_{CYC} - 17$	ns	*1
CAS $\uparrow \rightarrow$ data hold time	t_{CADH}	D31 to D16		0	—	ns	

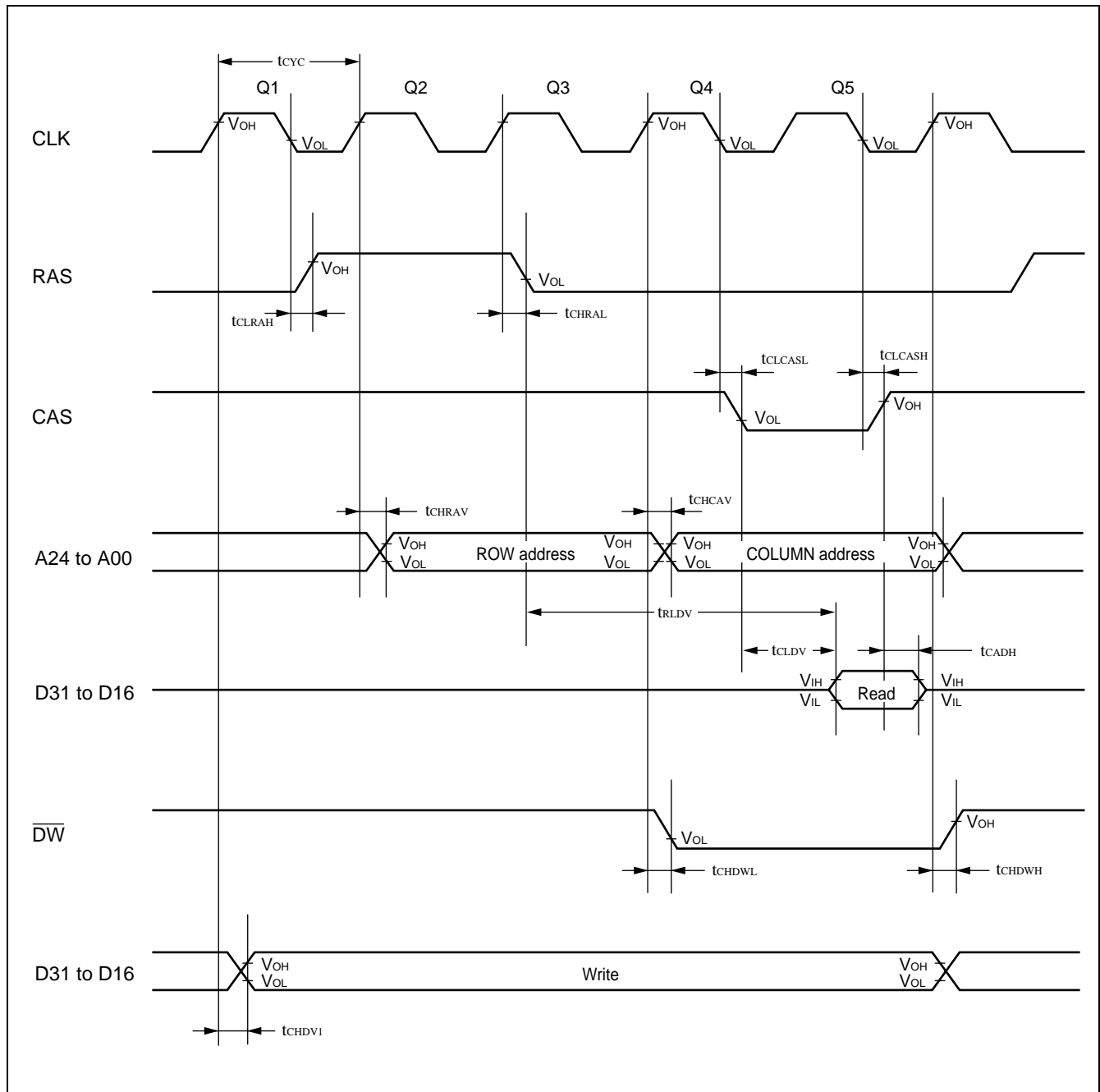
*1 : When Q1 cycle or Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

*2 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

$$\text{Equation : } (3 - n / 2) \times t_{CYC} - 20$$

MB91121



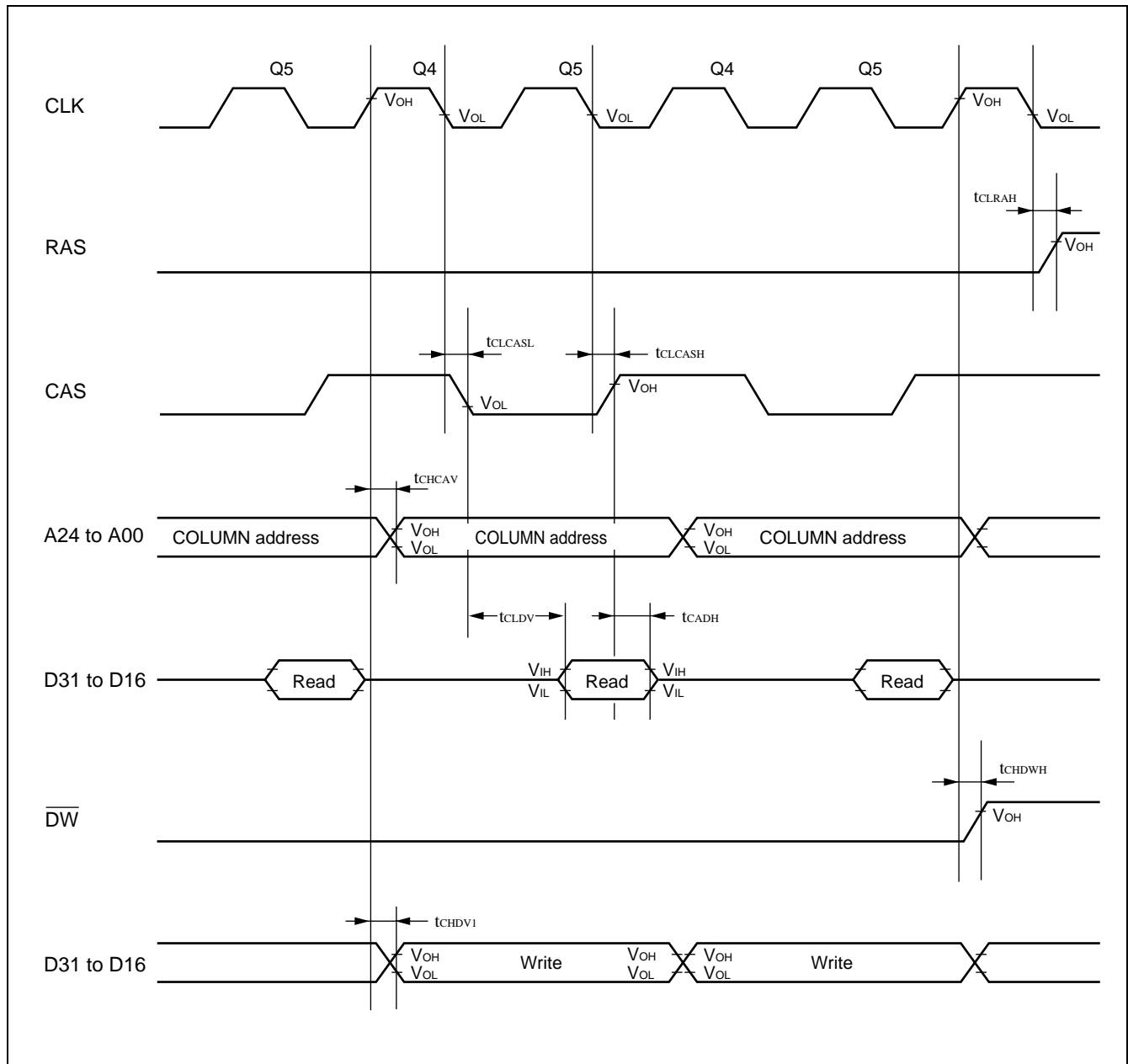
(10) Normal DRAM Mode Fast Page Read/Write Cycle

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	10	ns	
CAS delay time	t_{CLCASL}	CLK		—	10	ns	
	t_{CLCASH}	CAS		—	10	ns	
COLUMN address delay time	t_{CHCAV}	CLK A24 to A00		—	15	ns	
\overline{DW} delay time	t_{CHDWH}	CLK, \overline{DW}		—	15	ns	
Output data delay time	t_{CHDV1}	CLK D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV}	CAS		—	$t_{CYC} - 17$	ns	*
CAS $\uparrow \rightarrow$ data hold time	t_{CADH}	D31 to D16		0	—	ns	

* : When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

MB91121

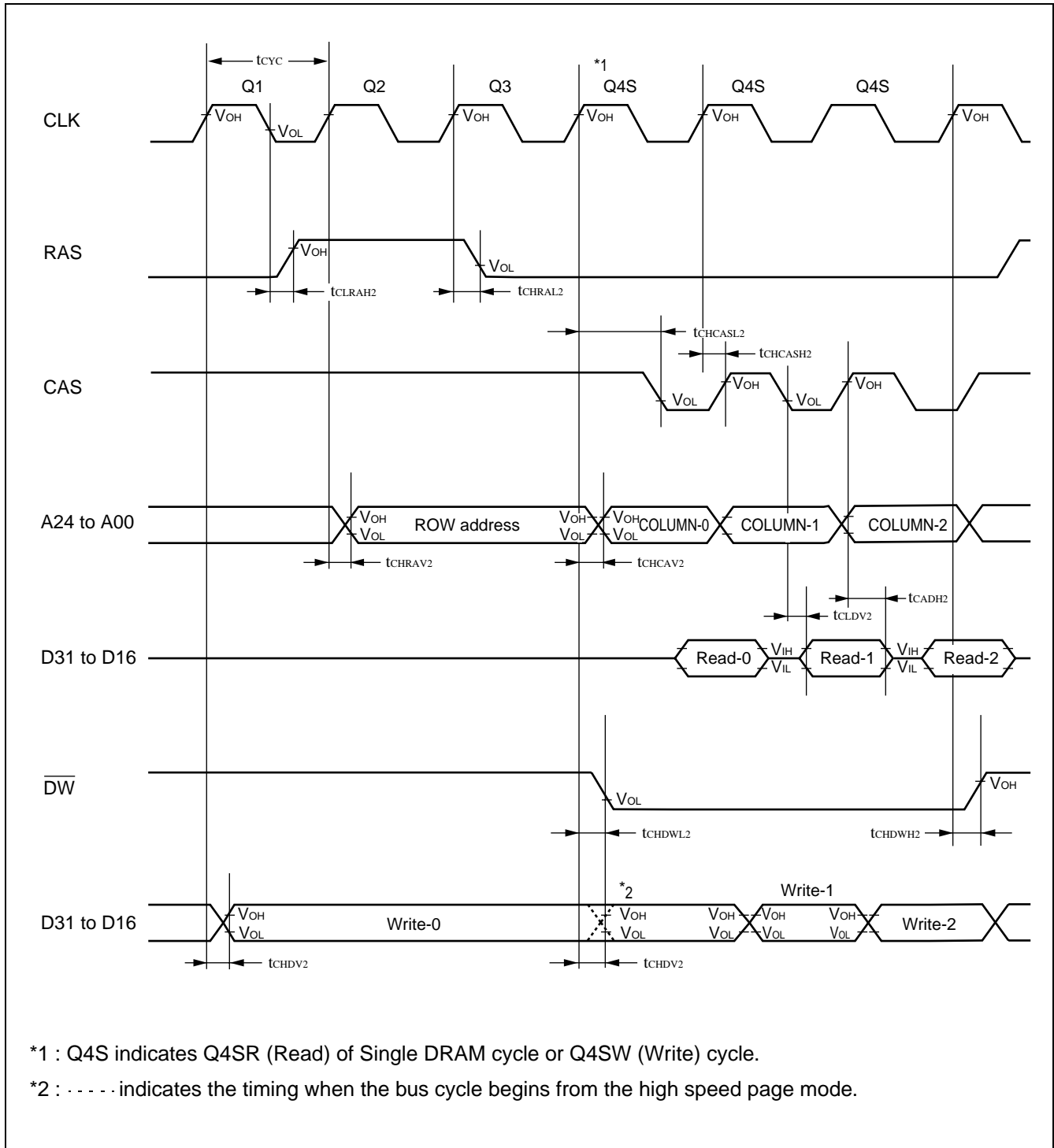


(11) Single DRAM Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH2}	CLK	—	—	10	ns	
	t_{CHRAL2}	RAS		—	10	ns	
CAS delay time	$t_{CHCASL2}$	CLK		—	$n / 2 \times t_{CYC}$	ns	
	$t_{CHCASH2}$	CAS		—	10	ns	
ROW address delay time	t_{CHRAV2}	CLK		—	15	ns	
COLUMN address delay time	t_{CHCAV2}	A24 to A00		—	15	ns	
\overline{DW} delay time	t_{CHDWL2}	CLK		—	15	ns	
	t_{CHDWH2}	\overline{DW}		—	15	ns	
Output data delay time	t_{CHDV2}	CLK		—	15	ns	
CAS $\downarrow \rightarrow$ Valid data input time	t_{CLDV2}	CAS		—	$(1 - n/2) \times t_{CYC} - 17$	ns	
CAS $\uparrow \rightarrow$ data hold time	t_{CADH2}	D31 to D16		0	—	ns	

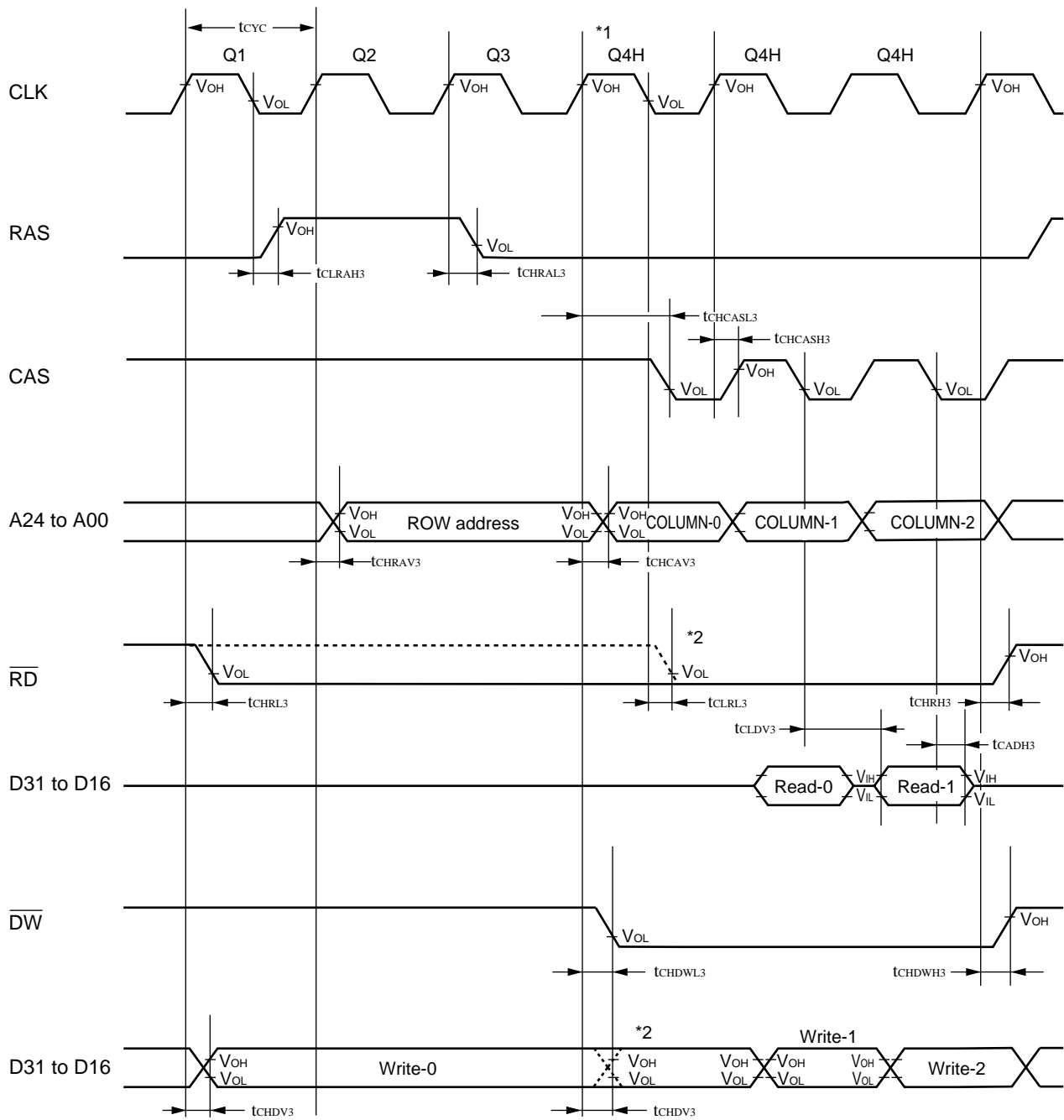
MB91121



(12) Hyper DRAM Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH3}	CLK	—	—	10	ns	
	t_{CHRAL3}	RAS		—	10	ns	
CAS delay time	$t_{CHCASL3}$	CLK		—	$n / 2 \times t_{CYC} + 8$	ns	
	$t_{CHCASH3}$	CAS		—	10	ns	
ROW address delay time	t_{CHRAV3}	CLK		—	15	ns	
COLUMN address delay time	t_{CHCAV3}	A24 to A00		—	15	ns	
$\overline{\text{RD}}$ delay time	t_{CHRL3}	CLK $\overline{\text{RD}}$		—	15	ns	
	t_{CHRH3}			—	15	ns	
	t_{CLRL3}			—	15	ns	
$\overline{\text{DW}}$ delay time	t_{CHDWL3}	CLK		—	15	ns	
	t_{CHDWH3}	$\overline{\text{DW}}$		—	15	ns	
Output data delay time	t_{CHDV3}	CLK D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV3}	CAS		—	$t_{CYC} - 20$	ns	
CAS $\downarrow \rightarrow$ data hold time	t_{CADH3}	D31 to D16		0	—	ns	



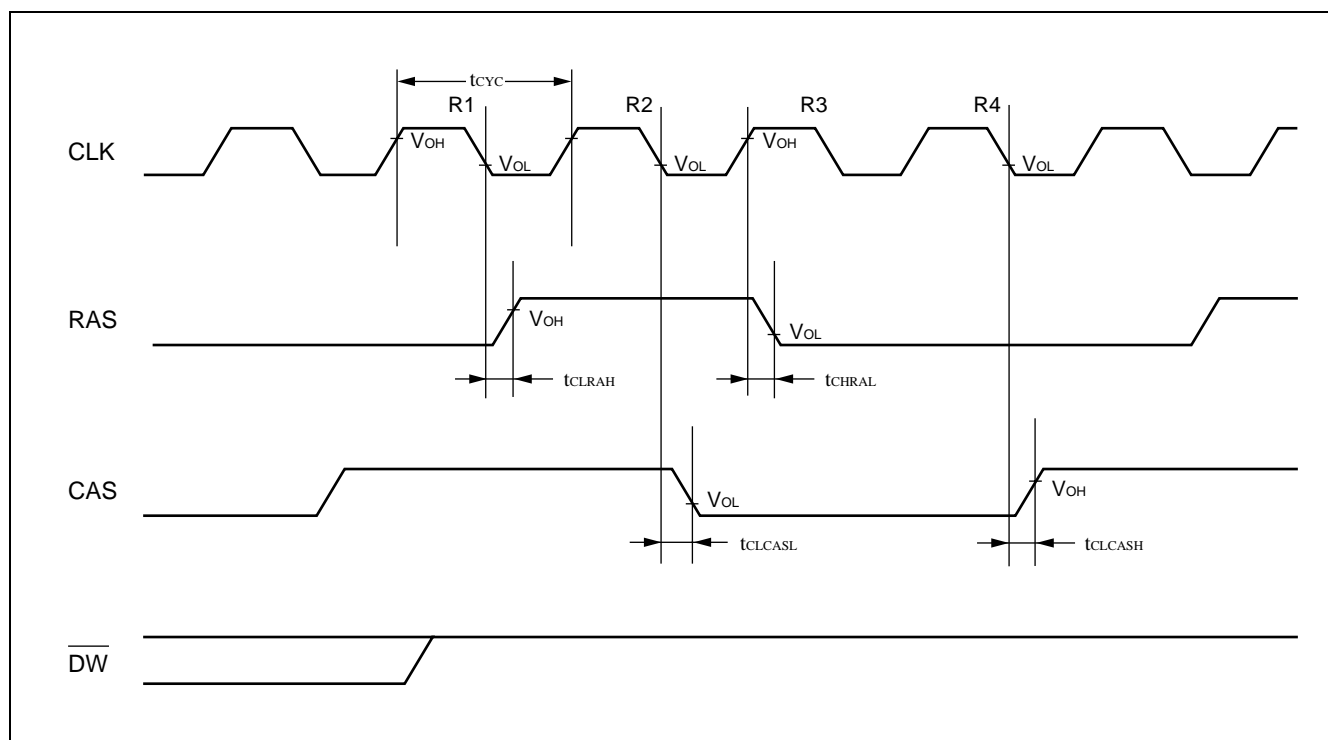
*1 : Q4H indicates Q4HR (Read) of Hyper DRAM cycle or Q4HW (Write) cycle.

*2 : indicates the timing when the bus cycle begins from the high speed page mode.

(13) CBR Refresh

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK	—	—	10	ns	
	t_{CHRAL}	RAS		—	10	ns	
CAS delay time	t_{CLCASL}	CLK		—	10	ns	
	t_{CLCASH}	CAS		—	10	ns	

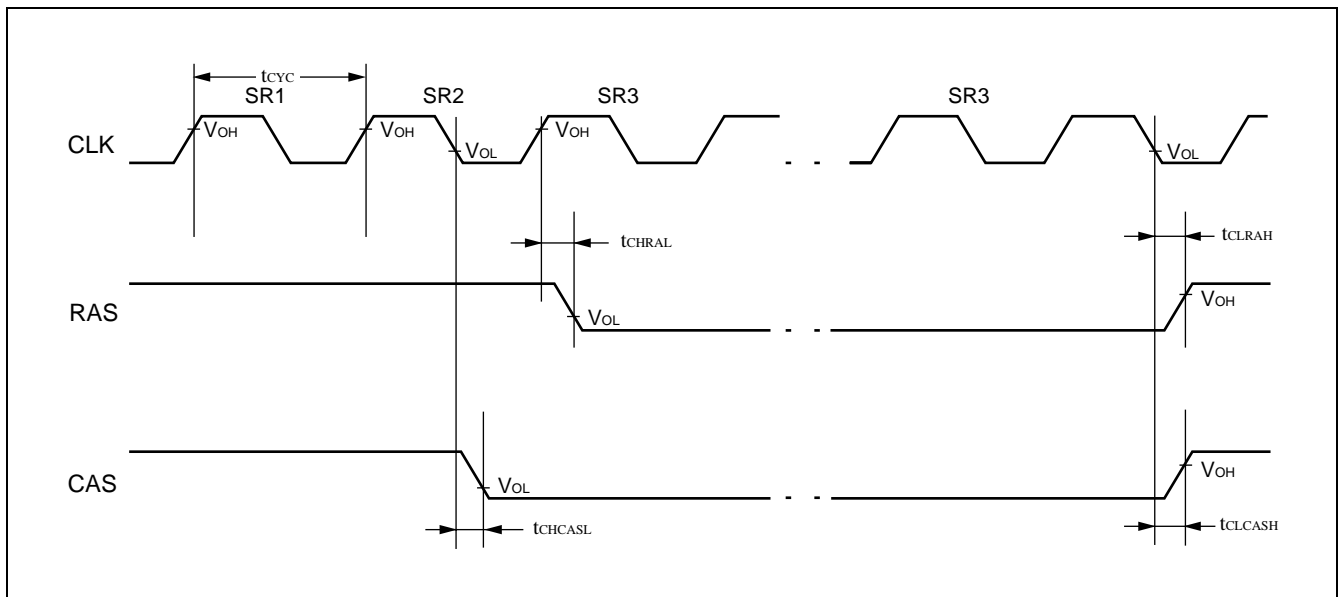


MB91121

(14) Self Refresh

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK	—	—	10	ns	
	t_{CHRAL}	RAS		—	10	ns	
CAS delay time	t_{CLCASL}	CLK		—	10	ns	
	t_{CLCASH}	CAS		—	10	ns	

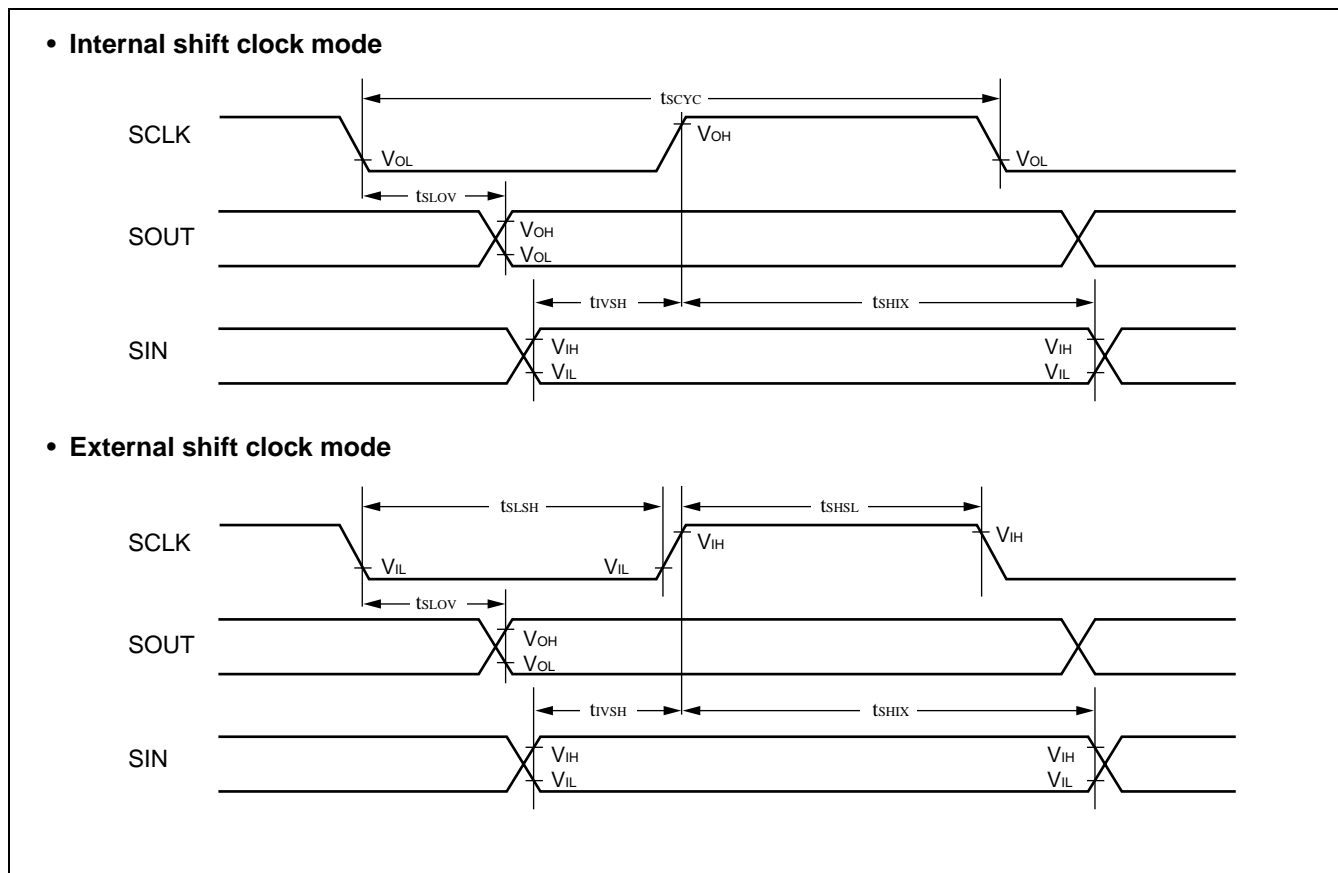


(15) UART Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SC0 to SC2	Internal shift clock mode	$8t_{CYCP}$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	SC0 to SC2 SO0 to SO2		-80	80	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{VSH}	SC0 to SC2 SI0 to SI2		100	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SC0 to SC2 SI0 to SI2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SC0 to SC2	External shift clock mode	$4t_{CYCP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SC0 to SC2		$4t_{CYCP}$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	SC0 to SC2 SO0 to SO2		—	150	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{VSH}	SC0 to SC2 SI0 to SI2		60	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SC0 to SC2 SI0 to SI2	60	—	ns		

Note : This rating is for AC characteristics in CLK synchronous mode.
 t_{CYCP} is a cycle time of peripheral system clock

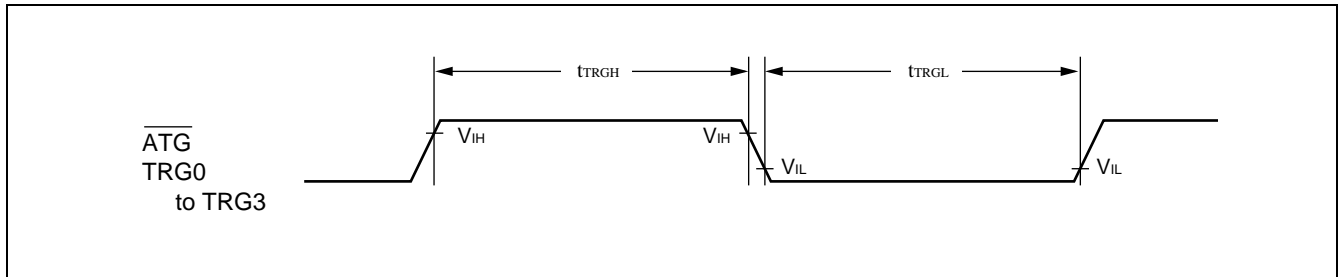


(16) Trigger System Input Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
A/D start trigger input time	t_{TRGH}	\overline{ATG}	—	$5t_{CYCP}$	—	ns	
External interrupt input time	t_{TRGL}	TRG0 to TRG3					

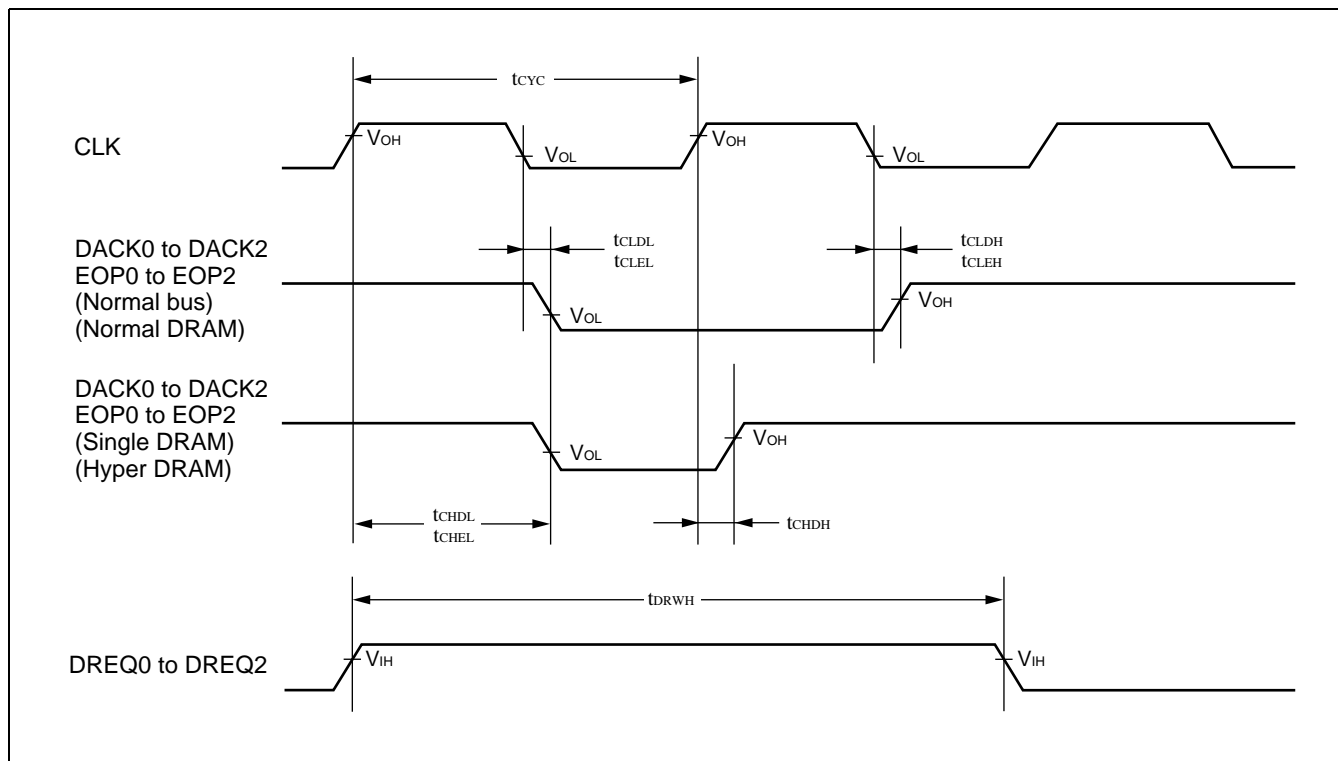
Note : t_{CYCP} is a cycle time of peripheral system clock



(17) DMA Controller Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	$2t_{CYC}$	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK DACK0 to DACK2		—	6	ns	
	t_{CLDH}	DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK EOP0 to EOP2		—	6	ns	
	t_{CLEH}	EOP0 to EOP2		—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK DACK0 to DACK2		—	$n / 2 \times t_{CYC}$	ns	
	t_{CHDH}	DACK0 to DACK2		—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK EOP0 to EOP2		—	$n / 2 \times t_{CYC}$	ns	
	t_{CHEH}	EOP0 to EOP2		—	6	ns	



5. A/D Converter Block Electrical Characteristics

($V_{CC} = AV_{CC} = AVRH = 3.3\text{ V}$, $AV_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	BIT
Total error	—	—	—	—	± 5.0	LSB
Linearity error	—	—	—	—	± 3.5	LSB
Differentiation linearity error	—	—	—	—	± 2.0	LSB
Zero transition voltage	V_{OT}	AN0 to AN7	-1.5	+0.5	+2.5	LSB
Full-scale transition voltage	V_{FST}	AN0 to AN7	$AVRH - 4.5$	$AVRH - 1.5$	$AVRH + 0.5$	LSB
Conversion time	—	—	5.6^{*1}	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	μA
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	$AVRH$	V
Reference voltage	—	$AVRH$	AV_{SS}	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	4	—	mA
	I_{AH}		—	—	5^{*2}	μA
Reference voltage supply current	I_R	$AVRH$	—	200	—	μA
	I_{RH}		—	—	5^{*2}	μA
Conversion variance between channels	—	AN0 to AN7	—	—	5	LSB

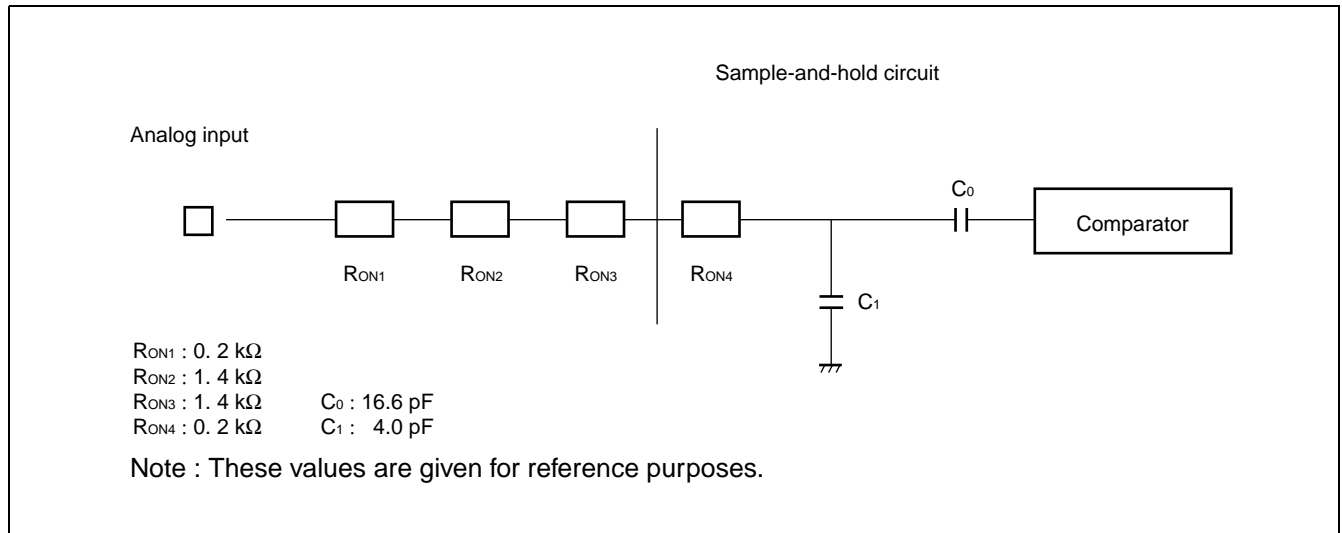
*1 : Machine clock = 25 MHz

*2 : Current value for A/D converters not in operation, CPU stop mode ($V_{CC} = AV_{CC} = AVRH = 3.3\text{ V}$)

Note :

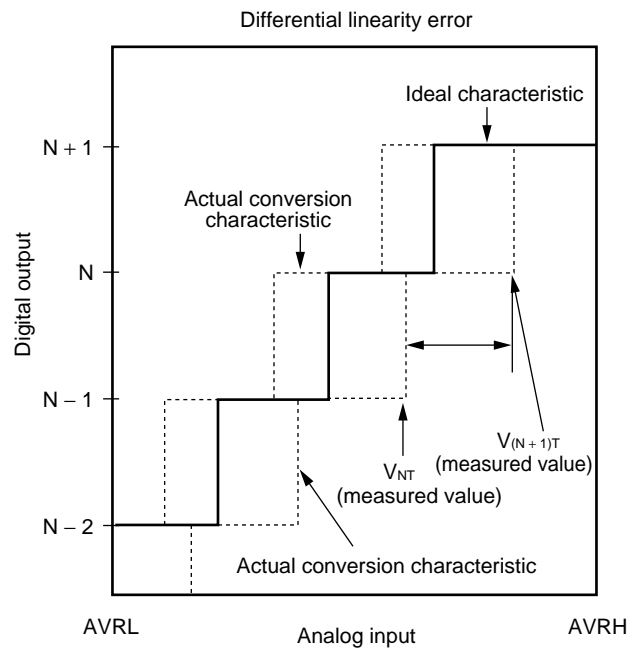
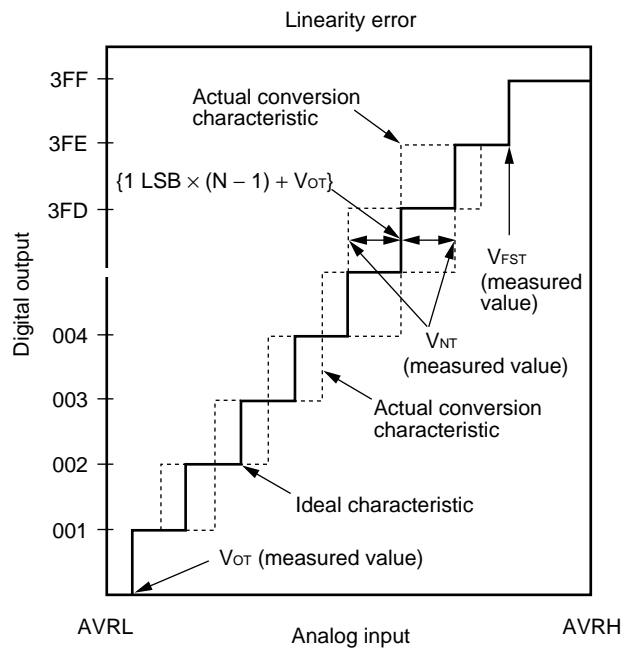
- As the absolute value of $AVRH$ decreases, relative error increases.
- Output impedance of external circuit of analog input under following conditions;
Output impedance of external circuit < 5 k Ω
If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling.

Analog input circuit example



6. A/D Converter Glossary

- Resolution
The smallest change in analog voltage detected by A/D converter.
- Linearity error
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”) .
- Differential linearity error
A deviation of a step voltage for changing the LSB of output code from ideal input voltage.



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

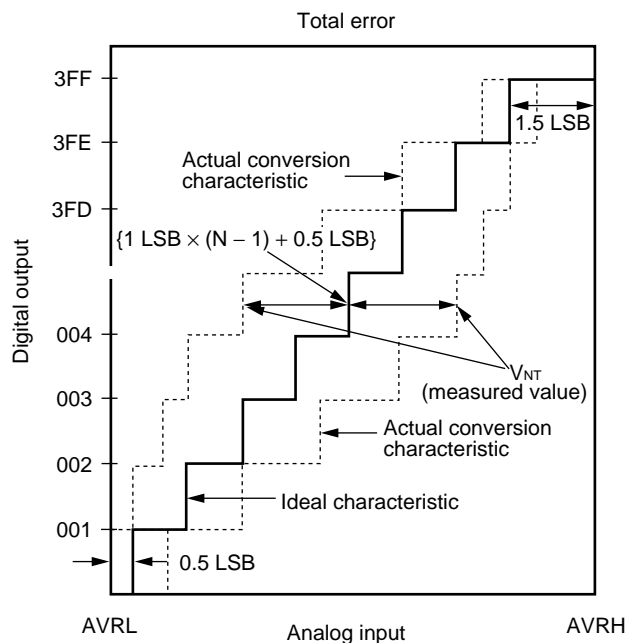
V_{OT} : A voltage for causing transition of digital output from (000)_H to (001)_H

V_{FST} : A voltage for causing transition of digital output from (3FE)_H to (3FF)_H

V_{NT} : A voltage for causing transition of digital output from (N - 1)_H to N

- Total error

A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

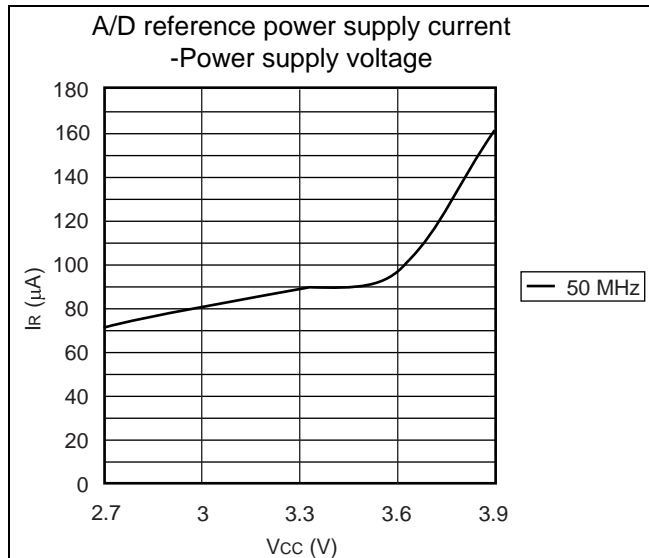
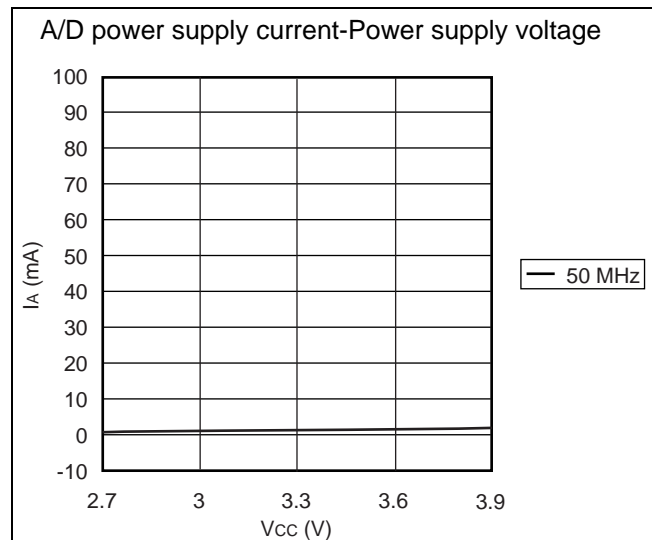
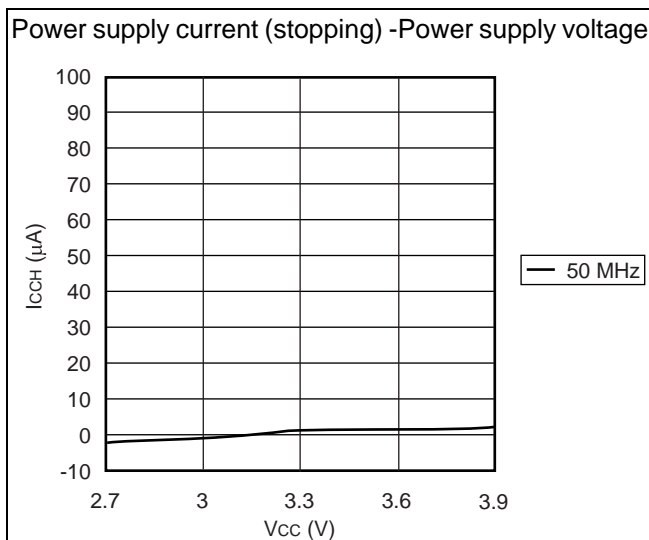
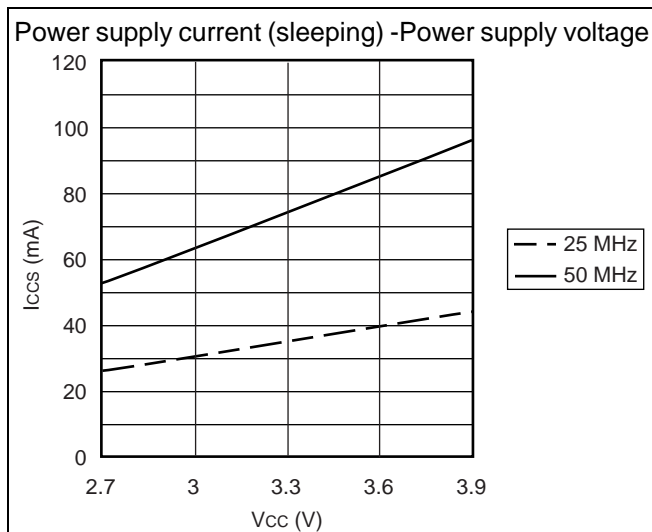
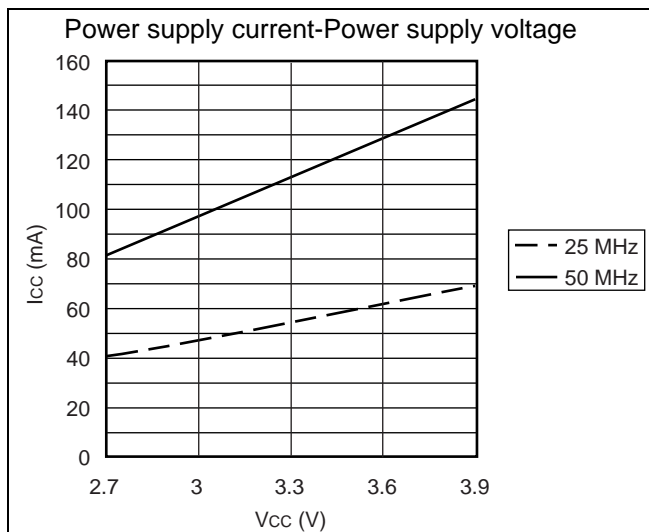
$$V_{OT} \text{ (ideal value)} = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (ideal value)} = AVRL - 1.5 \text{ LSB [V]}$$

V_{NT} : A voltage for causing transition of digital output from $(N - 1)$ to N

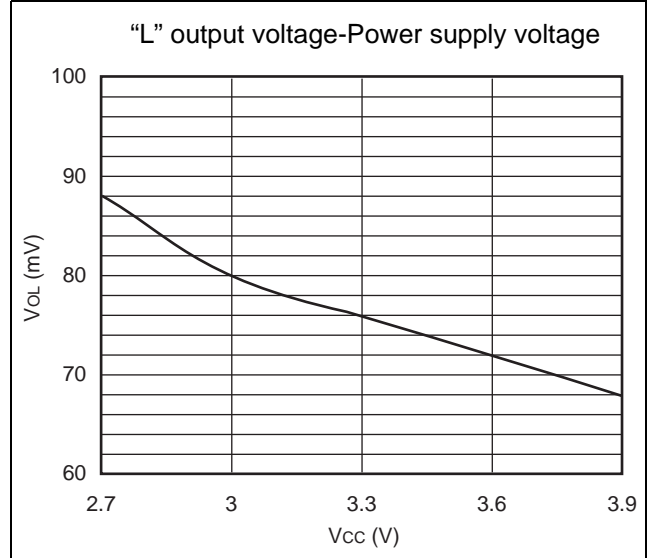
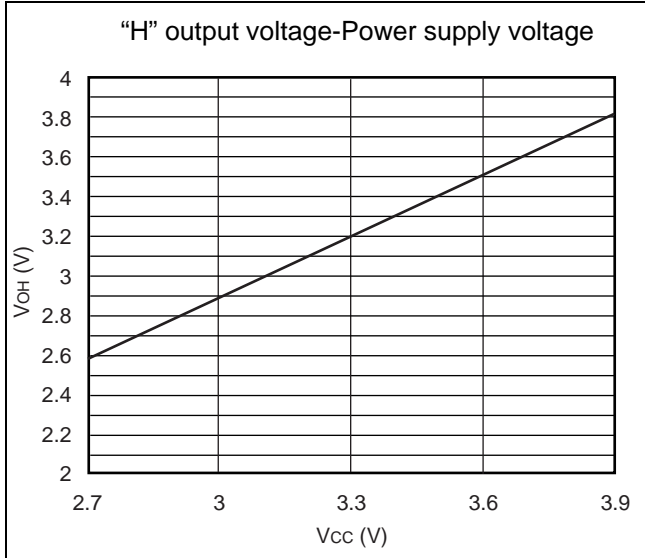
EXAMPLE CHARACTERISTICS

(1) Power Supply Current

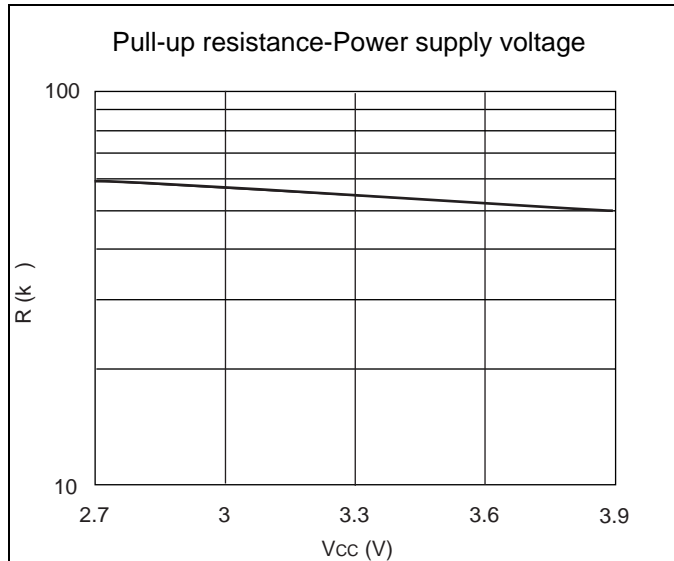


MB91121

(2) Output Voltage



(3) Pull-up Resistance



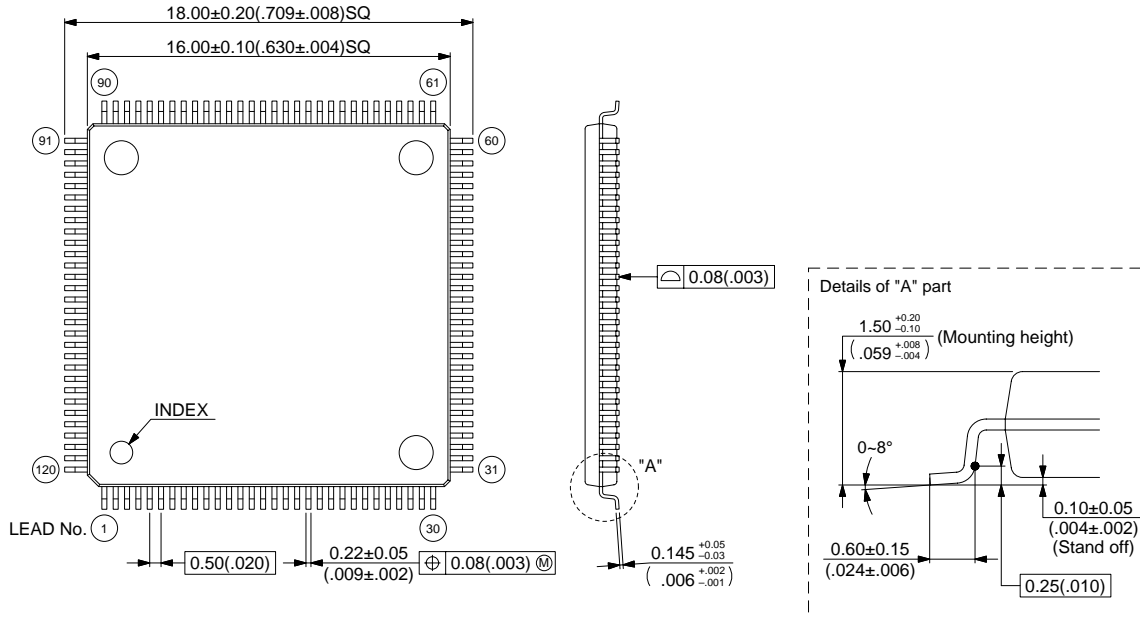
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91121PFV	120-pin Plastic LQFP (FPT-120P-M21)	

MB91121

■ PACKAGE DIMENSION

120-pin plastic LQFP
(FPT-120P-M21)



© 2001 FUJITSU LIMITED F120033S-c-3-3

Dimensions in mm (inches)

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.