NEC

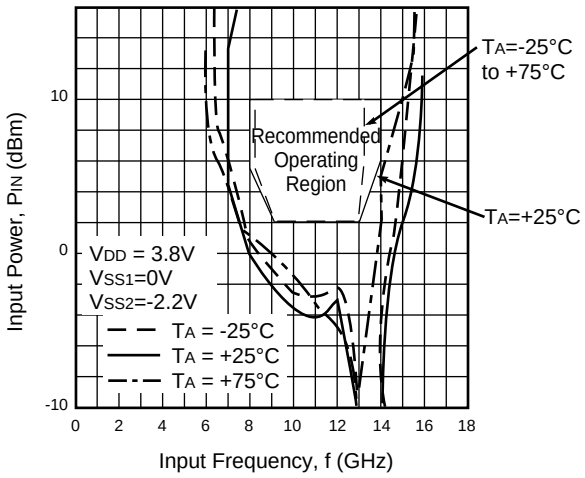
14 GHz DIVIDE-BY-8 DYNAMIC PRESCALER

UPG506B

FEATURES

- **WIDE OPERATING FREQUENCY RANGE:** f = 8 to 14 GHz (T_A = 25°C)
- **LOW PHASE NOISE**
- **GUARANTEED OPERATING TEMPERATURE RANGE** (T_A = -25°C to +75°C)

INPUT POWER vs. INPUT FREQUENCY



DESCRIPTION

The UPG506B is a GaAs divide-by-8 prescaler capable of operating up to 14 GHz. It is designed for use in frequency synthesizers of microwave communication systems and measurement equipment. The UPG506B is a dynamic frequency divider and employs BFL (Buffered FET Logic) circuits. The UPG506B is available in a hermetic 8-lead ceramic flat package.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = +3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V)

PART NUMBER PACKAGE OUTLINE			UPG506B BF08		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{DD}	Supply Current	mA	70	105	140
I_{SS1}	Sink Current[1] $I_{SS1} = I_{DD} - I_{SS2}$	mA		35	
I_{SS2}	Sink Current[1]	mA	44	70	96
$f_{IN(U)}$	Upper Limit of Input Frequency at P_{IN} = +6 dBm	GHz	14		
$f_{IN(L)}$	Lower Limit of Input Frequency at P_{IN} = +6 dBm	GHz			8
P_{IN}	Input Power at f = 9 to 13 GHz	dBm	2.0		10.0
P_{OUT}	Output Power at f_{IN} = 14 GHz	dBm	0	2.0	
$R_{TH(CH-C)}$	Thermal Resistance (Channel to Case)	°C/W		10.0	

Note:

1. Current is positive into the I_{DD} pin and returns through the I_{SS1} and I_{SS2} pins.

ELECTRICAL CHARACTERISTICS (T_A = -25°C to +75°C, V_{DD} = +3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V)

PART NUMBER PACKAGE OUTLINE			UPG506B BF08		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{DD}	Supply Current	mA		105	
I_{SS1}	Sink Current[1] $I_{SS1} = I_{DD} - I_{SS2}$	mA		35	
I_{SS2}	Sink Current[1]	mA		70	
$f_{IN(U)}$	Upper Limit of Input Frequency at P_{IN} = +6 dBm	GHz	13.2		
$f_{IN(L)}$	Lower Limit of Input Frequency at P_{IN} = +6 dBm	GHz			8.2
P_{IN}	Input Power at f = 9 to 13 GHz	dBm	2.0		10.0
P_{OUT}	Output Power at f_{IN} = 14 GHz	dBm	-1.0	1.0	

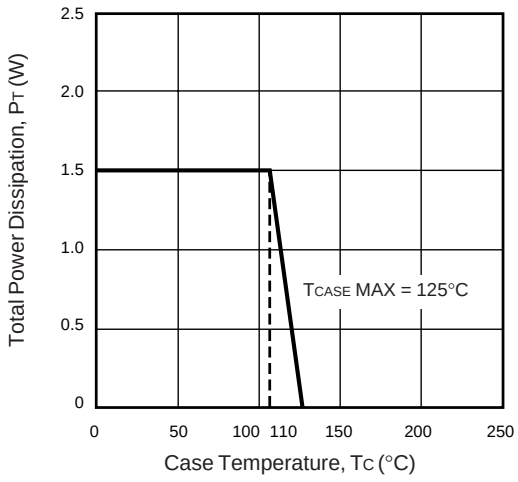
Note:
1. Current is positive into the I_{DD} pin and returns through the I_{SS1} and I_{SS2} pins.

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD} - V_{SS1}	Supply Voltage	V	5
V_{SS2} - V_{SS1}	Supply Current	mA	-5
P_T	Total Power Dissipation[2]	W	1.5
P_{IN}	Input Power Level	dBm	13
T_C	CaseTemperature	°C	-65 to +125
T_{STG}	Storage Temperature	°C	-65 to +175

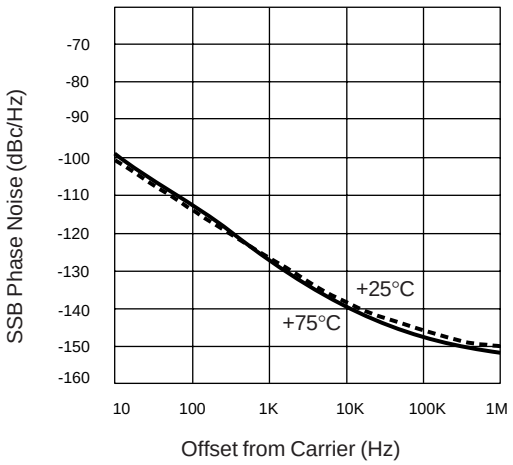
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. $T_C \leq 125^{\circ}C$.

POWER DERATING CURVES

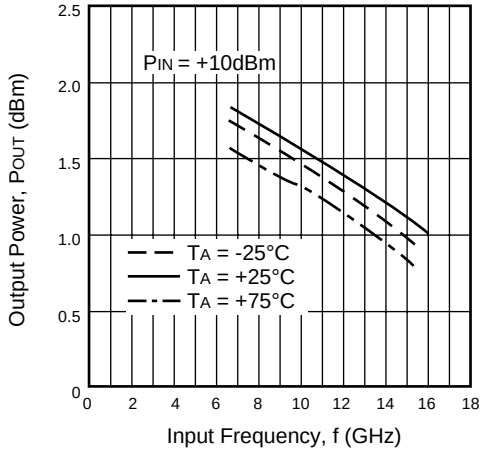


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

SSB PHASE NOISE vs. OFFSET FROM CARRIER
f_{IN} = 12.7 GHz

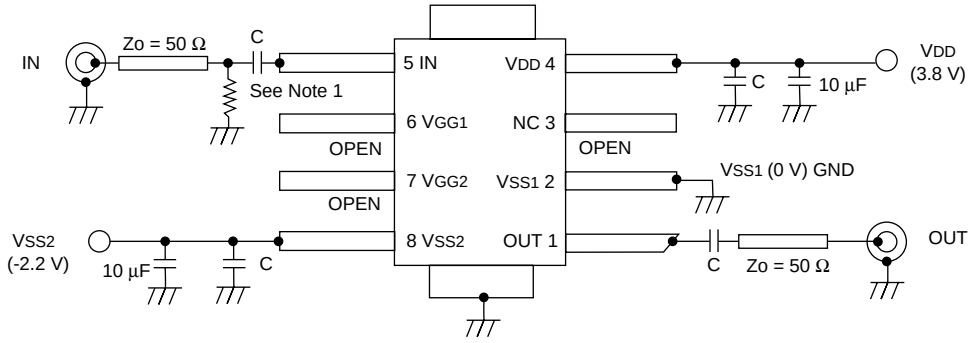


OUTPUT POWER vs. INPUT FREQUENCY



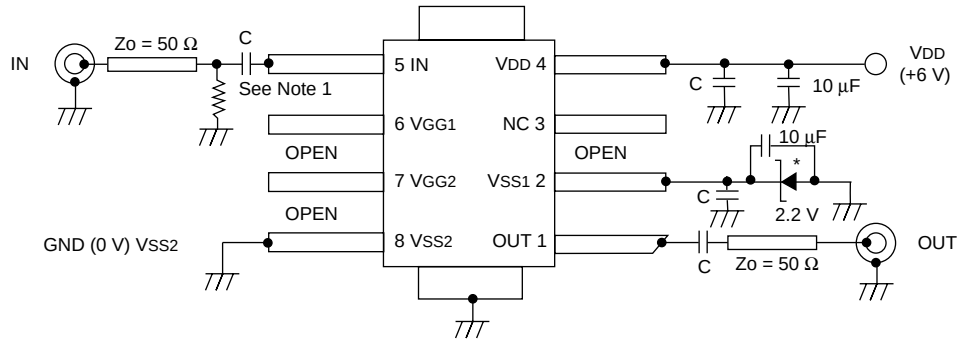
TEST CIRCUITS

CONFIGURATION 1
2 Bias Supply



VDD = 3.8 V
VSS1 = 0 V (GND)
VSS2 = –2.2 V
C: 1000 - 5000 pF Chip Capacitor

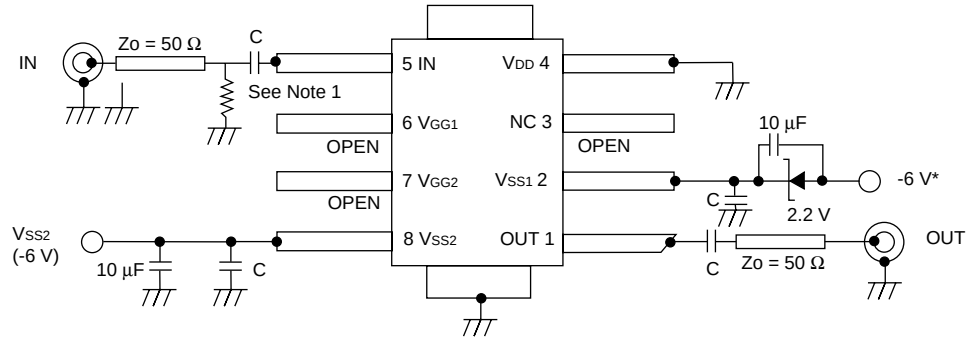
CONFIGURATION 2
Single Positive Bias Supply



VDD = +6.0 V
VSS2 = 0 V (GND)
C: 1000 - 5000 pF Chip Capacitor

* VSS1 should be connected to GND through a 2.2 V Zener Diode (RD2.2FB or IN3394).

CONFIGURATION 3
Single Negative Bias Supply



VDD = 0 V (GND)
VSS2 = –6 V
C: 1000 - 5000 pF Chip Capacitor

* For VSS1, the bias voltage of -6.0 should be applied through a 2.2 V Zener Diode (RD2.2FB or IN3394).

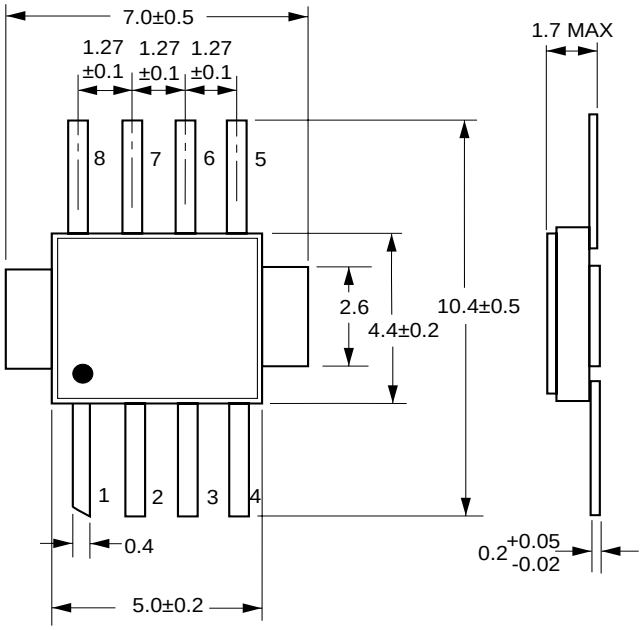
Notes:
1. Because of the high internal gain and gain compression of the UPG506B, the device is prone to self-oscillation in the absence of an RF input signal. This self-oscillation can be suppressed by either of the following means:

- Add a shunt resistor to the RF input line. Typically a resistor value between 50 and 1000 ohms will suppress the self-oscillation (see the test circuit schematic).
- Apply a negative voltage through a 1000 ohm resistor to the normally open VGG1 connection. Typically voltages between 0 and -9 volts will suppress the self-oscillation.

Both of these approaches will reduce the input sensitivity of the device (by as much as 3 dB for a 50 ohm shunt resistor), but otherwise have no effect on the reliability or electrical characteristics of the device.

OUTLINE DIMENSIONS (Units in mm)

UPG506B
PACKAGE OUTLINE BFO8



LEAD CONNECTIONS

1. OUTPUT	5. INPUT
2. V_{SS1}	6. V_{GG1}
3. NC*	7. V_{GG2}
4. V_{DD}	8. V_{SS2}

* No Connection