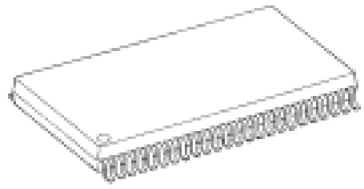
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCX164245FT

16-Bit Dual Supply Bus Transceiver



Weight: 0.25 g (typ.)

The TC74VCX164245FT is a dual supply, advanced high-speed CMOS 16-bit dual supply voltage interface bus transceiver fabricated with silicon gate CMOS technology.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 3.3-V or 2.5-V bus and a 2.5-V or 1.8-V bus in mixed 3.3-V or 2.5-V/2.5-V or 1.8-V supply systems.

The B-port interfaces with the 3.3-V or 2.5-V bus, the A-port with the 2.5-V or 1.8-V bus.

The direction of data transmission is determined by the level of the DIR input. The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

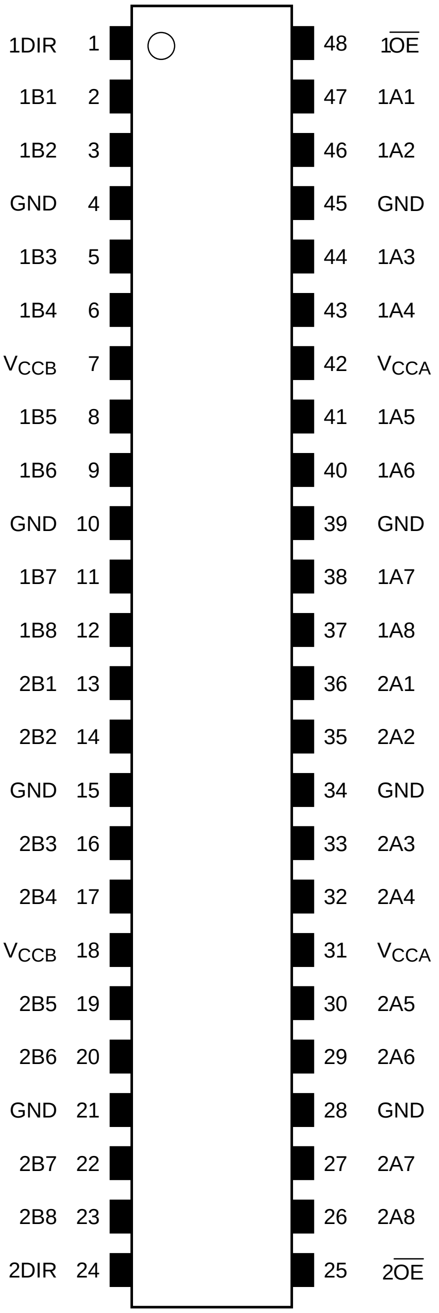
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

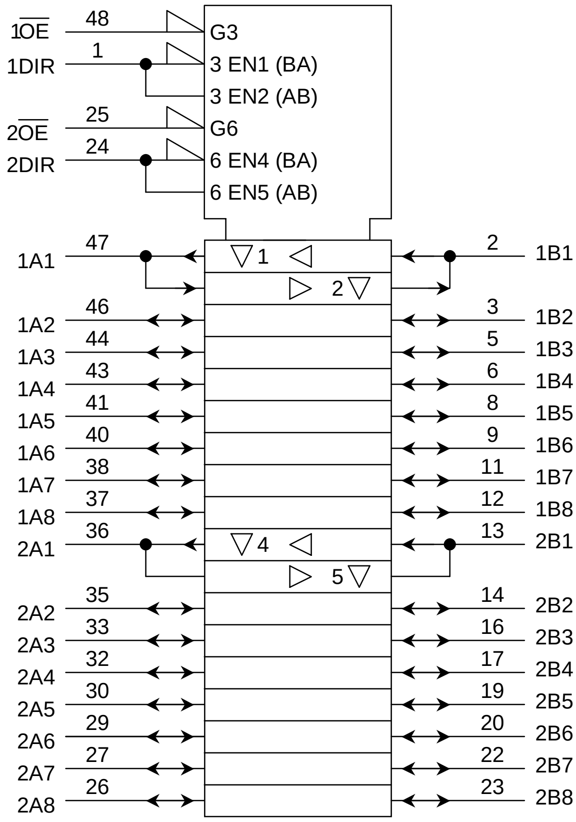
- Bidirectional interface between 3.3 V and 2.5 V, 3.3 V and 1.8 V, 2.5 V and 1.8 V
- High-speed: t_{pd} = 4.6 ns (max) (V_{CCB} = 3.3 ± 0.3 V, V_{CCA} = 2.5 ± 0.2 V)
  t_{pd} = 7.1 ns (max) (V_{CCB} = 3.3 ± 0.3 V, V_{CCA} = 1.8 ± 0.15 V)
  t_{pd} = 7.0 ns (max) (V_{CCB} = 2.5 ± 0.2 V, V_{CCA} = 1.8 ± 0.15 V)
- Output current: I_{OH}/I_{OL} = ±24 mA (min) (V_{CC} = 3.0 V)
  : I_{OH}/I_{OL} = ±18 mA (min) (V_{CC} = 2.3 V)
  : I_{OH}/I_{OL} = ±6 mA (min) (V_{CC} = 1.65 V)
- Latch-up performance: ±300 mA
- ESD performance: Machine model > ±200 V
  : Human body model > ±2000 V
- Package: TSSOP (thin shrink small outline package)
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Note 1: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

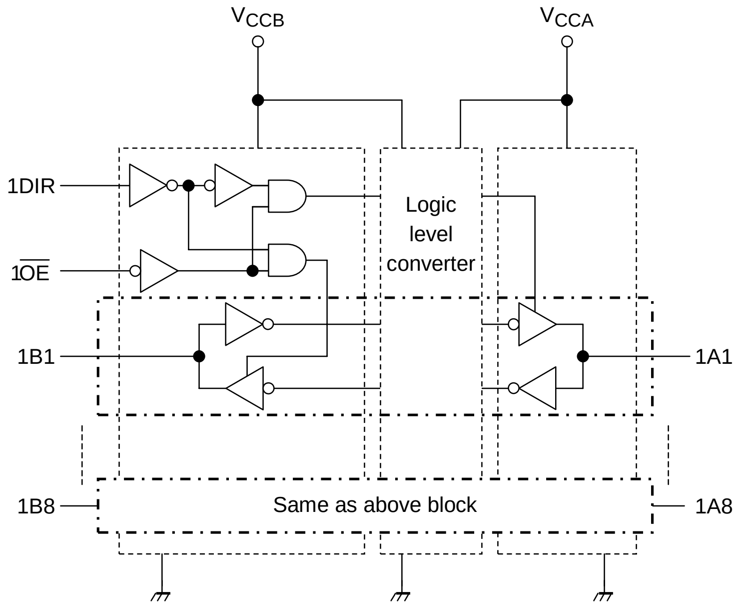
Inputs		Function		Outputs
$1\overline{OE}$	1DIR	Bus 1A1-1A8	Bus 1B1-1B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

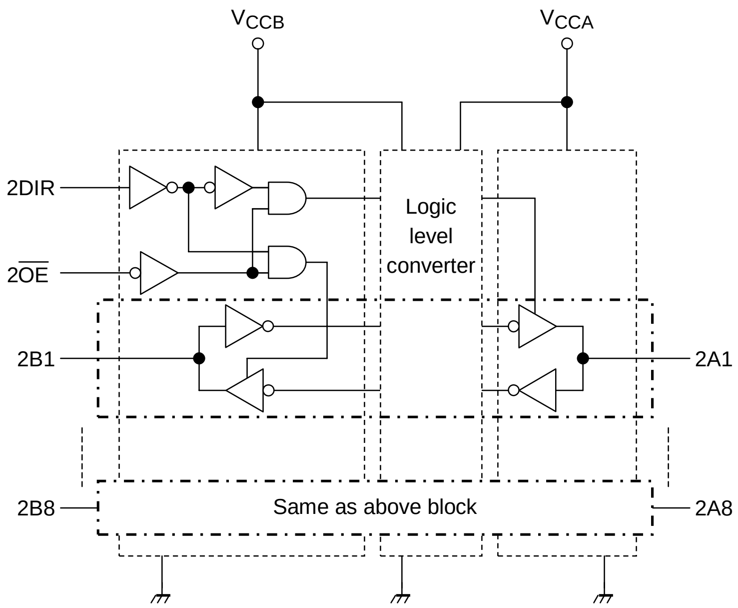
Inputs		Function		Outputs
$2\overline{OE}$	2DIR	Bus 2A1-2A8	Bus 2B1-2B8	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z		Z

X: Don’t care

Z: High impedance

Block Diagram





Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage (Note 2)	V_{CCB}	−0.5 to 4.6	V
	V_{CCA}	−0.5 to V_{CCB}	
DC input voltage (DIR, $\overline{OE}$)	V_{IN}	−0.5 to 4.6	V
DC bus I/O voltage	$V_{I/OB}$	−0.5 to 4.6 (Note 3)	V
		−0.5 to V_{CCB} + 0.5 (Note 4)	
	$V_{I/OA}$	−0.5 to 4.6 (Note 3)	
		−0.5 to V_{CCA} + 0.5 (Note 4)	
Input diode current	I_{IK}	−50	mA
Output diode current	$I_{I/OK}$	±50 (Note 5)	mA
DC output current	I_{OUTB}	±50	mA
	I_{OUTA}	±50	
DC V_{CC}/ground current per supply pin	I_{CCB}	±100	mA
	I_{CCA}	±100	
Power dissipation	P_D	400	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 2: $V_{CCB} > V_{CCA}$
Don't supply a voltage to V_{CCA} terminal when V_{CCB} is in the off-state.

Note 3: OFF state

Note 4: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 5: V_{OUT} < GND, $V_{OUT} > V_{CC}$

Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CCB}	2.3 to 3.6	V
	V_{CCA}	1.65 to 2.7	
Input voltage (DIR, $\overline{OE}$)	V_{IN}	0 to 3.6	V
Bus I/O voltage	$V_{I/OB}$	0 to 3.6 (Note 6)	V
		0 to V_{CCB} (Note 7)	
	$V_{I/OA}$	0 to 3.6 (Note 6)	
		0 to V_{CCA} (Note 7)	
Output current	I_{OUTB}	±24 (Note 8)	mA
		±18 (Note 9)	
	I_{OUTA}	±18 (Note 10)	
		±6 (Note 11)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 12)	ns/V

Note 6: Output in OFF state

Note 7: High or low state

Note 8: V_{CCB} = 3.0 to 3.6 V

Note 9: V_{CCA} = 2.3 to 2.7 V

Note 10: V_{CCA} = 2.3 to 2.7 V

Note 11: V_{CCA} = 1.65 to 1.95 V

Note 12: V_{INB} = 0.8 to 2.0 V, V_{CCB} = 3.0 V
V_{INA} = 0.7 to 1.6 V, V_{CCA} = 2.5 V

Electrical Characteristics

DC Characteristics (V_{CCB} = 3.3 ± 0.3 V, V_{CCA} = 2.5 ± 0.2 V)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
H-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		3.3 ± 0.3	2.5 ± 0.2	2.0	―	V
	V_{IHA}	An		3.3 ± 0.3	2.5 ± 0.2	1.6	―	
L-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		3.3 ± 0.3	2.5 ± 0.2	―	0.8	V
	V_{ILA}	An		3.3 ± 0.3	2.5 ± 0.2	―	0.7	
H-level output voltage	V_{OHB}	V_{IN} = V_{IH} or V_{IL}	I_{OHB} = −100 μA	3.3 ± 0.3	2.5 ± 0.2	V_{CCB} − 0.2	―	V
			I_{OHB} = −24 mA	3.0	2.5 ± 0.2	2.2	―	
	V_{OHA}		I_{OHA} = −100 μA	3.3 ± 0.3	2.5 ± 0.2	V_{CCA} − 0.2	―	
			I_{OHA} = −18 mA	3.3 ± 0.3	2.3	1.7	―	
L-level output voltage	V_{OLB}	V_{IN} = V_{IH} or V_{IL}	I_{OLB} = 100 μA	3.3 ± 0.3	2.5 ± 0.2	―	0.2	V
			I_{OLB} = 24 mA	3.0	2.5 ± 0.2	―	0.55	
	V_{OLA}		I_{OLA} = 100 μA	3.3 ± 0.3	2.5 ± 0.2	―	0.2	
			I_{OLA} = 18 mA	3.3 ± 0.3	2.3	―	0.6	
3-state output OFF state current	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		3.3 ± 0.3	2.5 ± 0.2	―	±10	μA
	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		3.3 ± 0.3	2.5 ± 0.2	―	±10	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		3.3 ± 0.3	2.5 ± 0.2	―	±5.0	μA
Power-off leakage current	I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	―	10	μA
Quiescent supply current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.3 ± 0.3	2.5 ± 0.2	―	20	μA
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.3 ± 0.3	2.5 ± 0.2	―	20	
	I_{CCB}	V_{CCB} < (V_{IN}, V_{OUT}) ≦ 3.6 V		3.3 ± 0.3	2.5 ± 0.2	―	±20	μA
	I_{CCA}	V_{CCA} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		3.3 ± 0.3	2.5 ± 0.2	―	±20	
	I_{CCTB}	V_{INB} = V_{CCB} − 0.6 V per input		3.3 ± 0.3	2.5 ± 0.2	―	750	μA
	I_{CCTA}	V_{INA} = V_{CCA} − 0.6 V per input		3.3 ± 0.3	2.5 ± 0.2	―	750	μA

DC Characteristics (V_{CCB} = 3.3 ± 0.3 V, V_{CCA} = 1.8 ± 0.15 V)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
H-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		3.3 ± 0.3	1.8 ± 0.15	2.0	—	V
	V_{IHA}	An		3.3 ± 0.3	1.8 ± 0.15	0.65 × V_{CC}	—	
L-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		3.3 ± 0.3	1.8 ± 0.15	—	0.8	V
	V_{ILA}	An		3.3 ± 0.3	1.8 ± 0.15	—	0.35 × V_{CC}	
H-level output voltage	V_{OHB}	V_{IN} = V_{IH} or V_{IL}	I_{OHB} = −100 μA	3.3 ± 0.3	1.8 ± 0.15	V_{CCB} − 0.2	—	V
			I_{OHB} = −24 mA	3.0	1.8 ± 0.15	2.2	—	
	V_{OHA}		I_{OHA} = −100 μA	3.3 ± 0.3	1.8 ± 0.15	V_{CCA} − 0.2	—	
			I_{OHA} = −6 mA	3.3 ± 0.3	1.65	1.25	—	
L-level output voltage	V_{OLB}	V_{IN} = V_{IH} or V_{IL}	I_{OLB} = 100 μA	3.3 ± 0.3	1.8 ± 0.15	—	0.2	V
			I_{OLB} = 24 mA	3.0	1.8 ± 0.15	—	0.55	
	V_{OLA}		I_{OLA} = 100 μA	3.3 ± 0.3	1.8 ± 0.15	—	0.2	
			I_{OLA} = 6 mA	3.3 ± 0.3	1.65	—	0.3	
3-state output OFF state current	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		3.3 ± 0.3	1.8 ± 0.15	—	±10	μA
	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		3.3 ± 0.3	1.8 ± 0.15	—	±10	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		3.3 ± 0.3	1.8 ± 0.15	—	±5.0	μA
Power-off leakage current	I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	10	μA
Quiescent supply current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.3 ± 0.3	1.8 ± 0.15	—	20	μA
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		3.3 ± 0.3	1.8 ± 0.15	—	20	
	I_{CCB}	V_{CCB} < (V_{IN}, V_{OUT}) ≦ 3.6 V		3.3 ± 0.3	1.8 ± 0.15	—	±20	μA
	I_{CCA}	V_{CCA} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		3.3 ± 0.3	1.8 ± 0.15	—	±20	
	I_{CCTB}	V_{INB} = V_{CCB} − 0.6 V per input		3.3 ± 0.3	1.8 ± 0.15	—	750	μA
	I_{CCTA}	V_{INA} = V_{CCA} − 0.6 V per input		3.3 ± 0.3	1.8 ± 0.15	—	750	μA

DC Characteristics (V_{CCB} = 2.5 ± 0.2 V, V_{CCA} = 1.8 ± 0.15 V)

Characteristics	Symbol	Test Condition		V_{CCB} (V)	V_{CCA} (V)	Ta = −40 to 85°C		Unit
						Min	Max	
H-level input voltage	V_{IHB}	DIR, $\overline{OE}$, Bn		2.5 ± 0.2	1.8 ± 0.15	1.6	—	V
	V_{IHA}	An		2.5 ± 0.2	1.8 ± 0.15	0.65 × V_{CC}	—	
L-level input voltage	V_{ILB}	DIR, $\overline{OE}$, Bn		2.5 ± 0.2	1.8 ± 0.15	—	0.7	V
	V_{ILA}	An		2.5 ± 0.2	1.8 ± 0.15	—	0.35 × V_{CC}	
H-level output voltage	V_{OHB}	V_{IN} = V_{IH} or V_{IL}	I_{OHB} = −100 μA	2.5 ± 0.2	1.8 ± 0.15	V_{CCB} − 0.2	—	V
			I_{OHB} = −18 mA	2.3	1.8 ± 0.15	1.7	—	
	V_{OHA}		I_{OHA} = −100 μA	2.5 ± 0.2	1.8 ± 0.15	V_{CCA} − 0.2	—	
			I_{OHA} = −6 mA	2.5 ± 0.2	1.65	1.25	—	
L-level output voltage	V_{OLB}	V_{IN} = V_{IH} or V_{IL}	I_{OLB} = 100 μA	2.5 ± 0.2	1.8 ± 0.15	—	0.2	V
			I_{OLB} = 18 mA	2.3	1.8 ± 0.15	—	0.6	
	V_{OLA}		I_{OLA} = 100 μA	2.5 ± 0.2	1.8 ± 0.15	—	0.2	
			I_{OLA} = 6 mA	2.5 ± 0.2	1.65	—	0.3	
3-state output OFF state current	I_{OZB}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.5 ± 0.2	1.8 ± 0.15	—	±10	μA
	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V		2.5 ± 0.2	1.8 ± 0.15	—	±10	
Input leakage current	I_{IN}	V_{IN} (DIR, $\overline{OE}$) = 0 to 3.6 V		2.5 ± 0.2	1.8 ± 0.15	—	±5.0	μA
Power-off leakage current	I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V		0	0	—	10	μA
Quiescent supply current	I_{CCB}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		2.5 ± 0.2	1.8 ± 0.15	—	20	μA
	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND		2.5 ± 0.2	1.8 ± 0.15	—	20	
	I_{CCB}	V_{CCB} < (V_{IN}, V_{OUT}) ≦ 3.6 V		2.5 ± 0.2	1.8 ± 0.15	—	±20	μA
	I_{CCA}	V_{CCA} ≦ (V_{IN}, V_{OUT}) ≦ 3.6 V		2.5 ± 0.2	1.8 ± 0.15	—	±20	
	I_{CCTB}	V_{INB} = V_{CCB} − 0.6 V per input		2.5 ± 0.2	1.8 ± 0.15	—	750	μA
	I_{CCTA}	V_{INA} = V_{CCA} − 0.6 V per input		2.5 ± 0.2	1.8 ± 0.15	—	750	μA

AC Characteristics (Ta = –40~85°C, Input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$)

$V_{CCB} = 3.3 \pm 0.3$ V, $V_{CCA} = 2.5 \pm 0.2$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	0.8	4.6	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	0.8	4.6	ns
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	0.8	4.4	ns
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	0.6	4.4	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	0.6	4.8	ns
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	0.8	4.8	ns
Output to output skew	t_{osLH} t_{osHL}	(Note 12)	—	0.5	ns

Note 12: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

$V_{CCB} = 3.3 \pm 0.3$ V, $V_{CCA} = 1.8 \pm 0.15$ V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.5	7.1	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.5	8.2	ns
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	0.8	4.5	ns
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	0.6	5.5	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	0.6	5.3	ns
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	0.8	5.6	ns
Output to output skew	t_{osLH} t_{osHL}	(Note 12)	—	0.5	ns

Note 12: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

V_{CCB} = 2.5 ± 0.2 V, V_{CCA} = 1.8 ± 0.15 V

Characteristics	Symbol	Test Condition	Min	Max	Unit
Propagation delay time (Bn → An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.5	7.0	ns
3-state output enable time ($\overline{OE}$ → An)	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.5	8.3	ns
3-state output disable time ($\overline{OE}$ → An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	0.8	4.6	ns
Propagation delay time (An → Bn)	t_{pLH} t_{pHL}	Figure 1, Figure 2	0.8	5.8	ns
3-state output enable time ($\overline{OE}$ → Bn)	t_{pZL} t_{pZH}	Figure 1, Figure 3	0.8	5.8	ns
3-state output disable time ($\overline{OE}$ → Bn)	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	0.8	5.2	ns
Output to output skew	t_{osLH} t_{osHL}	(Note 12)	—	0.5	ns

Note 12: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics (Ta = 25°C, Input: $t_r = t_f$ = 2.0 ns, C_L = 30 pF)

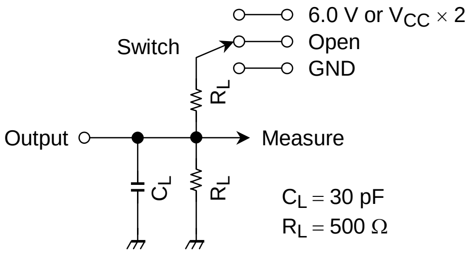
Characteristics		Symbol	Test Condition	V_{CCB} (V)	V_{CCA} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	B → A	V_{OLP}	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	1.8	0.25	V
				3.3	1.8	0.25	
				3.3	2.5	0.6	
	A → B			2.5	1.8	0.6	
				3.3	1.8	0.8	
				3.3	2.5	0.8	
Quiet output minimum dynamic V_{OL}	B → A	V_{OLV}	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	1.8	−0.25	V
				3.3	1.8	−0.25	
				3.3	2.5	−0.6	
	A → B			2.5	1.8	−0.6	
				3.3	1.8	−0.8	
				3.3	2.5	−0.8	
Quiet output minimum dynamic V_{OH}	B → A	V_{OHV}	$V_{IH} = V_{CC}$, V_{IL} = 0 V	2.5	1.8	1.3	V
				3.3	1.8	1.3	
				3.3	2.5	1.7	
	A → B			2.5	1.8	1.7	
				3.3	1.8	2.0	
				3.3	2.5	2.0	

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	V_{CCB} (V)	V_{CCA} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	DIR, $\overline{OE}$	3.3	2.5	7	pF
Output capacitance	$C_{I/O}$	—	An, Bn	3.3	2.5	8	pF
Power dissipation capacitance (Note 13)	C_{PDA}	—	A ⇒ B (DIR = “H”)	3.3	2.5	2	pF
			B ⇒ A (DIR = “L”)	3.3	2.5	33	
	C_{PDB}	—	A ⇒ B (DIR = “H”)	3.3	2.5	24	
			B ⇒ A (DIR = “L”)	3.3	2.5	3	

Note 13: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per bit)

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @V_{CC} = 3.3 ± 0.3 V V_{CC} × 2 @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 ± 0.15 V
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

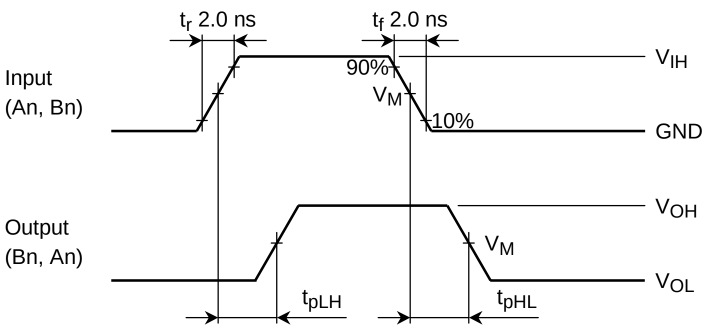


Figure 2 t_{pLH}, t_{pHL}

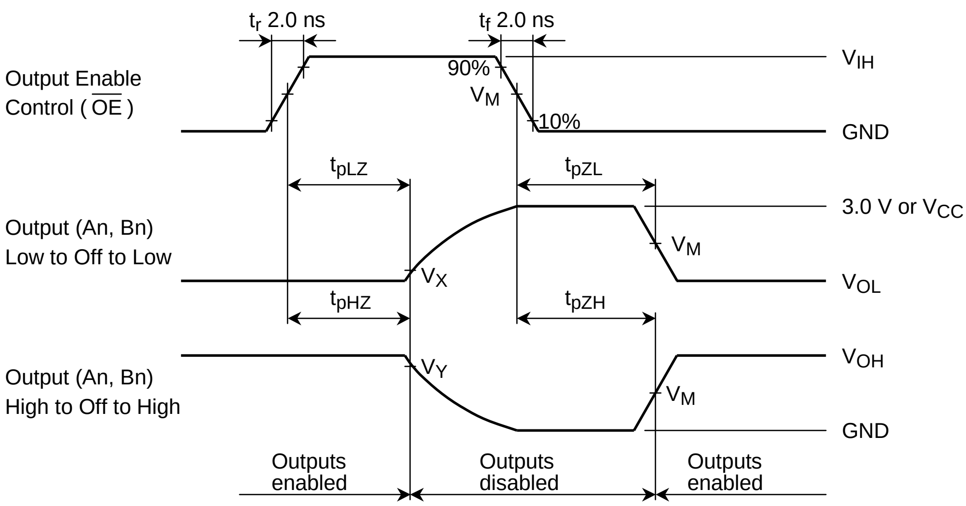
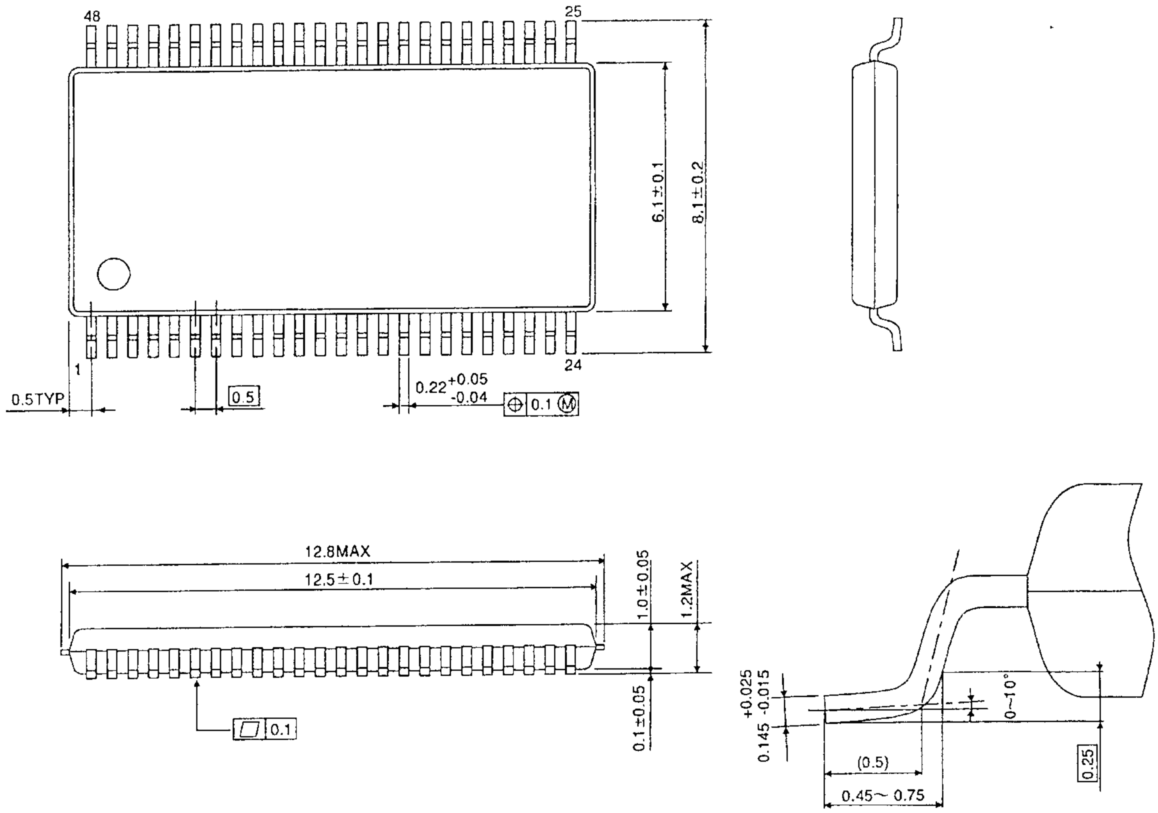


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 ± 0.15 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Package Dimensions

TSSOP48-P-0061-0.50 Unit : mm



Weight: 0.25 g (typ.)

RESTRICTIONS ON PRODUCT USE

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