UTC MJD210 PNP EPITAXIAL PLANAR SILICON TRANSISTOR

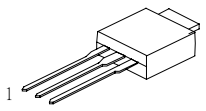
PNP SILICON DPAK FOR SURFACE MOUNT APPLICATIONS

DESCRIPTION

The UTC MJD210 is designed for low voltage, low-power, high-gain audio amplifier applications.

FEATURE

*Collector-Emitter Sustaining Voltage
V_{CEO}(sus) =25V (Min) @ I_C =10mA
*High DC Current Gain
h_{FE} =70 (Min) @ I_C=500mA
=45 (Min) @ I_C=2A
=10 (Min) @ I_C=5A
*Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
*Straight Lead Version in Plastic Sleeves ("-1" Suffix)
*Lead Formed Version in 16mm Tape and Reel ("T4" Suffix)
*Low Collector – Emitter Saturation Voltage
V_{CE}(sat) = 0.3V (Max) @ I_C =500mA
= 0.75V (Max) @ I_C = 2.0 A
*High Current-Gain-Bandwidth Product
f_T = 65 MHz (Min) @ I_C = 100 mA
*Annular Construction for Low Leakage
I_{CBO} = 100 nA @ Rated V_{CB}



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1: BASE 2: COLLECTOR 3: EMITTER

MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V_{CB}	40	V
Collector-Emitter Voltage	V_{CEO}	25	V
Emitter-Base Voltage	V_{EB}	7	V
Collector Current-Continuous	I_C	5	A
Peak		10	
Base Current	I_B	1	A
Total Device Dissipation @ T_C=25°C	P_D	12.5	W
Derate above 25°C		0.1	W/°C
Total Device Dissipation @ T_A=25°C*	P_D	1.4	W
Derate above 25°C		0.011	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W
Junction to Ambient*	$R_{\theta JA}$	89.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (note 1)	V_{CEO}(sus)	I_C=10mA, I_B=0	25	-	V
Collector Cutoff Current	I_{CBO}	V_{CB}=40V, I_E=0	-	100	nA
		V_{CB}=40V, I_E=0, T_J=125°C	-	100	nA
Emitter Cutoff Current	I_{EBO}	V_{BE}=7V, I_C=0	-	100	nA
ON CHARACTERISTICS					
DC Current Gain (note 2)	h_{FE}	I_C=500mA, V_{CE}=1V	70	-	
		I_C=2A, V_{CE}=1V	45	180	
		I_C=5A, V_{CE}=2V	10	-	
Collector-Emitter Saturation Voltage (note 2)	V_{CE}(sat)	I_C=500mA, I_B=50mA	-	0.3	V
		I_C=2A, I_B=200mA	-	0.75	
		I_C=5A, I_B=1A	-	1.8	
Base-Emitter Saturation Voltage (note 1)	V_{BE}(sat)	I_C=5A, I_B=1A	-	2.5	V
Base-Emitter On Voltage (note 1)	V_{BE}(on)	I_C=2A, V_{CE}=1V	-	1.6	V
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (note 3)	f_T	I_C=100mA, V_{CE}=10V, f_{test} = 10MHz	65		MHz
Output Capacitance	Cob	V_{CB}=10V, I_E=0, f=0.1MHz	-	120	pF

*When surface mounted on minimum pad sizes recommended. (continued)

NOTE 1: Pulse Test: Pulse Width = 300μs, Duty Cycle ≈ 2%.

NOTE 2: Pulse Test: Pulse Width = 300μs, Duty Cycle ≈ 2%.

NOTE 3: $f_T = |h_{fe}| \cdot f_{test}$.

FIG. 1 POWER DERATING

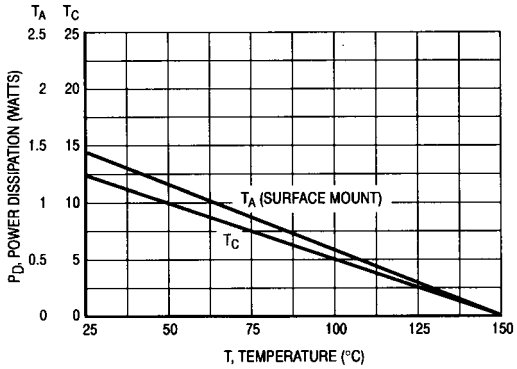
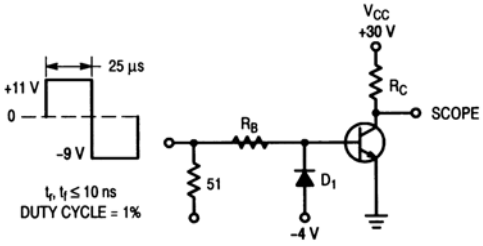


FIG. 2 SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS D1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$mA
FOR PNP TEST CIRCUIT
MSD6100 USED BELOW $I_B \approx 100$mA
REVERSE ALL POLARITIES

FIG. 3 TURN-ON TIME

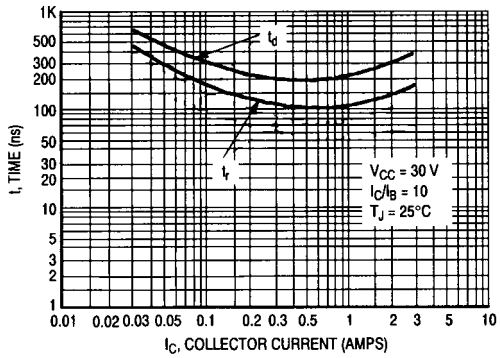


FIG. 4 TURN-OFF TIME

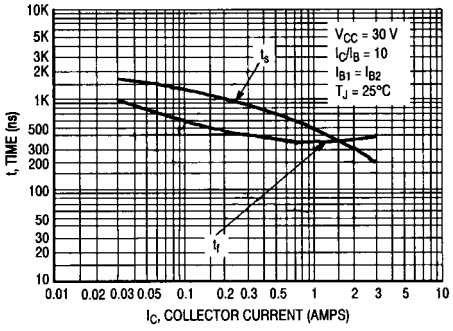


FIG. 5 DC CURRENT GAIN

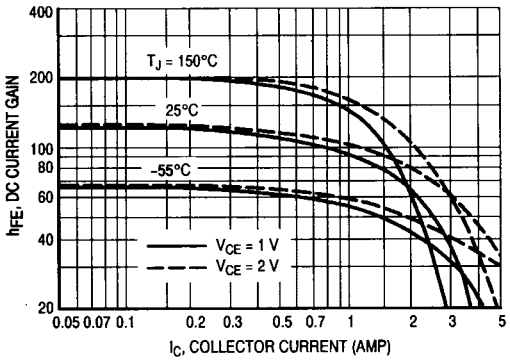


FIG. 6 "ON" VOLTAGE

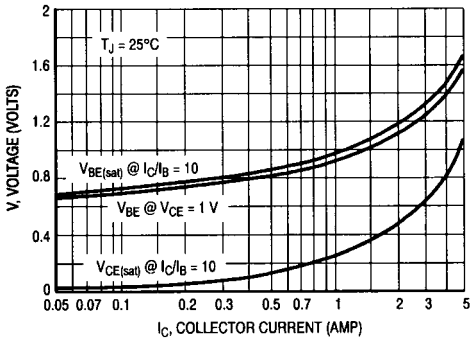


FIG. 7 TEMPERATURE CURRENT (AMP)

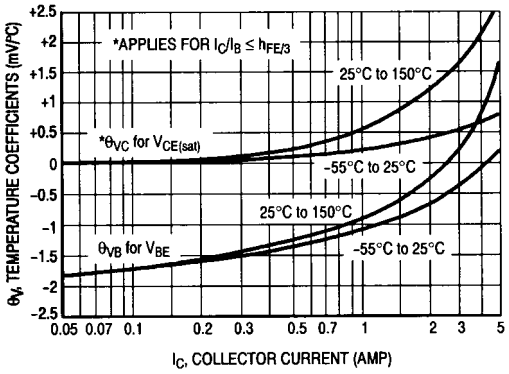


FIG. 8 THERMAL RESPONSE

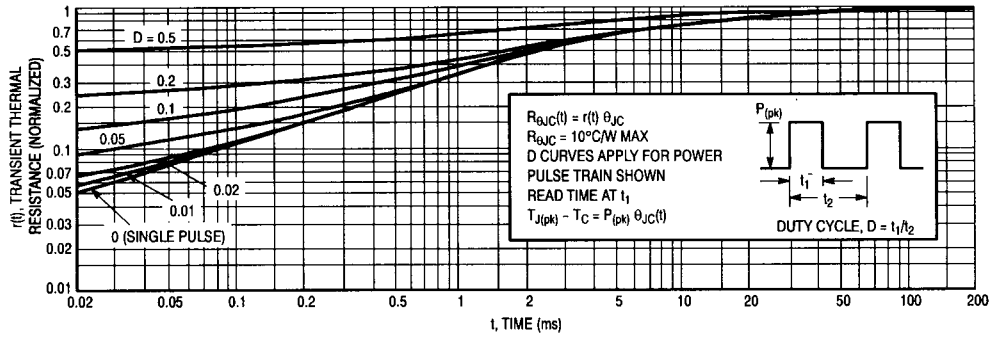
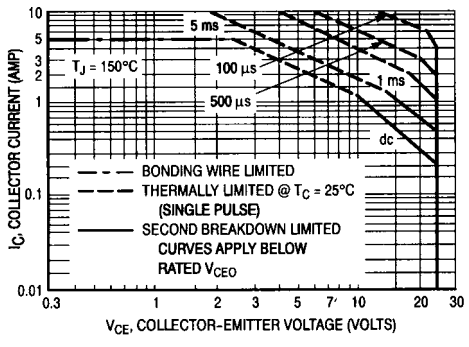


FIG. 9 ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 9 is based on $T_J(pk)$=150°C; Tc is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \le 150°C$. $T_J(pk)$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIG. 10 CAPACITANCE