

**ILA8138A**

**5.1V +12V REGULATOR WITH DISABLE AND RESET**

The ILA8138A is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included in all the versions.

- Output currents up to 1 A
- Fixed precision OUTPUT 1 voltages 5.1 V  $\pm$  2%
- Fixed precision OUTPUT 2 voltages 12 V  $\pm$  2%
- OUTPUT 1 with RESET facility
- OUTPUT 2 with DISABLE by TTL input
- Short circuit protection at both outputs
- Thermal protection
- Low drop output voltage



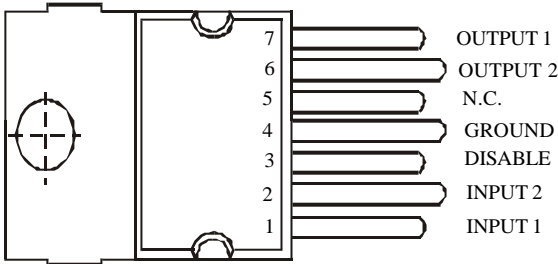
**TO-220AB/7  
HEPTAWAT**  
(Plastic Package)

**ORDERING INFORMATION**

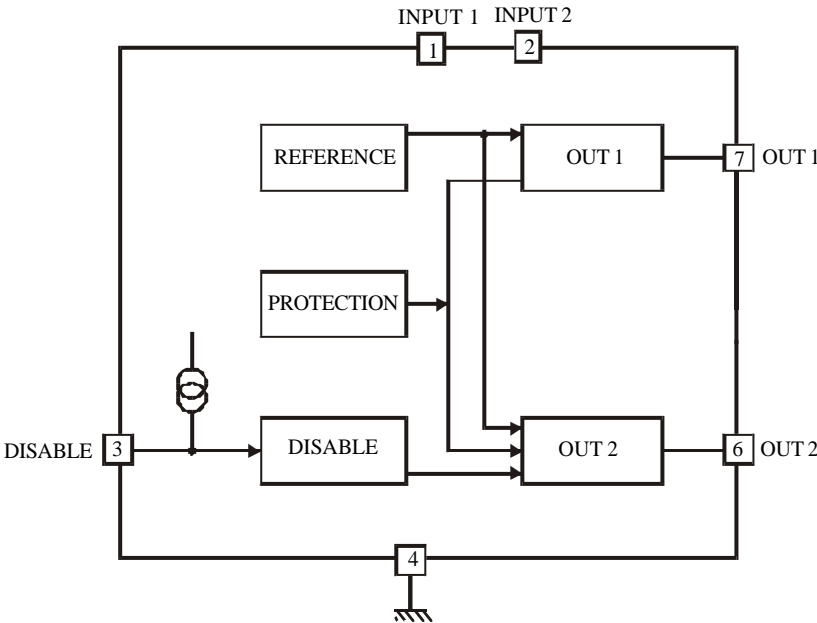
**ILA8138A** Plastic Package  
**IZ8138A** chip

$T_j = -0^\circ$  to  $130^\circ\text{C}$

**PIN ASSIGNMENT**



**BLOCK DIAGRAM**



**MAXIMUM RATINGS\***

Symbol	Parameter	Min	Max	Unit
V <sub>IN1</sub>	DC Input Voltage Pin 1	0	20	V
V <sub>IN2</sub>	DC Input Voltage Pin 2	0	20	V
V <sub>DIS</sub>	Disable Input Voltage Pin 3	0	20	V
I <sub>O1,2</sub>	Output Currents	0	1.6	A
T <sub>stg</sub>	Storage Temperature	-65	150	°C
T <sub>J</sub>	Junction Temperature	0	150	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>IN1</sub>	DC Input Voltage Pin 1	7.0	16	V
V <sub>IN2</sub>	DC Input Voltage Pin 2	14	18	V
V <sub>DIS</sub>	Disable Input Voltage Pin 3	0	7.0	V
I <sub>O1,2</sub>	Output Currents	0	1.6	A
T <sub>J</sub>	Junction Temperature	0	130	°C

**THERMAL DATA**

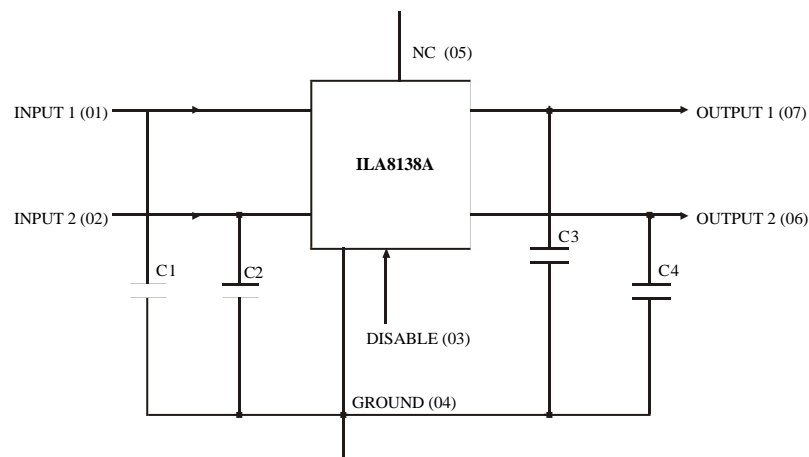
Symbol	Parameter	Value	Unit
R <sub>th(j-c)</sub>	Maximum Thermal Resistance Junction-case	6	°C/W
R <sub>th(j-a)</sub>	Maximum Thermal Resistance Junction-ambient	60	°C/W

**ELECTRICAL CHARACTERISTICS** ( $V_{IN1} = 7\text{ V}$ ,  $V_{IN2} = 14\text{ V}$ ,  $T_j = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
$V_{O1}$	Output Voltage	$V_{IN1} = 7\text{ V}$ , $I_{O1} = -10\text{ mA}$	5.0	5.2	V
$V_{O2}$		$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$ , $I_{O2} = -10\text{ mA}$	11.76	12.24	V
$V_{O1}$		$-5\text{ mA} \leq I_{O2} \leq -750\text{ mA}$ , $7\text{ V} \leq V_{IN1} \leq 14\text{ V}$	4.9	5.3	V
$V_{O2}$		$-5\text{ mA} \leq I_{O2} \leq -750\text{ mA}$ , $14\text{ V} \leq V_{IN2} \leq 18\text{ V}$ , $V_{IN1} = 7\text{ V}$	11.5	12.5	V
$\Delta V_{O1\text{ LI}}$	Line Regulation	$7\text{ V} \leq V_{IN2} \leq 14\text{ V}$ , $I_{O1} = -200\text{ mA}$		50	mV
$\Delta V_{O2\text{ LI}}$		$14\text{ V} \leq V_{IN2} \leq 18\text{ V}$ , $I_{O1} = -200\text{ mA}$ , $V_{IN1} = 7\text{ V}$		120	
$\Delta V_{O1\text{ LO}}$	Load Regulation	$V_{IN1} = 7\text{ V}$ , $-5\text{ mA} \leq I_{O1} \leq -0.6\text{ mA}$		100	mV
$\Delta V_{O2\text{ LO}}$		$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$ , $-5\text{ mA} \leq I_{O2} \leq -0.6\text{ mA}$		250	
$V_{IO1}$	Dropout Voltage	$V_{IN1} = 7\text{ V}$ , $I_{O1} = -750\text{ mA}$		1.4	V
		$V_{IN1} = 7\text{ V}$ , $I_{O1} = -1.0\text{ mA}$		2.0	
$V_{IO2}$	Dropout Voltage	$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$ , $I_{O1} = -750\text{ mA}$		1.4	V
		$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$ , $I_{O1} = -1.0\text{ mA}$		2.0	
$I_Q$	Quiescent Current	$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$ , $V_{DIS} = 0.8\text{ V}$ , $I_{O1} = -10\text{ mA}$		2.0	mA
$I_{O1,2\text{ SC}}$	Short Circuit Output Current	$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$		1.6	A
		$V_{IN1} = 16\text{ V}$ , $V_{IN2} = 16\text{ V}$		1.0	
$I_{DIS}$	Disable Bias Current	$0\text{ V} \leq V_{DIS} \leq 7\text{ V}$ , $V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$	-100	2.0	$\mu\text{A}$
$V_{DISH}$	Disable Voltage High (out 2 active)	$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$	2		V
$V_{DISL}$	Disable Voltage Low (out 2 disabled)	$V_{IN1} = 7\text{ V}$ , $V_{IN2} = 14\text{ V}$		0.8	V

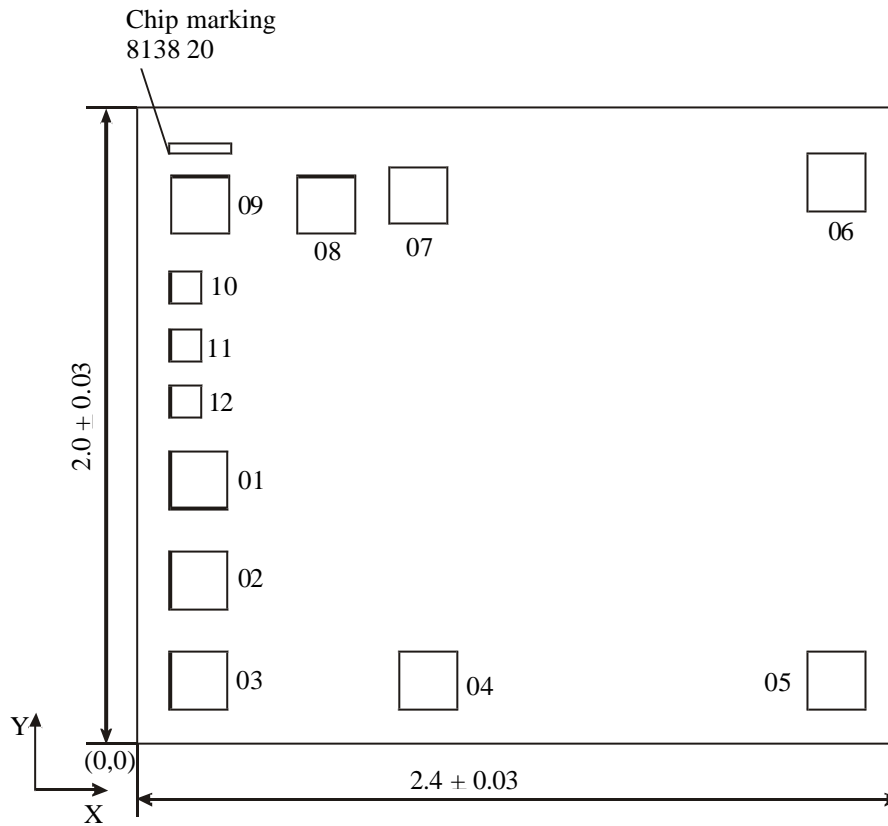
**TYPICAL APPLICATION**

C1 to C4 = 10  $\mu\text{F}$





**CHIP PAD DIAGRAM**



**Location of marking (mm):** left lower corner  $x=0.100$ ,  $y=1.854$ .

**Chip thickness:**  $0.35 \pm 0.02$  mm.

**PAD LOCATION**

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	GND	0.105	0.740	0.18 x 0.18
02	-	0.105	0.425	0.18 x 0.18
03	-	0.105	0.110	0.18 x 0.18
04	OUTPUT 2	0.825	0.110	0.18 x 0.18
05	OUTPUT 1	2.110	0.110	0.18 x 0.18
06	INPUT 1	2.110	1.675	0.18 x 0.18
07	INPUT 2	0.795	1.635	0.18 x 0.18
08	-	0.505	1.605	0.18 x 0.18
09	DISABLE	0.110	1.605	0.18 x 0.18
10	-	0.105	1.385	0.10 x 0.10
11	-	0.105	1.205	0.10 x 0.10
12	-	0.105	1.025	0.10 x 0.10

Note: Pad location is given as per passivation layer