

# HD74LV174A

## Hex D-type Flip-Flops with Clear

# HITACHI

ADE-205-269 (Z)  
1st Edition  
April 1999

### Description

This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the clock input. The clear input when low, sets all outputs to a low state. Low-voltage and high-speed operation is suitable for battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

### Features

- $V_{CC} = 2.0\text{ V}$  to  $5.5\text{ V}$  operation
- All inputs  $V_{IH}$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 0\text{ V}$  to  $5.5\text{ V}$ )
- All outputs  $V_O$  (Max.) =  $5.5\text{ V}$  (@ $V_{CC} = 0\text{ V}$ )
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.3\text{ V}$  (@ $V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Output current  $\pm 6\text{ mA}$  (@ $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ),  $\pm 12\text{ mA}$  (@ $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ )

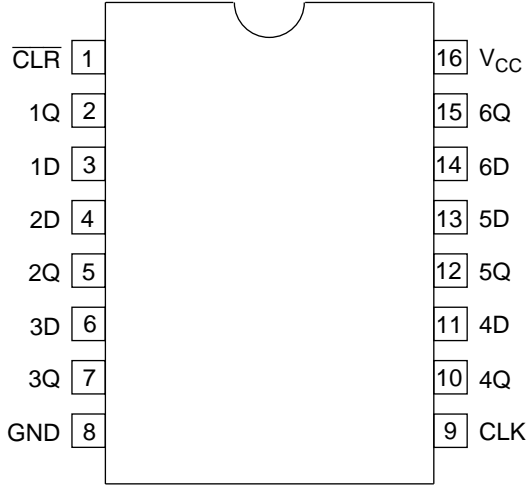
### Function Table

#### Inputs

CLR	CLK	D	Output Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	↓	X	no change

Note: H: High level  
L: Low level  
X: Immaterial  
↑: Low to high transition  
↓: High to low transition

## Pin Arrangement



(Top view)

**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range* <sup>1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range* <sup>1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L $V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* <sup>3</sup>	$P_T$	785	mW	SOP
		500		TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

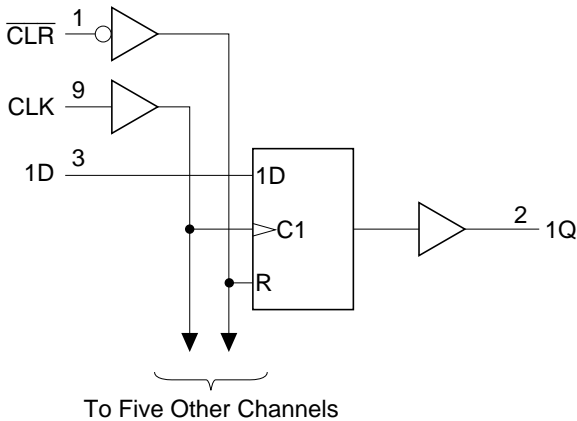
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	2.0	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	H or L
Output current	$I_{OH}$	—	-50	$\mu A$	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	$I_{OL}$	—	50	$\mu A$	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	$T_a$	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

## Logic Diagram



**DC Electrical Characteristics**

- $T_a = -40$  to  $85^\circ\text{C}$

Item	Symbol	$V_{CC}$ (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	$V_{IH}$	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	$V_{IL}$	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	$V_{OH}$	Min to Max	$V_{CC} - 0.1$	—	—	V	$I_{OH} = -50 \mu\text{A}$
		2.3	2.0	—	—		$I_{OH} = -2 \text{ mA}$
		3.0	2.48	—	—		$I_{OH} = -6 \text{ mA}$
		4.5	3.8	—	—		$I_{OH} = -12 \text{ mA}$
	$V_{OL}$	Min to Max	—	—	0.1		$I_{OL} = 50 \mu\text{A}$
		2.3	—	—	0.4		$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44		$I_{OL} = 6 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 12 \text{ mA}$
Input current	$I_{IN}$	0 to 5.5	—	—	$\pm 1$	$\mu\text{A}$	$V_I = 5.5 \text{ V}$ or GND
Quiescent supply current	$I_{CC}$	5.5	—	—	20	$\mu\text{A}$	$V_I = V_{CC}$ or GND, $I_O = 0$
Output leakage current	$I_{OFF}$	0	—	—	5	$\mu\text{A}$	$V_I$ or $V_O = 0 \text{ V}$ to $5.5 \text{ V}$
Input capacitance	$C_{IN}$	3.3	—	1.7	—	pF	$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Switching Characteristics

- $V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	55	115	—	50	—	MHz	CL = 15 pF		
		45	90	—	40	—				
Propagation delay time	tPLH / tPHL	—	8.4	17.1	1.0	19.0	ns	CL = 15 pF	CLK	Q
		—	10.8	20.6	1.0	23.0				
	tPHL	—	6.3	17.3	1.0	19.5	ns	CL = 15 pF	CLR	
		—	8.2	21.9	1.0	23.5				
Setup time	tSU	8.5	—	—	9.5	—	ns			Data before CLK↑
		4.0	—	—	4.0	—				CLR inactive before CLK↑
Hold time	th	-0.5	—	—	0.0	—	ns			Data after CLK↑
Pulse width	tw	6.0	—	—	6.5	—	ns			CLR L
		7.0	—	—	7.0	—				CLK H or L

**Switching Characteristics (cont)**

$V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock fre- quency	fmax	95	170	—	50	—	MHz	CL = 15 pF		
		55	130	—	40	—				
Propa- gation delay time	tPLH / tPHL	—	5.8	11.0	1.0	13.0	ns	CL = 15 pF	CLK	Q
		—	7.5	14.5	1.0	16.5				
	tPHL	—	4.5	11.4	1.0	13.5	ns	CL = 15 pF	CLR	
		—	6.0	14.9	1.0	17.0				
Setup time	tSU	5.0	—	—	6.0	—	ns		Data before CLK↑	
		3.0	—	—	3.0	—				
Hold time	th	0.0	—	—	0.0	—	ns		Data after CLK↑	
Pulse width	tW	5.0	—	—	5.0	—	ns		CLR L	
		5.0	—	—	5.0	—				

## Switching Characteristics (cont)

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	130	240	—	110	—	MHz	CL = 15 pF		
		90	180	—	80	—				
Propagation delay time	tPLH / tPHL	—	4.1	7.2	1.0	8.5	ns	CL = 15 pF	CLK	Q
		—	5.5	9.2	1.0	10.5				
	tPHL	—	3.0	7.6	1.0	9.0	ns	CL = 15 pF	CLR	
		—	4.2	9.6	1.0	11.0				
Setup time	tSU	4.5	—	—	4.5	—	ns		Data before CLK↑	
		2.5	—	—	2.5	—				
Hold time	th	0.5	—	—	0.5	—	ns		Data after CLK↑	
Pulse width	tW	5.0	—	—	5.0	—	ns		CLR L	
		5.0	—	—	5.0	—				



## Output-skew Characteristics

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ C$			$T_a = -40 \text{ to } 85^\circ C$		Unit
			Min	Typ	Max	Min	Max	
Output skew	$t_{sk(O)}$	2.3 to 2.7	—	—	2.0	—	2.0	ns
		3.0 to 3.6	—	—	1.5	—	1.5	
		4.5 to 5.5	—	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

## Operating Characteristics

- $C_L = 50 \text{ pF}$

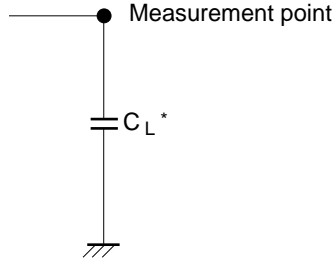
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ C$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	3.3	—	14	—	pF	$f = 10 \text{ MHz}$
		5.0	—	15.1	—		

## Noise Characteristics

- $C_L = 50 \text{ pF}$

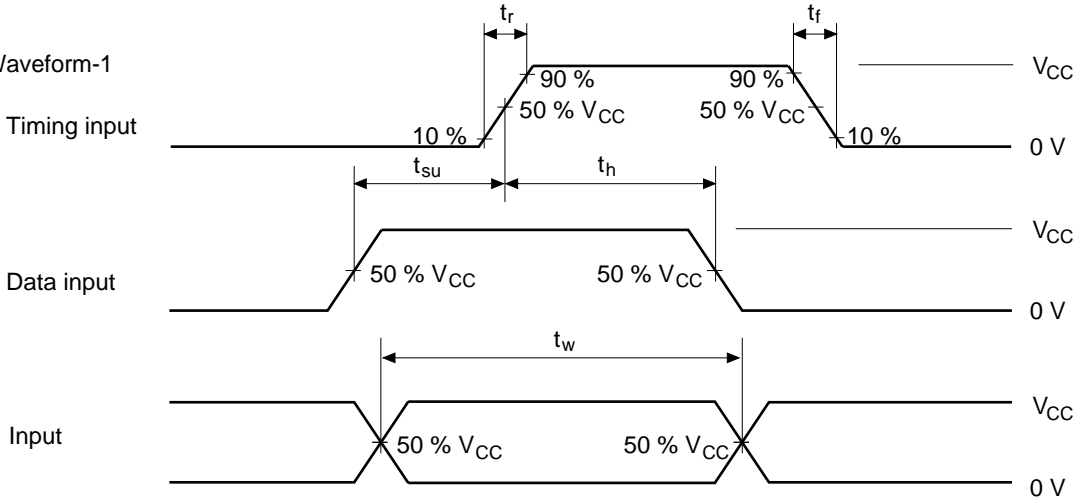
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ C$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic $V_{OL}$	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic $V_{OL}$	$V_{OL(V)}$	3.3	—	-0.3	-0.8		
Quiet output, minimum dynamic $V_{OH}$	$V_{OH(V)}$	3.3	—	3.0	—		
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99		

**Test Circuit**

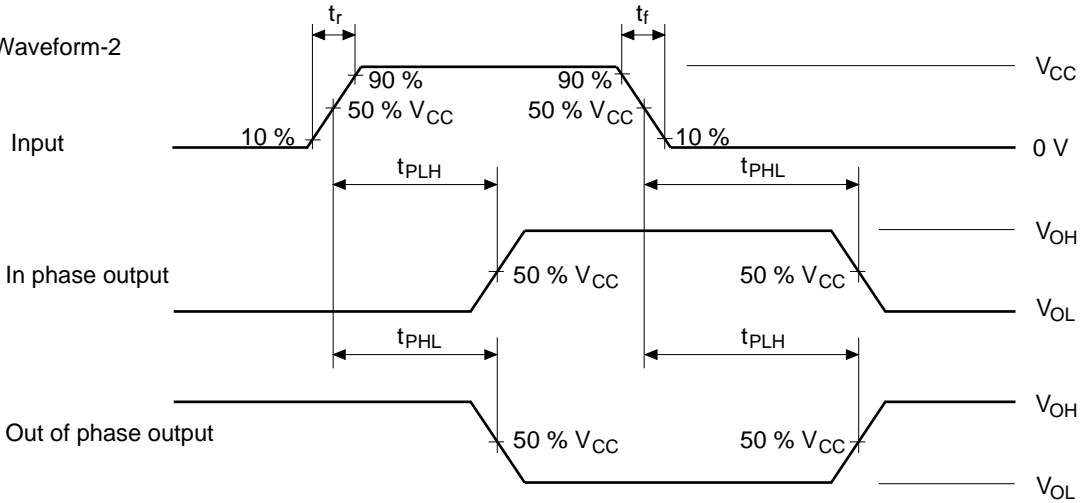


Note:  $C_L$  includes the probe and jig capacitance.

• Waveform-1

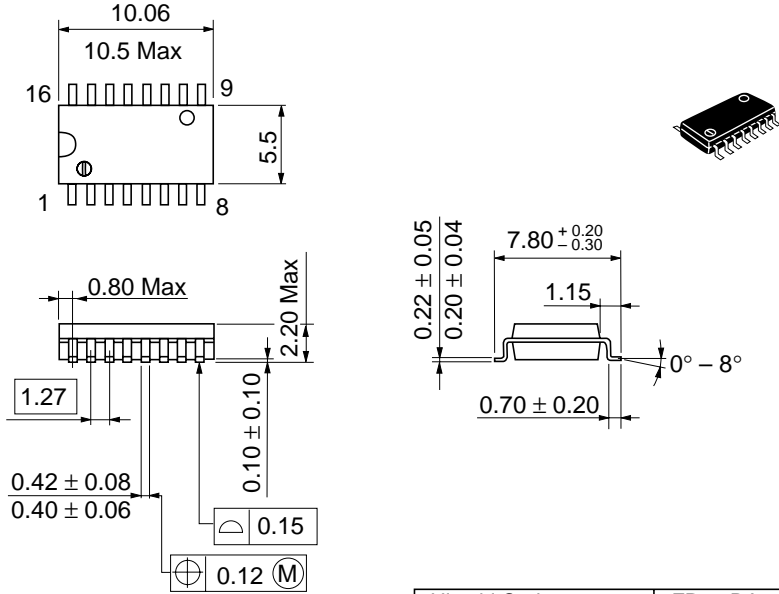


• Waveform-2



- Notes: 1. Input waveform:  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$   
 2. The output is measured one at a time with one transition per measurement.

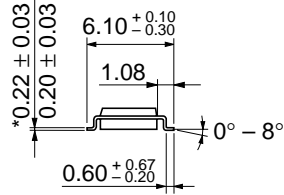
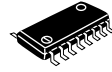
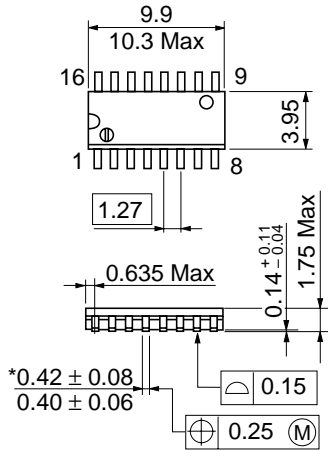
## Package Dimensions



Dimension including the plating thickness  
Base material dimension

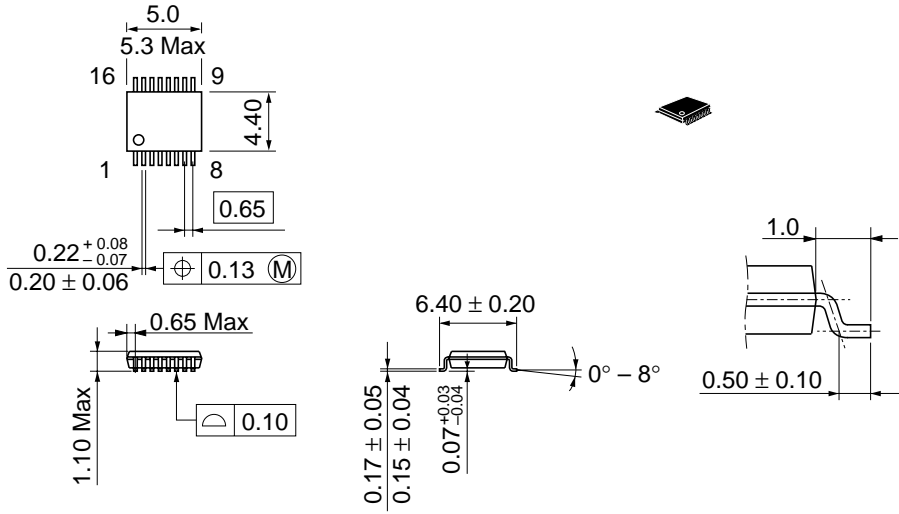
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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