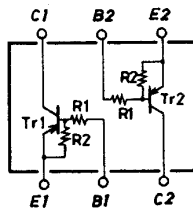


**FC105**

PNP Epitaxial Planar Silicon Composite Transistor

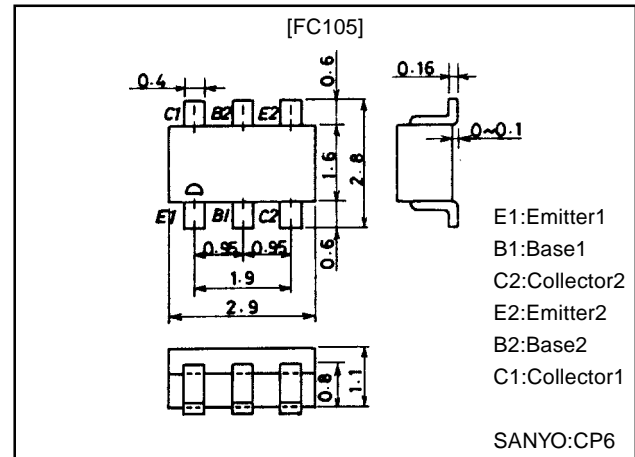
Switching Applications**Features**

- On-chip bias resistors ($R1=47k\Omega$, $R2=47k\Omega$)
- Composite type with 2 transistors contained in the CP package currently in use, improving the mounting efficiency greatly.
- The FC105 is formed with two chips, being equivalent to the 2SA1341, placed in one package.
- Excellent in thermal equilibrium and pair capability.

Electrical Connection**Package Dimensions**

unit:mm

2067



E1:Emitter1
B1:Base1
C2:Collector2
E2:Emitter2
B2:Base2
C1:Collector1

SANYO:CP6

Specifications**Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$**

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------|-----------|------------|------------|------------------|
| Collector-to-Base Voltage | V_{CBO} | | -50 | V |
| Collector-to-Emitter Voltage | V_{CEO} | | -50 | V |
| Emitter-to-Base Voltage | V_{EBO} | | -10 | V |
| Collector Current | I_C | | -100 | mA |
| Collector Current (Pulse) | I_{CP} | | -200 | mA |
| Collector Dissipation | P_C | 1 unit | 200 | mW |
| Total Dissipation | P_T | | 300 | mW |
| Junction Temperature | T_J | | 150 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | | -55 to+150 | $^\circ\text{C}$ |

Electrical Characteristics at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--------------------------|---------------|---|---------|------|------|---------------|
| | | | min | typ | max | |
| Collector Cutoff Current | I_{CBO} | $V_{CB}=-40\text{V}$, $I_E=0$ | | | -0.1 | μA |
| Collector Cutoff Current | I_{CEO} | $V_{CE}=-40\text{V}$, $I_B=0$ | | | -0.5 | μA |
| Emitter Cutoff Current | I_{EBO} | $V_{EB}=-5\text{V}$, $I_C=0$ | -30 | -53 | -80 | μA |
| DC Current Gain | h_{FE} | $V_{CE}=-5\text{V}$, $I_C=-5\text{mA}$ | 50 | | | |
| Gain-Bandwidth Product | f_T | $V_{CE}=-10\text{V}$, $I_C=-5\text{mA}$ | | 200 | | MHz |
| Output Capacitance | C_{ob} | $V_{CB}=-10\text{V}$, $f=1\text{MHz}$ | | 5.1 | | pF |
| C-E Saturation Voltage | $V_{CE(sat)}$ | $I_C=-5\text{mA}$, $I_B=-0.25\text{mA}$ | | -0.1 | -0.3 | V |
| C-B Breakdown Voltage | $V_{(BR)CBO}$ | $I_C=-10\mu\text{A}$, $I_E=0$ | -50 | | | V |
| C-E Breakdown Voltage | $V_{(BR)CEO}$ | $I_C=-100\mu\text{A}$, $R_{BE}=\infty$ | -50 | | | V |
| Input OFF-State Voltage | $V_{I(off)}$ | $V_{CE}=-5\text{V}$, $I_C=-100\mu\text{A}$ | -0.8 | -1.1 | -1.5 | V |
| Input ON-State Voltage | $V_{I(on)}$ | $V_{CE}=-0.2\text{V}$, $I_C=-5\text{mA}$ | -1.0 | -2.5 | -5.0 | V |
| Input Resistance | R_1 | | 32 | 47 | 62 | $k\Omega$ |
| Resistance Ratio | R_1/R_2 | | 0.9 | 1.0 | 1.1 | |

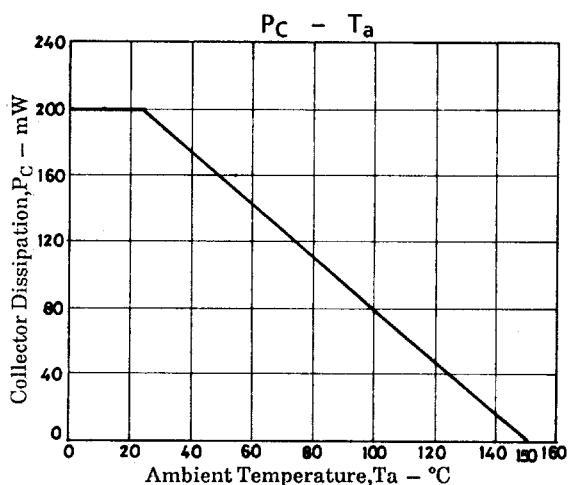
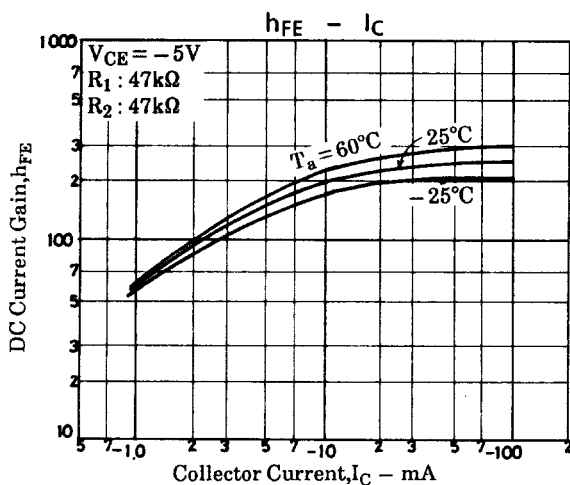
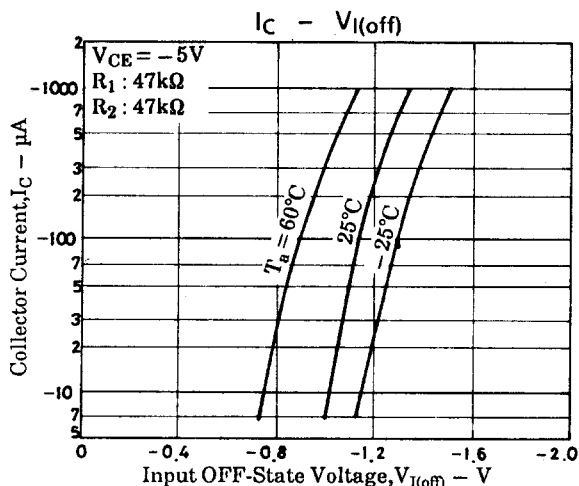
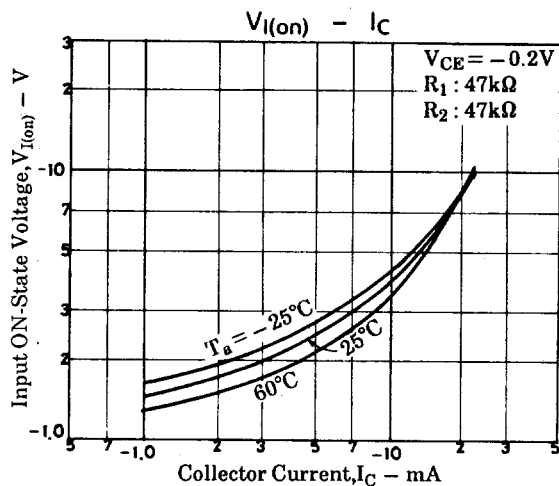
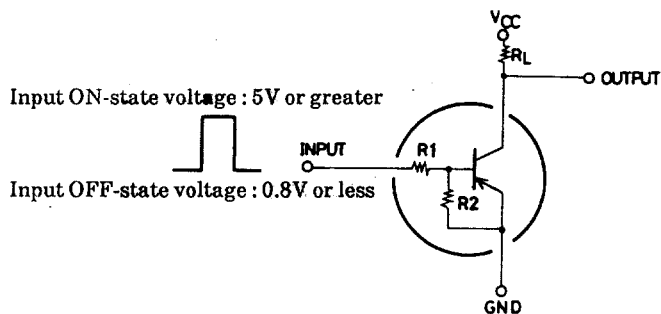
Note: The specifications shown above are for each individual transistor.

Marking:105

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Sample Application Circuit



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