

SMD 8 Pin 5 Tap TTL Compatible Active Delay Lines

EPA1140-XX & EPA1140-XX-RC

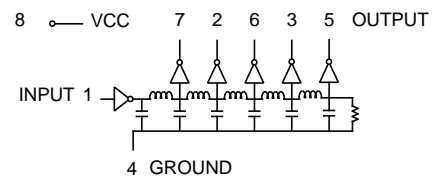
Add "-RC" after part number for RoHS Compliant

PCA Part Number	Tap Delays ($\pm 5\%$ or $\pm 2nS$)	Total Delay ($\pm 5\%$ or $\pm 2nS$)	PCA Part Number	Tap Delays ($\pm 5\%$ or $\pm 2nS$)	Total Delay ($\pm 5\%$ or $\pm 2nS$)
EPA1140-25(-RC)	5, 10, 15, 20	25	EPA1140-150(-RC)	30, 60, 90, 120	150
EPA1140-30(-RC)	6, 12, 18, 24	30	EPA1140-175(-RC)	35, 70, 105, 140	175
EPA1140-35(-RC)	7, 14, 21, 28	35	EPA1140-200(-RC)	40, 80, 120, 160	200
EPA1140-40(-RC)	8, 16, 24, 32	40	EPA1140-225(-RC)	45, 90, 135, 180	225
EPA1140-45(-RC)	9, 18, 27, 36	45	EPA1140-250(-RC)	50, 100, 150, 200	250
EPA1140-50(-RC)	10, 20, 30, 40	50	EPA1140-300(-RC)	60, 120, 180, 240	300
EPA1140-60(-RC)	12, 24, 36, 48	60	EPA1140-350(-RC)	70, 140, 210, 280	350
EPA1140-75(-RC)	15, 30, 45, 60	75	EPA1140-400(-RC)	80, 160, 240, 320	400
EPA1140-100(-RC)	20, 40, 60, 80	100	EPA1140-450(-RC)	90, 180, 270, 360	450
EPA1140-125(-RC)	25, 50, 75, 100	125	EPA1140-500(-RC)	100, 200, 300, 400	500

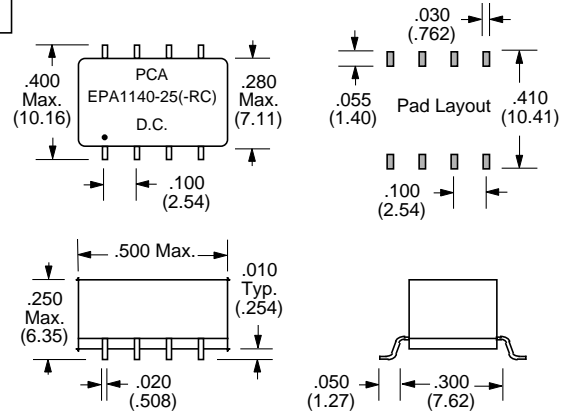
† Whichever is greater. Delay times referenced from input to leading and trailing edges at 25°C, 5.0V, with no load.

DC Electrical Characteristics Parameter		Test Conditions	Min.	Max.	Unit
V _{OH}	High-Level Output Voltage	V _{CC} = min. V _{IL} = max. I _{OH} = max	2.7		V
V _{OL}	Low-Level Output Voltage	V _{CC} = min. V _{IH} = min. I _{OL} = max		0.5	V
V _{IK}	Input Clamp Voltage	V _{CC} = min. I _I = I _{IK}		-1.2	V
I _{IH}	High-Level Input Current	V _{CC} = max. V _{IN} = 2.7V		50	µA
		V _{CC} = max. V _{IN} = 5.25V		1.0	mA
I _{IL}	Low-Level Input Current	V _{CC} = max. V _{IN} = 0.5V		-2	mA
I _{OS}	Short Circuit Output Current	V _{CC} = max. V _{OUT} = 0. (One output at a time)	-40	-100	mA
I _{CCH}	High-Level Supply Current	V _{CC} = max. V _{IN} = OPEN		75	mA
I _{CCL}	Low-Level Supply Current	V _{CC} = max. V _{IN} = 0		75	mA
T _{RO}	Output Rise Time	T _d 500 nS (0.75 to 2.4 Volts)		4	nS
N _H	Fanout High-Level Output	V _{CC} = max. V _{OH} = 2.7V		20 TTL Load	
N _L	Fanout Low-Level Output	V _{CC} = max. V _{OL} = 0.5V		10 TTL Load	

Schematic



Package



Recommended Operating Conditions		Min.	Max.	Unit
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IH}	High-Level Input Voltage	2.0		V
V _{IL}	Low-Level Input Voltage		0.8	V
I _{IK}	Input Clamp Current		-18	mA
I _{OH}	High-Level Output Current		-1.0	mA
I _{OL}	Low-Level Output Current		20	mA
PW*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T _A	Operating Free-Air Temperature	-55	+125	°C

*These two values are inter-dependent.

Input Pulse Test Conditions @ 25° C			Unit
E _{IN}	Pulse Input Voltage	3.2	Volts
P _W	Pulse Width % of Total Delay	110	%
T _{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P _{RR}	Pulse Repetition Rate @ T _d 200 nS	1.0	MHZ
	Pulse Repetition Rate @ T _d > 200 nS	100	KHZ
V _{CC}	Supply Voltage	5.0	Volts

Notes :	EPA1140-XX	EPA1140-XX-RC
1. Lead Finish	SnPb	Hot Tin Dip (Sn) †
2. Peak Temperature Rating	225°C	260°C
4. Weight	.976 grams	.976 grams
5. Packaging Information (*Add "TR" to end of part number, but in front of "-RC" when placing order)	(Tube) TBD pieces/tube (Tape & Reel) TBD pieces/13" reel ("EPA1140-XXTR")	TBD pieces/tube TBD pieces/13" reel ("EPA1140-XXTR-RC")

† Lead Material : Matte Tin with Ni Barrier

Unless Otherwise Specified Dimensions are in Inches /mm ± .010 / .25