



dsPIC33FJ12GP201/202 Rev. A2 Silicon Errata

The dsPIC33FJ12GP201/202 (Rev. A2) devices you received were found to conform to the specifications and functionality described in the following documents:

- DS70264 – “dsPIC33FJ12GP201/202 Data Sheet”
- DS70157 – “dsPIC30F/33F Programmer’s Reference Manual”

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC33FJ12GP201
- dsPIC33FJ12GP202

dsPIC33FJ12GP201/202 Rev. A2 silicon is identified by performing a “Reset and Connect” operation to the device using MPLAB® ICD 2 or MPLAB REAL ICE™ in-circuit emulator, with MPLAB IDE v7.60 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*.

The errata described in this document will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. JTAG Programming
JTAG programming does not work.
2. UART
UART receptions may be corrupted if the Baud Rate Generator (BRG) is set up for 4x mode.
3. UART
The auto-baud feature may not calculate the correct baud rate when the BRG is set up for 4x mode.
4. UART
With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.
5. UART
The auto-baud feature measures baud rate inaccurately for certain baud rate and clock speed combinations.
6. Traps and Idle Mode
If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine.

The following sections describe the errata and work around to these errata, where they may apply.

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1. Module: JTAG Programming

JTAG programming does not work.

Work around

None.

2. Module: UART

UART receptions may be corrupted if the Baud Rate Generator is set up for 4x mode (BRGH = 1).

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

3. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRGH, is set. With the BRGH bit set, the baud rate calculation used is the same as BRG = 0.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRGH bit.

4. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

5. Module: UART

The auto-baud feature may miscalculate for certain baud rate and clock speed combinations, resulting in a BRG value that is greater than or less than the expected value by 1. This may result in reception or transmission failures.

Work around

Test the auto-baud rate at various clock speed and baud rate combinations that would be used in an application. If an inaccurate BRG value is generated, manually correct the baud rate in user software.

6. Module: Traps and Idle Mode

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled) the user software should check the state of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred, and then perform the appropriate clock switch operation.

APPENDIX A: REVISION HISTORY

Revision A (5/2007)

Initial release of this document, which includes silicon issues 1 (JTAG Programming), 2 (UART) through 5 (UART) and 6 (Traps and Idle Mode).

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NOTES:

Note the following details of the code protection feature on Microchip devices:

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