DS2405
Addressable Switch

www.maxim-ic.com

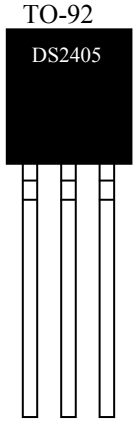
FEATURES

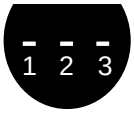
- Open-drain PIO pin is controlled by matching 64-bit, laser-engraved registration number associated with each device
- Logic level of open drain output can be determined over 1-Wire® bus for closed-loop control
- PIO pin sink capability is greater than 4mA at 0.4V
- Multiple DS2405s can be identified on a common 1-Wire bus and be turned on or off independent of other devices on the bus
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code +48-bit serial number +8-bit CRC tester) assures absolute identity because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- Reduces control, address, data, and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
- 8-bit family code specifies DS2405 communications requirements to reader
- 8-bit cyclic redundancy check ensures error-free selection
- Zero standby power required
- Low cost TO-92, SOT-223, or 6-pin TSOC surface mount package
- 1-Wire communication operates over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C

1-Wire is a registered trademark of Dallas Semiconductor.

PIN ASSIGNMENT

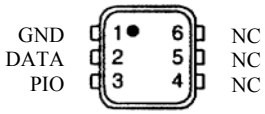
TO-92





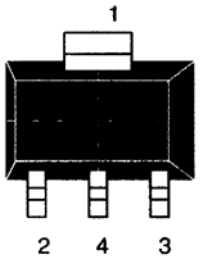
BOTTOM VIEW
See Mech.
Drawings Section

TSOC PACKAGE



TOP VIEW
3.7 X 4.0 X 1.5

SOT–223

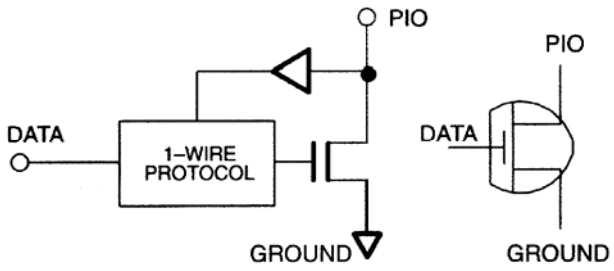


TOP VIEW

NOTE: The leads of TO-92 packages on tape-and-reel are formed to approximately 100 mils (2.54 mm) spacing. For details refer to drawing 56-G0006-003.

PIN DESCRIPTION

TO-92		TSOC	
Pin 1	- Ground	Pin 1	- Ground
Pin 2	- Data	Pin 2	- Data
Pin 3	- PIO	Pin 3	- PIO
Pin 4	- Ground	Pin 4-6	-No Connect



ORDERING INFORMATION

DS2405	TO-92 package
DS2405Z	4-pin SOT-223 package
DS2405P	6-pin TSOC package
DS2405/T&R	Tape & Reel version of DS2405
DS2405Z/T&R	Tape & Reel version of DS2405Z
DS2405P/T&R	Tape & Reel version of DS2405P

DESCRIPTION

The DS2405 Addressable Switch is an open drain N-channel transistor that can be turned on or off by matching the 64-bit factory-lasered registration number within each part. The 64-bit number consists of an 8-bit family code, a unique 48-bit serial number, and an 8-bit cyclic redundancy check. Communication with the DS2405 follows the standard Dallas Semiconductor 1-Wire protocol and can be accomplished with a single port pin of a microcontroller. Multiple DS2405 devices can reside on a common 1-Wire bus creating a MicroLAN. The network controller circuitry is embedded within the chip including a search algorithm to determine the identity of each DS2405 on the network. The open drain output (PIO pin) for each DS2405 on the MicroLan can be independently toggled on or off whether there is one or many devices sharing the same 1-Wire bus. The logic level of the PIO pin for each device on the MicroLan can also be individually sensed and reported to the bus master.

OVERVIEW

The DS2405 Addressable Switch provides a means for assigning an electronically readable identification to a particular node or location with additional control capability provided by an open drain N-channel MOSFET that can be remotely switched and sensed via communication over the 1-Wire bus. The DS2405 contains a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit family code (05h). The 64-bit ROM portion of the DS2405 not only creates an absolutely unique electronic identification for the device itself but also is a means to locate and change or obtain the state of the switch that is associated with the 64-bit ROM. The structure of the 64-bit ROM is shown in Figure 1. The device derives its power entirely from the 1-Wire bus by storing energy on an internal capacitor during periods of time when the signal line is high and continues to operate off of this "parasite" power source during the low times of the 1-Wire line until it returns high to replenish the parasite (capacitor) supply. The DS2405 uses the standard Dallas Semiconductor 1-Wire protocol for data transfers, with all data being read and written least significant bit first. Communication to and from the DS2405 requires a single bidirectional line that is typically the port pin of the microcontroller. The 1-Wire bus master (microcontroller) must first issue one of five ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM, and 5) Active-Only Search ROM. These commands operate on the 64-bit lasered ROM portion of each device and can singulate a specific device if many are present on the 1-Wire line as well as indicate to the bus how many and what type of each device is present. The protocol required for these ROM function commands is described in Figure 4. After a ROM function command is successfully executed, the open drain output can be toggled or its current status determined via the 1-Wire bus.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS2405 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing). For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton® Standards.

Hardware Configuration

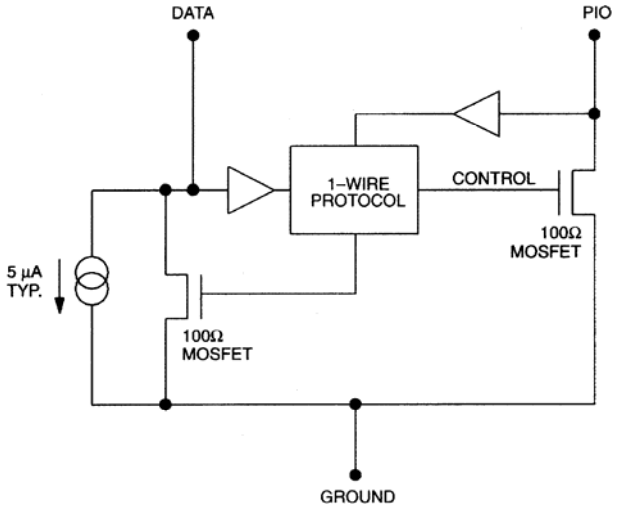
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain connection or 3-state outputs. The DS2405 is an open drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pullup resistor should be approximately 5 kΩ for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbits/s.

The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 μs, one or more of the devices on the bus may be reset. In addition, the state of the PIO pin for one or more of the DS2405s on the bus may return to its default (off) condition.

DS2405 MEMORY MAP Figure 1

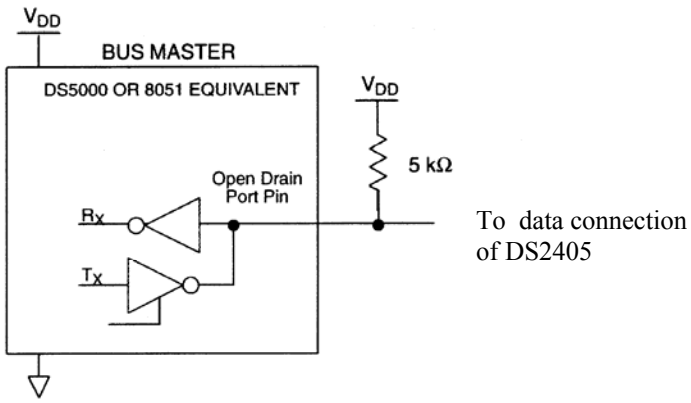
8-Bit CRC Code		48-Bit Serial Number		8-Bit Family Code (05h)	
MSB	LSB	MSB	LSB	MSB	LSB

DS2405 EQUIVALENT CIRCUIT Figure 2

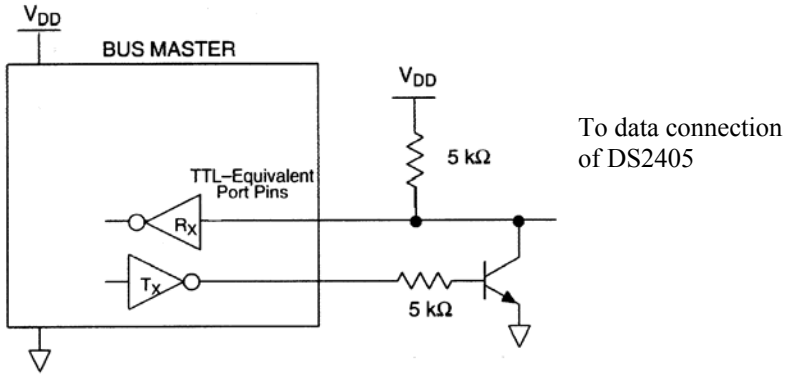


BUS MASTER CIRCUIT Figure 3

A) Open Drain



B) Standard TTL



TRANSACTION SEQUENCE

The sequence for accessing the DS2405 via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a Reset Pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s).

The Presence Pulse lets the bus master know that at least one DS2405 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of five ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 4).

Read ROM [33h]

This command allows the bus master to read the DS2405's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can be used only if there is a single DS2405 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result).

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific device on a multidrop bus. All devices that do not match the 64-bit ROM sequence will wait for a Reset Pulse. The DS2405 that exactly matches the 64-bit ROM sequence will toggle the state of its PIO pin after the 64th bit of the match is entered. If the open drain N-channel device was off, it will be turned on and vice versa. After the last bit of the ROM sequence is received from the bus master and the PIO pin of the selected DS2405 has toggled, additional read time slots issued by the bus master will cause the DS2405 to output the logic state of its PIO pin onto the 1-Wire bus. If the pulldown is on and the PIO pin is a logical 0, the DS2405 will respond with read-0 time slots. If the pulldown is off and the PIO pin is a logical 1 (external pullup is required), the DS2405 will respond with read-1 time slot. Each additional read time slot issued by the bus master will continue to indicate the state of the PIO pin until a Reset Pulse is received from the bus master.

Search ROM [F0h]

When a system is initially interrogated, the bus master may not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. This process of elimination involves repeated application of a simple three-step procedure where the bus master starts by reading a bit position in the 64-bit ROM, followed by reading the complement of that bit position, and finally writing to all the devices still involved in the search the desired logic value for that bit position. An example is shown below and a flowchart for the search algorithm can be found in the "Book of DS19xx iButton Standards."

Four devices are connected to the 1-Wire bus. Their binary ROM contents are listed below:

device 1: xxxxxx10101100
device 2: xxxxxx01010101
device 3: xxxxxx10101111
device 4: xxxxxx10001000

The x's represent the higher remaining bits. Shown are the lowest 8 bits of the ROM contents. The least significant bit is to the right in this representation. The search process runs as follows:

1. The master begins the initialization sequence by issuing a Reset Pulse. The devices respond by issuing Presence Pulses.

2. The master will then issue the Search ROM command on the 1-Wire bus.

3. The master reads 1 bit from the 1-Wire bus. Each device will respond by placing the value of the first bit of its respective ROM data onto the 1-Wire bus. Devices 1 and 4 will place a 0 onto the 1-Wire bus; that is, they pull it low. Devices 2 and 3 will send a 1 by allowing the line to stay high. The result is the logical AND of all devices on the line; therefore the master reads a 0. The master will issue another read time slot. Since the ROM Search command is being executed, all devices respond to this second read by placing the complement of the first bit of their respective ROM data onto the 1-Wire Bus. Devices 1 and 4 will send a 1; devices 2 and 3 will send a 0. Thus the 1-Wire bus will be pulled low. The master again reads a 0 for the complement of the first ROM data bit. This tells the master that there are devices on the bus that have a 0 in the first position and others that have a 1. If all devices had a 0 in this bit position, the reading would be 01; if the bit position contained a 1, the result would be 10. (Note that the 11 condition indicates that no devices are present on the 1-Wire bus.)

4. The master now decides to write a 0 on the 1-Wire bus. This deselects Devices 2 and 3 for the remainder of the search pass, leaving only devices 1 and 4 participating in the search process.

5. The master performs two more reads and receives a 0 followed by a 1 bit. This indicates that all active devices have a 0 in this bit position of their ROM.

6. The master then writes a 0 to keep devices 1 and 4 selected.

7. The master executes two reads and receives two 0 bits. This again indicates that both 1 and 0 exist as the third bit of the ROM of the active devices.

8. The master again writes a 0. This deselects device 1, leaving device 4 as the only active device.

9. Subsequent reads to the end of the ROM will not show bit conflicts. Therefore, they directly tell the master the ROM contents of the active device. After having learned any new ROM bit, the master has to resend this bit to keep the device selected. As soon as all ROM bits of the device are known and the last bit is resent by the master, the device is ready to output the state of the PIO pin using additional read time slots.

10. The master must learn the other devices' ROM data. Therefore, it starts another ROM Search sequence by repeating steps 1 through 7.

11. At the highest bit position, where the master wrote a 0 at the first pass (step 8), it now writes a 1. This deselects device 4, leaving device 1 active.

12. As in step 9, subsequent reads to the end of the ROM will not show bit conflicts. This completes the second ROM Search pass where the master has learned another ROM's contents.

13. The master must learn the other devices' ROM data. Therefore, it starts another ROM Search sequence by repeating steps 1 to 3.

14. At the second highest bit position where the master wrote a 0 at the first pass (step 4), it now writes a 1. This deselects devices 1 and 4, leaving devices 2 and 3 active.

15. The master sends two read time slots and receives two 0 bits, indicating a bit conflict.

16. The master again decides to write a 0. This deselects device 3, leaving device 2 as the only active device.

17. As in step 9, subsequent reads to the end of the ROM will not show bit conflicts. This completes the third ROM Search pass where the master has learned another ROM's contents.

18. The master must learn the other devices' ROM data. Therefore it starts another ROM Search sequence by repeating steps 13 to 15.

19. At the highest bit position where the master wrote a 0 at the previous pass (step 16), it now writes a 1. This deselects device 2, leaving device 3 active.

20. As in step 17, subsequent reads to the end of the ROM will not show bit conflicts. This completes the fourth ROM Search pass where the master has learned another ROM's contents.

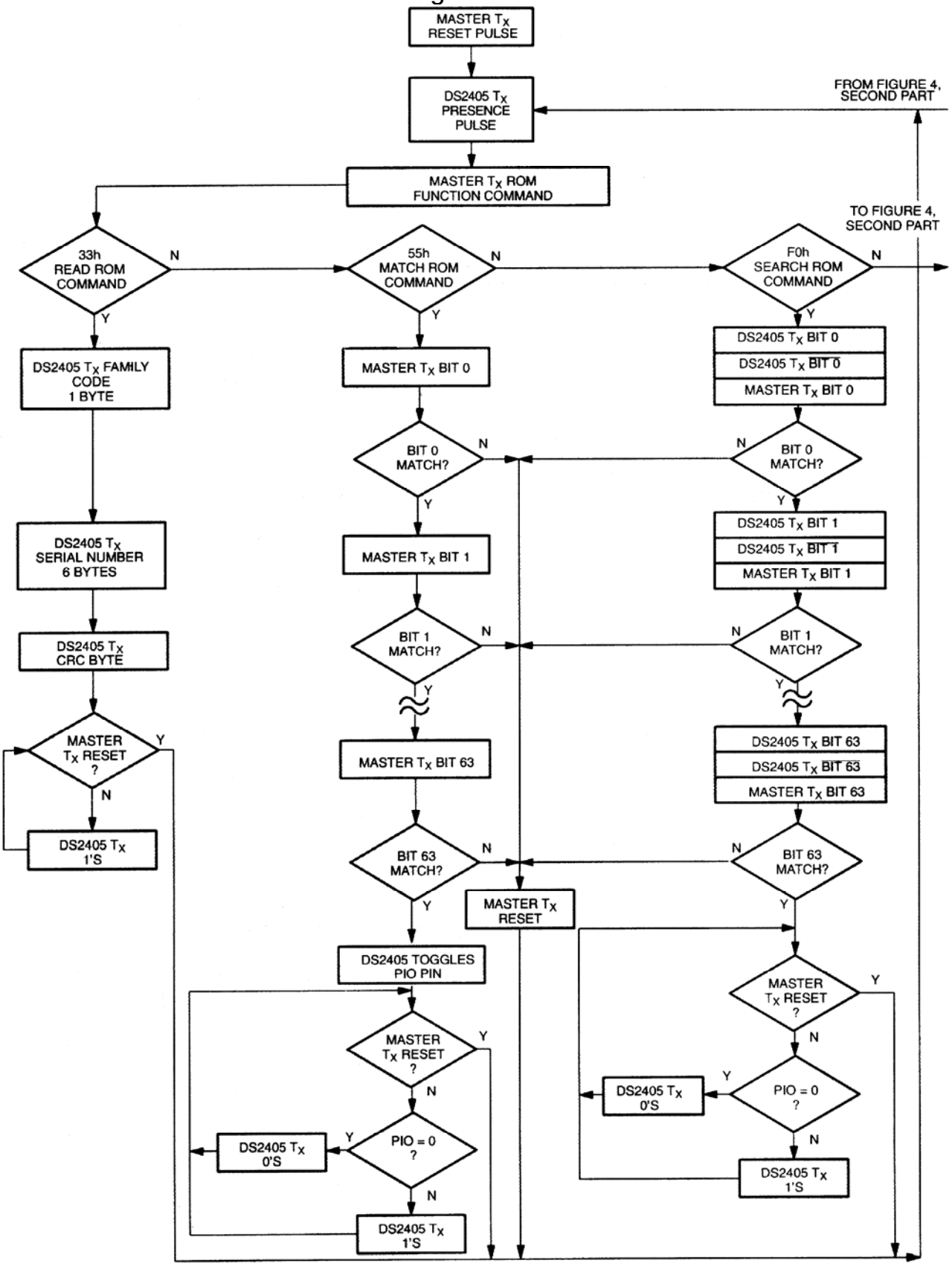
After one complete pass, the bus master knows the contents of the 64-bit ROM in one device. Subsequent passes will reveal the total number of devices and their individual ROM codes. In addition, after each complete pass of the search that successfully determines the 64-bit ROM for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM has been issued since all other devices will have dropped out of the search process and are waiting for a Reset Pulse. The DS2405 that was discovered by the search process will not toggle the state of its PIO pin at the end of the search, but additional read time slots issued by the bus master after the search is completed will cause the DS2405 to output the logic state of its PIO pin onto the 1-Wire bus. If the pulldown is on and the PIO pin is a logical 0, the DS2405 will respond with read-0 time slots. If the pulldown is off and the PIO pin is a logical 1 (external pullup is required), the DS2405 will respond with read-1 time slots. Each additional read time slot issued by the bus master will continue to indicate the state of the PIO pin until a Reset Pulse is received from the bus master. The combination of Match ROM and Search ROM allows the user to change the state of the PIO pin and report the current state (Match ROM) or simply report the current state of the PIO pin without changing it (Search ROM).

Active-Only Search ROM [ECh]

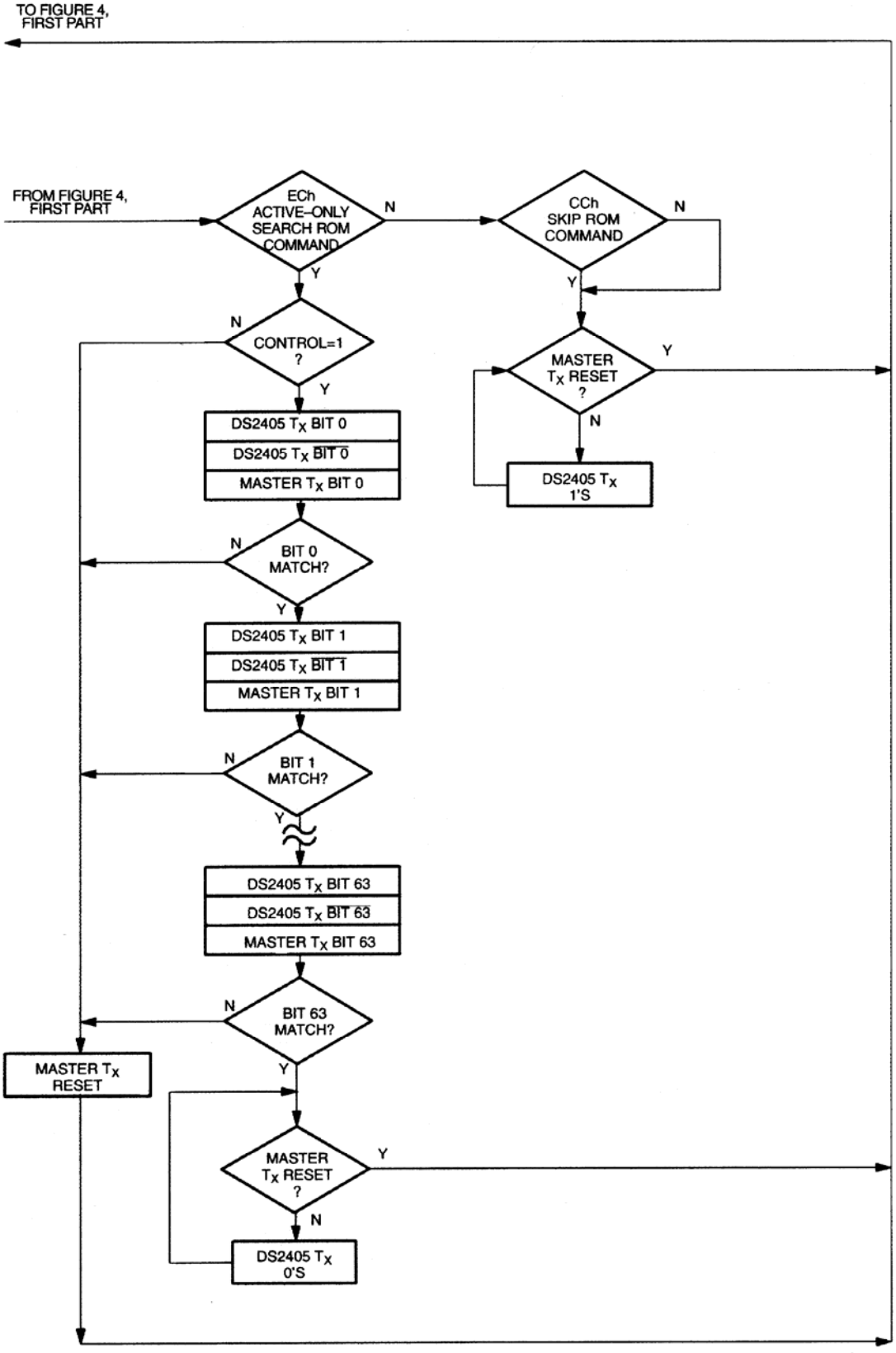
The Active-Only Search ROM command operates similarly to the Search ROM command except that only devices with their output pulldown turned on are allowed to participate in the search. This provides an efficient means for the bus master to determine devices on a multidrop system that are active (PIO pin driven low). After each pass of the active-only search that successfully determines the 64-bit ROM for a specific device on the multidrop bus with its output pulldown turned on, that particular device can be individually accessed as if a Match ROM had been issued since all other devices will have dropped out of the active-only search process and are waiting for a Reset Pulse. The DS2405 that was discovered by the active-only search process will not toggle the state of its PIO pin at the end of the search, but additional read time slots issued by the bus master after the search is completed will cause the DS2405 to output the logic state of the PIO pin (see Figure 2) onto the 1-wire bus. Since the Active-Only Search ROM command only operates on devices with their pulldown on, the internal CONTROL signal for each of these parts is always a logical 1. With CONTROL=1, the selected DS2405 will respond to the bus master with read-0 time slots after an active-only search pass is successfully completed. Each additional read time slot issued by the bus master will continue to appear as a read-0 until a Reset Pulse is received from the bus master. If the CONTROL signal is a logical 0 for any DS2405, that device will not participate in the Active-Only Search. The combination of Search ROM and Active-Only Search ROM allows the user to search in the most efficient manner depending on the requirements. If the bus master interrogates a multidrop system comprised of DS2405s whose PIO conditions are unknown, the Active-Only Search can quickly determine which devices are turned on. The two commands also allow the bus master to separately determine the state of the PIO pin and the internal CONTROL signal which may be useful in detecting certain conditions. If Search ROM returns read-0 time slots (PIO=logical 0) for a given device, it may be due to that particular DS2405 driving its PIO pin low, or under certain conditions the logical 0 may be caused by some other device holding PIO low. If that same device is found using an active-only search, CONTROL must be a logical 1 and the PIO pin is being held low by the DS2405. If that same

device is not found using an active-only search, CONTROL must be a logical 0 and the PIO pin is being held low by some other device or perhaps a fault condition such as a PIO shorted to ground. A second fault condition may be detected if Search ROM for a given device returns read-1 time slots (PIO=logical 1) but Active-Only Search ROM is successful (CONTROL=logical 1) and returns read-0 time slots for the same device, indicating the possibility that PIO may be shorted to a positive voltage.

ROM FUNCTIONS FLOW CHART Figure 4



ROM FUNCTIONS FLOW CHART Figure 4 (cont.)



Skip ROM [CCh]

The complete 1-Wire protocol for all Dallas Semiconductor iButtons contains a Skip ROM command. Since the DS2405 contains only the 64-bit ROM with no additional data fields, the Skip ROM is not applicable and will cause no further activity on the 1-Wire bus if executed. The DS2405 does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Skip ROM (for example, a DS2405 and DS1994 on the same bus).

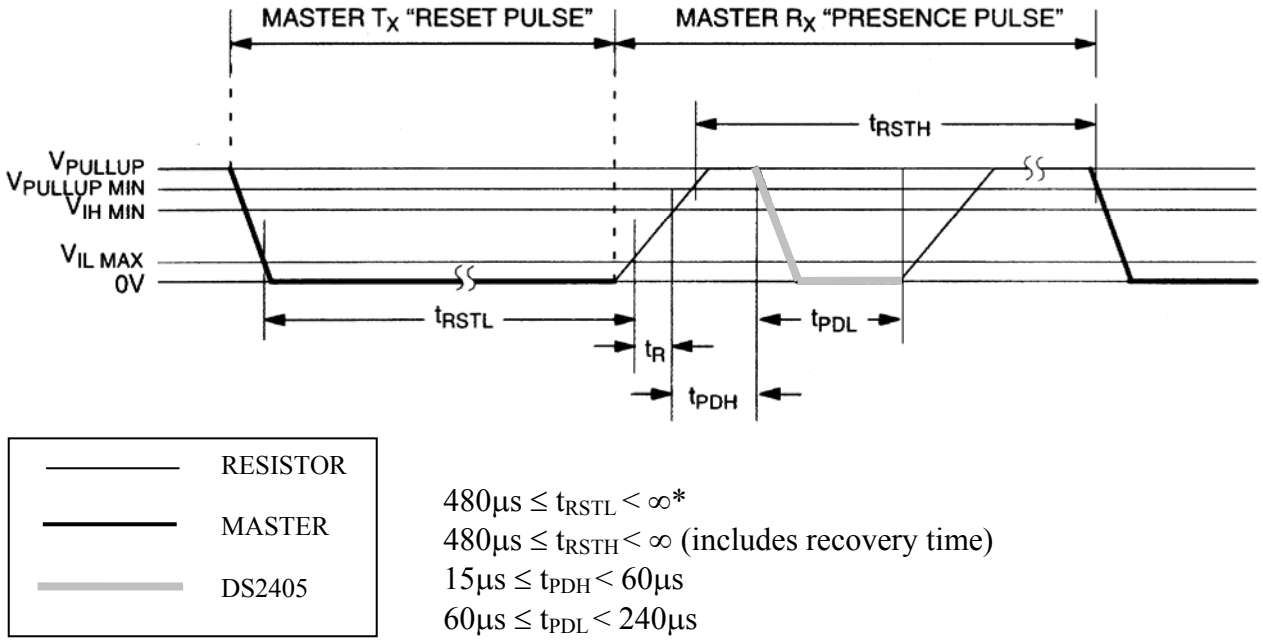
1-WIRE SIGNALING

The DS2405 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1 and read data. All these signals except Presence Pulse are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2405 is shown in Figure 5. A Reset Pulse followed by a Presence Pulse indicates the DS2405 is ready to send or receive data given the correct ROM command.

The bus master transmits (TX) a Reset Pulse (t_{RSTL}, minimum 480µs). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the 5kΩ pullup resistor. After detecting the rising edge on the data pin, the DS2405 waits (t_{PDH}, 15-60µs) and then transmits the Presence Pulse (t_{PDL}, 60-240µs).

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



480µs ≤ t_{RSTL} < ∞*
480µs ≤ t_{RSTH} < ∞ (includes recovery time)
15µs ≤ t_{PDH} < 60µs
60µs ≤ t_{PDL} < 240µs

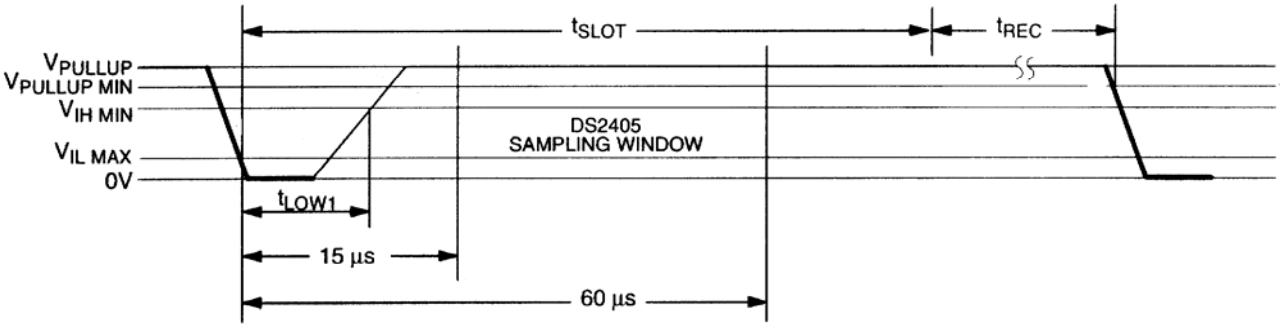
* In order not to mask interrupt signaling by other devices on the 1-Wire bus, t_{RSTL} + t_R should always be less than 960µs.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS2405 to the master by triggering a delay circuit in the DS2405. During write time slots, the delay circuit determines when the DS2405 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2405 will hold the data line low overriding the "1" generated by the master. If the data bit is a 1, the device will leave the read data time slot unchanged.

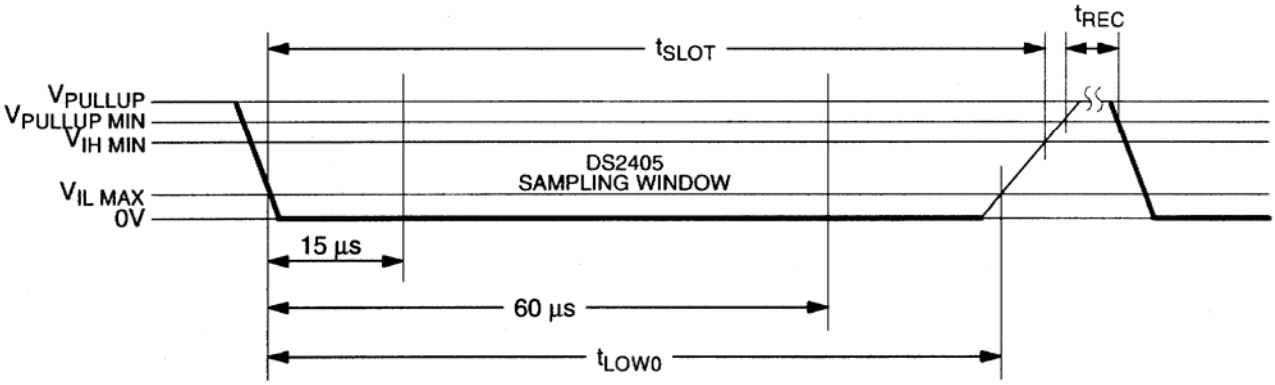
READ/WRITE TIMING DIAGRAM Figure 6

Write-1 Time Slot



$60\mu s \le t_{SLOT} < 120\mu s$
$1\mu s \le t_{LOW1} < 15\mu s$
$1\mu s \le t_{REC} < \infty$

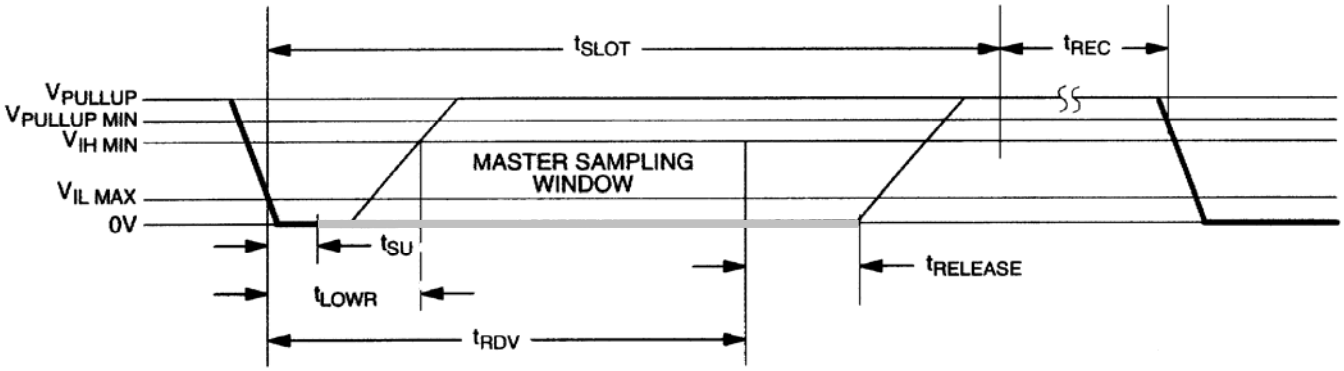
Write-0 Time Slot

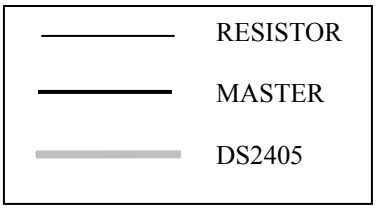


$60\mu s \le t_{LOW0} < t_{SLOT} < 120\mu s$
$1\mu s \le t_{REC} < \infty$

READ/WRITE TIMING DIAGRAM Figure 6 (cont.)

Read-Data Time Slot





$60\mu s \le t_{SLOT} < 120\mu s$
$1\mu s \le t_{LOWR} < 15\mu s$
$0 \le t_{RELEASE} < 45\mu s$
$1\mu s \le t_{REC} < \infty$
$t_{RDV} = 15\mu s$
$t_{SU} < 1\mu s$

CRC GENERATION

To validate the data transmitted from the DS2405, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the DS2405. If the two CRC values match, the transmission is error-free.

The equivalent polynomial function of this CRC is:

$CRC = x^8 + x^5 + x^4 + 1$

For more details, see the Book of DS19xx iButton Standards.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Solder Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} = 2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1,6,8
Logic 0	V_{IL}	-0.3		+0.8	V	1,10
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1,2
Input Load Current (DATA pin)	I_L		5		µA	3
Input Resistance (PIO pin)	I_R	10			MΩ	9

CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance DATA pin	C_D			800	pF	7
Capacitance PIO pin	C_P			10	pF	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} =2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write-1 Low Time	t_{LOW1}	1		15	µs	12
Write-0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	12
Read Data Valid	t_{RDV}		15		µs	11
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	13
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP} = external pullup voltage.

3. Input load is to ground.

4. An additional reset or communication sequence cannot begin until the reset high time has expired.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge and will remain valid for 14µs minimum (15µs total from falling edge on 1-Wire bus).

6. V_{IH} is a function of the external pull-up resistor and the V_{CC} supply.

7. Capacitance on the data pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull-up the data line to V_{CC}, 5µs after power has been applied the parasite capacitance will not affect normal communications.

8. V_{IH} for PIO pin should always be greater than or equal to V_{PUP} -0.3V.

9. Input resistance is to ground.

10. Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.

11. The optimal sampling point for the master is as close as possible to the end of the 15µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read 1 time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read 0 time slot, it ensures that a read will occur before the fastest 1-Wire device(s) release the line.

12. The duration of the low pulse sent by the master should be a minimum of 1µs with a maximum value as short as possible to allow time for the pull-up resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write 1 Low Time, or before the master samples in the case of a Read Low Time.

13. The Reset Low Time (t_{RSTL}) should be restricted to a maximum of 960µs to allow interrupt signaling; otherwise, it could mask or conceal interrupt pulses.