# 21–24 GHz GaAs MMIC Low Noise Amplifier



#### AA022N1-00

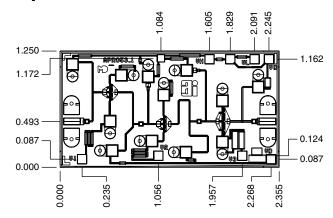
#### **Features**

- Single Bias Supply Operation (4.5 V)
- 2.6 dB Typical Noise Figure at 23 GHz
- 19 dB Typical Small Signal Gain
- 0.25 µm Ti/Pd/Au Gates
- 100% On-Wafer RF, DC and Noise Figure Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

#### **Description**

Alpha's three-stage reactively-matched 21–24 GHz MMIC low noise amplifier has typical small signal gain of 19 dB with a typical noise figure of 2.6 dB at 23 GHz. The chip uses Alpha's proven 0.25 µm low noise PHEMT technology, and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged reliable part with through-substrate via holes and gold-based backside metallization to facilitate a conductive epoxy die attach process.

# **Chip Outline**



Dimensions indicated in mm. All DC (V) pads are  $0.1 \times 0.1 \text{ mm}$  and RF In, Out pads are 0.07 mm wide. Chip thickness = 0.1 mm.

# **Absolute Maximum Ratings**

Characteristic	Value	
Operating Temperature (T <sub>C</sub> )	-55°C to +90°C	
Storage Temperature (T <sub>ST</sub> )	-65°C to +150°C	
Bias Voltage (V <sub>D</sub> )	6 V <sub>DC</sub>	
Power In (P <sub>IN</sub> )	10 dBm	
Junction Temperature (T <sub>J</sub> )	175°C	

# Electrical Specifications at $25^{\circ}$ C ( $V_{DS} = 4.5$ V)

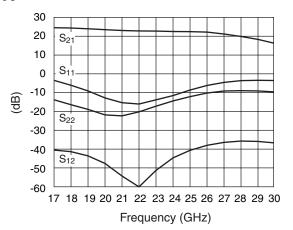
Parameter	Condition	Symbol	Min.	Typ. <sup>3</sup>	Max.	Unit
Drain Current		I <sub>DS</sub>		35	50	mA
Small Signal Gain	F = 21–24 GHz	G	16	19		dB
Noise Figure	F = 23 GHz	NF		2.6	2.8	dB
Input Return Loss	F = 21–24 GHz	RL		-7	-6	dB
Output Return Loss	F = 21–24 GHz	RLO		-14	-10	dB
Output Power at 1 dB Gain Compression <sup>1</sup>	F = 23 GHz	P <sub>1 dB</sub>		8		dBm
Thermal Resistance <sup>2</sup>		Θ <sub>JC</sub>		92		°C/W

<sup>1.</sup> Not measured on a 100% basis.

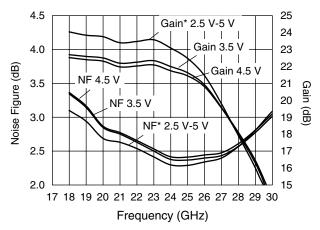
<sup>2.</sup> Calculated value based on measurement of discrete FET.

Typical represents the median parameter value across the specified frequency range for the median chip.

### **Typical Performance Data**

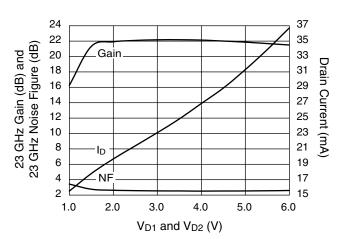


#### Typical Small Signal Performance S-Parameters (V<sub>D</sub> = 4.5 V)



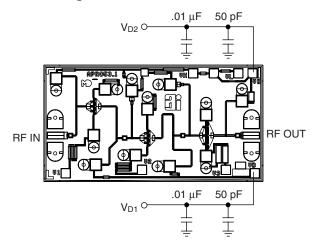
# Typical Gain and Noise Figure Performance for Three Bias Conditions

\*Special Bias:  $V_{D1} = 2.5 \text{ V}$ ,  $V_{D2} = 5.0 \text{ V}$ 



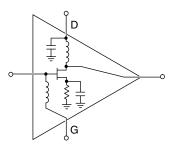
Typical Gain and Noise Figure Performance vs. Drain Bias  $(V_{D1} = V_{D2})$ 

### **Bias Arrangement**



For biasing on, adjust  $V_{DS}$  from zero to the desired value (4.5 V recommended). For biasing off, reverse the biasing on procedure.

#### **Circuit Schematic**



Detail A

