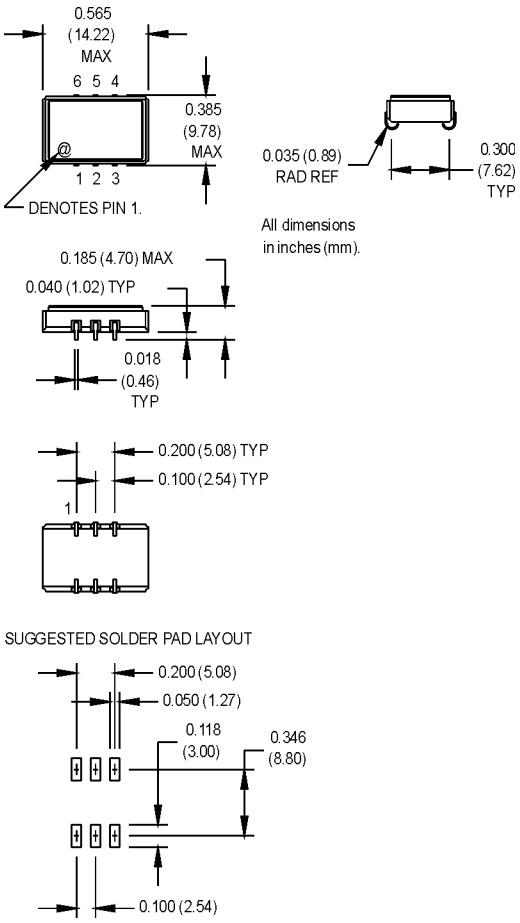
MPV3 Series
9x14 mm, 3.3 Volt, LVPECL/LVDS, VCXO

- Versatile VCXO to 800 MHz with good jitter (3 ps typical)
- Used in low jitter clock synthesizers and SONET applications



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable/Disable or N/C
3	Ground/Case
4	Output Q
5	Output $\overline{Q}$ or N/C
6	+Vcc

Ordering Information

MPV3 1 0 R 1 L J -R 00.0000 MHz

- **Product Series**
- **Temperature Range**
  - 1: 0°C to +70°C
  - 2: -40°C to +85°C
  - 6: -20°C to +70°C
  - 8: 0°C to +50°C
- **Stability**
  - 0: Nominal per APR selection
- **Output Type**
  - R: Complementary, Enable
  - Z: Complementary, w/o Enable
- **Absolute Pull Range**
  - 1: ±50 ppm (±35 ppm typ. Stability)
  - 2: ±100 ppm (±20 ppm typ. Stability)
  - 5: ±80 ppm (±25 ppm typ. Stability)
  - 8: ±25 ppm (±50 ppm typ. Stability)
- **Symmetry/Output Logic Type**
  - L: 45/55% LVDS
  - P: 45/55% PECL
  - H: 40/60% LVDS
  - Q: 40/60% PECL
- **Package/Lead Configurations**
  - J: J-lead
- **RoHS Compliance**
  - Blank: non-RoHS compliant part
  - -R: RoHS compliant part
- **Frequency (customer specified)**

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		800	MHz	
Operating Temperature	T_A	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
Aging						
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz
Pullability/APR		(See Ordering Information)				See Note 2
Control Voltage	Vc	0.3	1.65	3	V	Pin 1 voltage
Linearity			5	10	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	-3 dB bandwidth
Input Impedance	Zin	50k			Ohms	
Input Voltage	Vcc	3.135	3.3	3.465	V	
Input Current	Icc					
0.75 MHz to 26 MHz				60/30	mA	PECL/LVDS
26 MHz to 104 MHz				95/60	mA	PECL/LVDS
104 MHz to 800 MHz				105/60	mA	PECL/LVDS
Output Type						PECL/LVDS
Load		50 Ohms to Vcc -2 VDC 100 Ohm differential load				See Note 3 PECL waveform LVDS waveform
Symmetry (Duty Cycle)						Vcc -1.3 VDC (PECL)
(Per Symmetry Code)		(See Ordering Information)				50% of Waveform (LVDS)
Output Skew				200	ps	
Differential Voltage	Vo	250	340	450	mV	LVDS only
Logic "1" Level	Voh	Vcc -1.02			V	PECL
Logic "0" Level	Vol			Vcc -1.63	V	PECL
Rise/Fall Time	Tr/Tf		0.35	0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable Function		80% Vcc min or N/C: output active 20% Vcc max: output disables to high-Z				
Start up Time			5		ps	
Phase Jitter	ϕJ		3	5	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)	**10 Hz**	**100 Hz**	**1 kHz**	**10 kHz**	**100 kHz**	**Offset from carrier**
@ 19.44 MHz	-60	-90	-112	-140	-150	dBc/Hz
@ 155.52 MHz	-60	-90	-112	-123	-120	dBc/Hz
@ 622.08 Mhz	-60	-90	-108	-108	-105	dBc/Hz

1. Stability given for deviation over temperature.
2. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.
3. PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

MtronPTI Lead Free Solder Profile