Integrated Device Technology, Inc.

# FAST CMOS 12-BIT TRI-PORT BUS EXCHANGER

**IDT54/74FCT16260AT/CT/ET**
**IDT54/74FCT162260AT/CT/ET**

## FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
  - Extended commercial range of -40°C to +85°C
  - $V_{CC}$ = 5V ±10%
- **Features for FCT16260AT/CT/ET:**
  - High drive outputs (-32mA $I_{OH}$, 64mA $I_{OL}$)
  - Power off disable outputs permit "live insertion"
  - Typical $V_{OLP}$ (Output Ground Bounce) < 1.0V at $V_{CC}$ = 5V, $T_A$ = 25°C
- **Features for FCT162260AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical $V_{OLP}$ (Output Ground Bounce) < 0.6V at $V_{CC}$ = 5V, $T_A$ = 25°C

## DESCRIPTION:

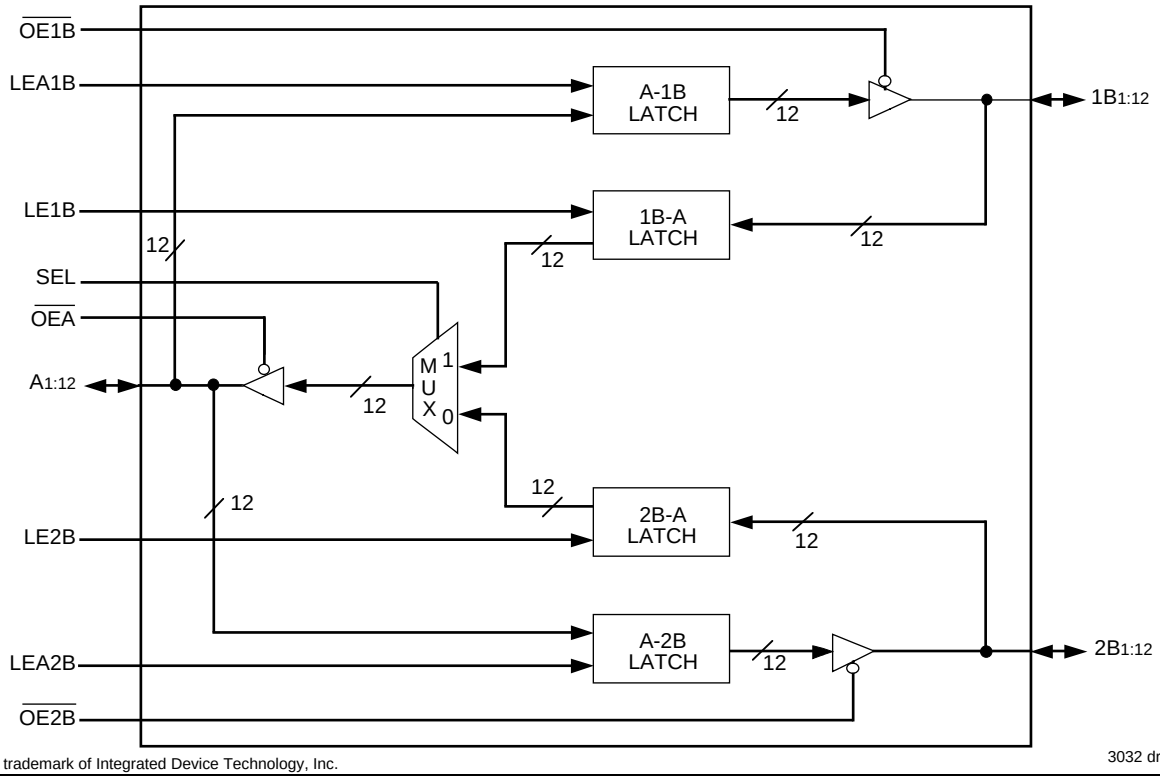
The FCT16260AT/CT/ET and the FCT162260AT/CT/ET Tri-Port Bus Exchangers are high-speed 12-bit latched bus multiplexers/transceivers for use in high-speed microprocessor applications. These Bus Exchangers support memory interleaving with latched outputs on the B ports and address multiplexing with latched inputs on the B ports.

The Tri-Port Bus Exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The latch enable (LE1B, LE2B, LEA1B and LEA2B) inputs control data storage. When a latch-enable input is HIGH, the latch is transparent. When a latch-enable input is LOW, the data at the input is latched and remains latched until the latch enable input is returned HIGH. Independent output enables ($\overline{OE1B}$ and $\overline{OE2B}$) allow reading from one port while writing to the other port.

The FCT16260AT/CT/ET are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162260AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times - reducing the need for external series terminating resistors.

## FUNCTIONAL BLOCK DIAGRAM




3032 drw 01

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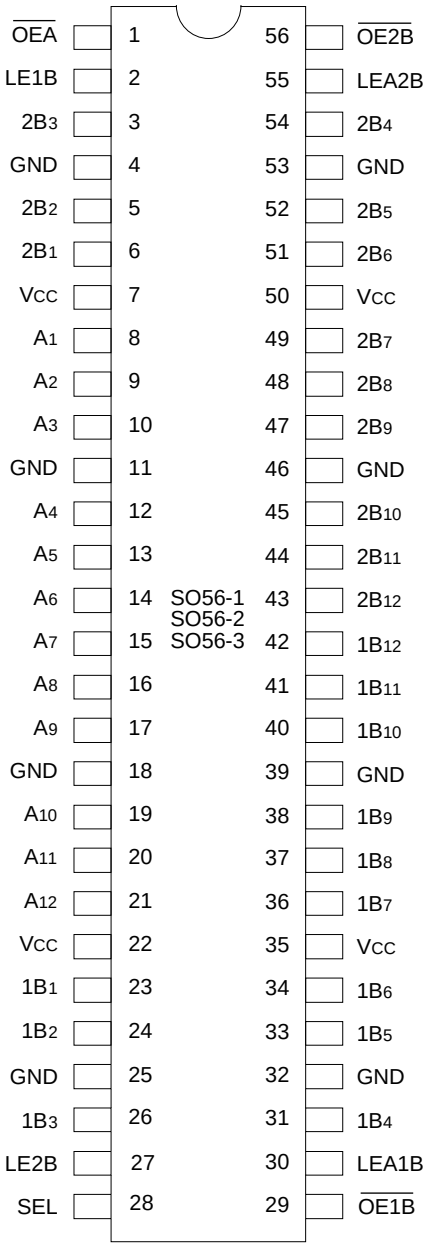
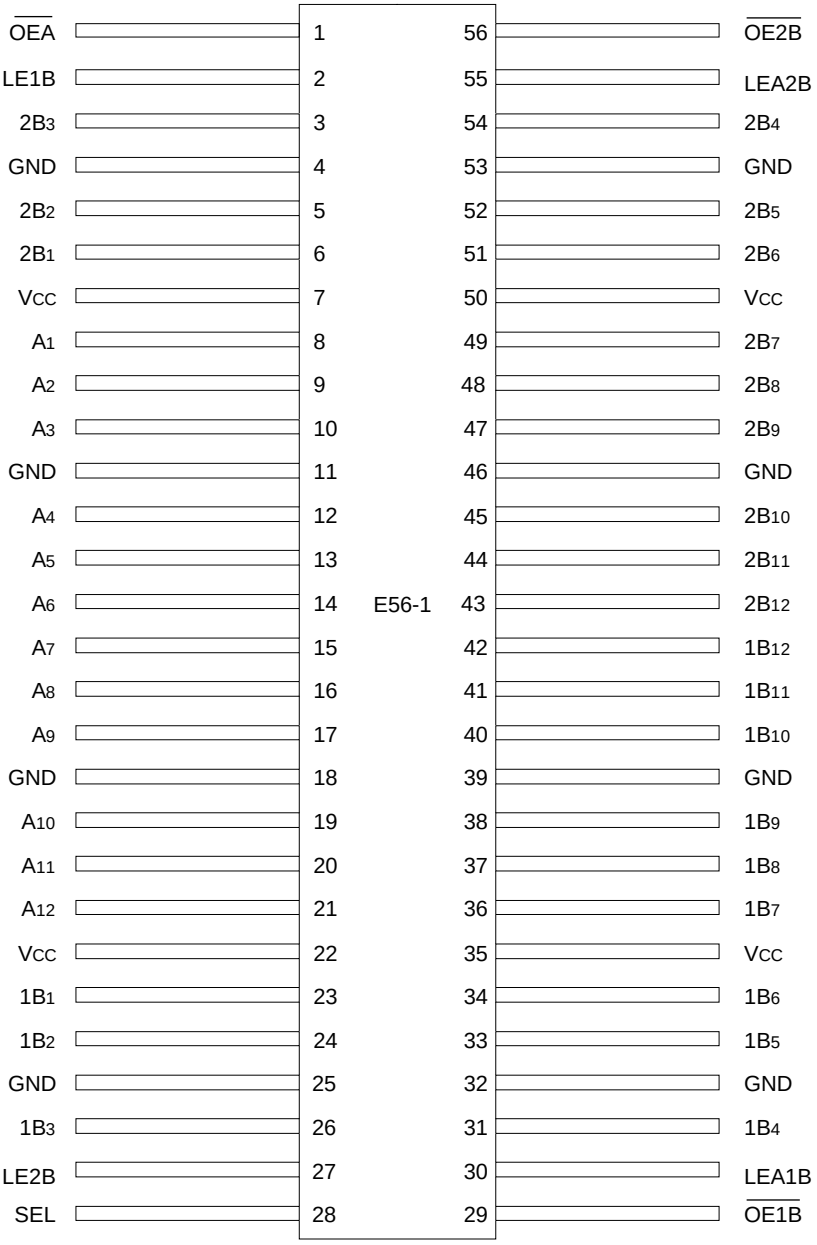
## PIN CONFIGURATIONS




**SSOP/ TSSOP/TVSOP TOP VIEW**

3032 drw 02




**CERPACK TOP VIEW**

3032 drw 03

## PIN DESCRIPTION

| Signal | I/O | Description |
|---|---|---|
| A(1:12) | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. |
| 1B(1:12) | I/O | Bidirectional Data Port 1B. Connected to the even path or even bank of memory. |
| 2B(1:12) | I/O | Bidirectional Data Port 2B. Connected to the odd path or odd bank of memory. |
| LEA1B | I | Latch Enable Input for A-1B Latch. The Latch is open when LEA1B is HIGH. Data from the A-port is latched on the HIGH to LOW transition of LEA1B. |
| LEA2B | I | Latch Enable Input for A-2B Latch. The Latch is open when LEA2B is HIGH. Data from the A-Port is latched on the HIGH to LOW transition of LEA2B. |
| LE1B | I | Latch Enable Input for the 1B-A Latch. The Latch is open when LE1B is HIGH. Data from the 1B port is latched on the HIGH to LOW transition of LE1B. |
| LE2B | I | Latch Enable Input for the 2B-A Latch. The Latch is open when LE2B is HIGH. Data from the 2B port is latched on the HIGH to LOW transition of LE2B. |
| SEL | I | 1B or 2B Path Selection. When HIGH, SEL enables data transfer from 1B Port to A Port. When LOW, SEL enables data transfer from 2B Port to A Port. |
| $\overline{OEA}$ | I | Output Enable for A Port (Active LOW). |
| $\overline{OE1B}$ | I | Output Enable for 1B Port (Active LOW). |
| $\overline{OE2B}$ | I | Output Enable for 2B Port (Active LOW). |

3032 tbl 01

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ +0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +120 | mA |

3032 tbl 02

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 3.5 | 6.0 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 0V | 3.5 | 8.0 | pF |

3032 tbl 03

**NOTE:**
1. This parameter is measured at characterization but not tested.

## FUNCTION TABLES(2)

| Inputs | | | | | | Output |
|---|---|---|---|---|---|---|
| 1B | 2B | SEL | LE1B | LE2B | $\overline{OEA}$ | A |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | A(1) |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | A(1) |
| X | X | X | X | X | H | Z |

3032 tbl 04

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| A | LEA1B | LEA2B | $\overline{OE1B}$ | $\overline{OE2B}$ | 1B | 2B |
| H | H | H | L | L | H | H |
| L | H | H | L | L | L | L |
| H | H | L | L | L | H | B(1) |
| L | H | L | L | L | L | B(1) |
| H | L | H | L | L | B(1) | H |
| L | L | H | L | L | B(1) | L |
| X | L | L | L | L | B(1) | B(1) |
| X | X | X | H | H | Z | Z |
| X | X | X | L | H | Active | Z |
| X | X | X | H | L | Z | Active |
| X | X | X | L | L | Active | Active |

3032 tbl 05

**NOTES:**
1. Output level before the indicated steady-state input conditions were established.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ± 10%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current (Input pins)[5] | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| | Input HIGH Current (I/O pins)[5] | | | — | — | ±1 | |
| $I_{IL}$ | Input LOW Current (Input pins)[5] | | $V_I$ = GND | — | — | ±1 | |
| | Input LOW Current (I/O pins)[5] | | | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[5] | | $V_O$ = 0.5V | — | — | ±1 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | –80 | –140 | –225 | mA |
| $V_H$ | Input Hysteresis | — | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 5 | 500 | µA |

3032 tbl 06

## OUTPUT DRIVE CHARACTERISTICS FOR FCT16260T

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_O$ | Output Drive Current | $V_{CC}$ = Max., $V_O$ = 2.5V[3] | | –50 | — | –180 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –3mA | 2.5 | 3.5 | — | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –12mA MIL.<br>$I_{OH}$ = –15mA COM'L. | 2.4 | 3.5 | — | V |
| | | | $I_{OH}$ = –24mA MIL.<br>$I_{OH}$ = –32mA COM'L.[4] | 2.0 | 3.0 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 48mA MIL.<br>$I_{OL}$ = 64mA COM'L. | — | 0.2 | 0.55 | V |
| $I_{OFF}$ | Input/Output Power Off Leakage[5] | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 4.5V | | — | — | ±1 | µA |

3032 tbl 07

## OUTPUT DRIVE CHARACTERISTICS FOR FCT162260T

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{ODL}$ | Output LOW Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | 60 | 115 | 200 | mA |
| $I_{ODH}$ | Output HIGH Current | $V_{CC}$ = 5V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 1.5V[3] | | –60 | –115 | –200 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –16mA MIL.<br>$I_{OH}$ = –24mA COM'L. | 2.4 | 3.3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA MIL.<br>$I_{OL}$ = 24mA COM'L. | — | 0.3 | 0.55 | V |

3032 lnk 08

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at $T_A$ = –55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>One Output Port Enabled<br>LExx = $V_{CC}$<br>One Input Bit Toggling<br>One Output Bit Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 60 | 100 | µA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>fi = 10MHz | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.6 | 1.5 | mA |
| | | 50% Duty Cycle<br>One Output Port Enabled<br>LExx = $V_{CC}$<br>One Input Bit Toggling<br>One Output Bit Toggling | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 0.9 | 2.3 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>fi = 2.5MHz | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.8 | 3.5[5] | |
| | | 50% Duty Cycle<br>One Output Port Enabled<br>LExx = $V_{CC}$<br>Twelve Input Bits Toggling<br>Twelve Output Bits Toggling | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 4.8 | 12.5[5] | |

3032 tbl 09

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $N_{CP}$ = Number of Clock Inputs at $f_{CP}$
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | FCT16260AT/162260AT | | | | FCT16260CT/162260CT | | | | FCT16260ET/162260ET | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Ax to 1Bx or Ax to 2Bx | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 5.2 | 1.5 | 5.6 | 1.5 | 4.7 | 1.5 | 5.1 | 1.5 | 3.6 | — | — | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>1Bx to Ax or 2Bx to Ax | | 1.5 | 5.6 | 1.5 | 5.9 | 1.5 | 5.0 | 1.5 | 5.4 | 1.5 | 3.6 | — | — | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LExB to Ax | | 1.5 | 5.2 | 1.5 | 5.6 | 1.5 | 4.7 | 1.5 | 5.1 | 1.5 | 4.0 | — | — | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>LEA1B to 1Bx or<br>LEA2B to 2Bx | | 1.5 | 4.7 | 1.5 | 5.2 | 1.5 | 4.4 | 1.5 | 4.8 | 1.5 | 4.0 | — | — | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>SEL to Ax | | 1.5 | 5.2 | 1.5 | 5.6 | 1.5 | 4.7 | 1.5 | 5.1 | 1.5 | 4.0 | — | — | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OEA}$ to Ax, $\overline{OE1B}$ to 1Bx, or<br>$\overline{OE2B}$ to 2Bx | | 1.5 | 5.7 | 1.5 | 6.1 | 1.5 | 5.1 | 1.5 | 5.4 | 1.5 | 4.4 | — | — | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>$\overline{OEA}$ to Ax, $\overline{OE1B}$ to 1Bx, or<br>$\overline{OE2B}$ to 2Bx | | 1.5 | 4.4 | 1.5 | 4.8 | 1.5 | 4.0 | 1.5 | 4.4 | 1.5 | 4.0 | — | — | ns |
| $t_{SU}$ | Set-Up Time, HIGH or LOW<br>Data to Latch | | 1.5 | — | 1.5 | — | 1.0 | — | 1.0 | — | 1.0 | — | — | — | ns |
| $t_H$ | Hold Time, Latch to Data | | 1.0 | — | 1.5 | — | 1.0 | — | 1.5 | — | 1.0 | — | — | — | ns |
| $t_W$ | Pulse Width, Latch HIGH[4] | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | — | — | ns |
| $t_{SK}(o)$ | Output Skew[3] | | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | — | ns |

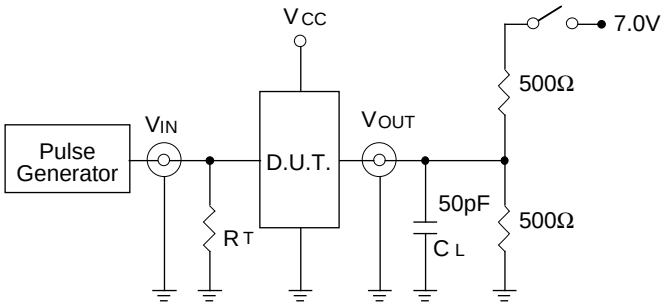
**NOTES:**

3032 tbl 10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS




3032 lnk 04

### SWITCH POSITION

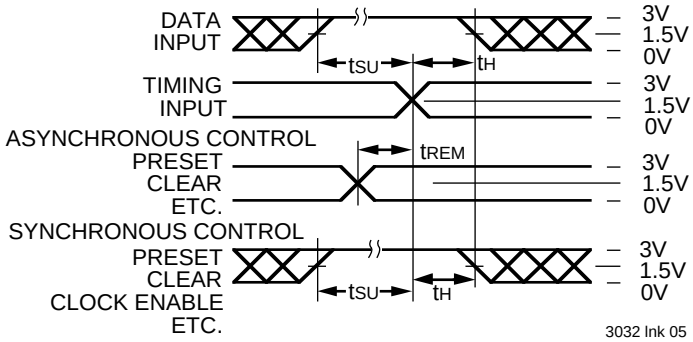
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

3032 lnk 11

**DEFINITIONS:**

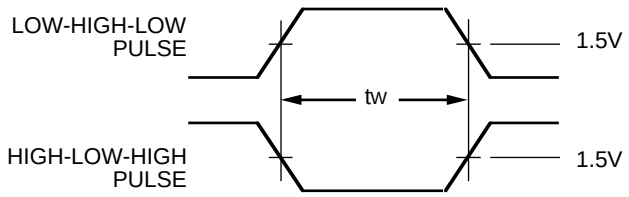
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



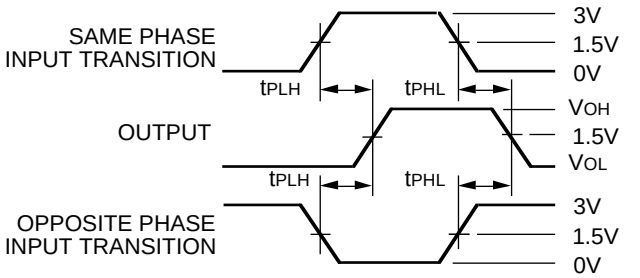

3032 lnk 05

## PULSE WIDTH



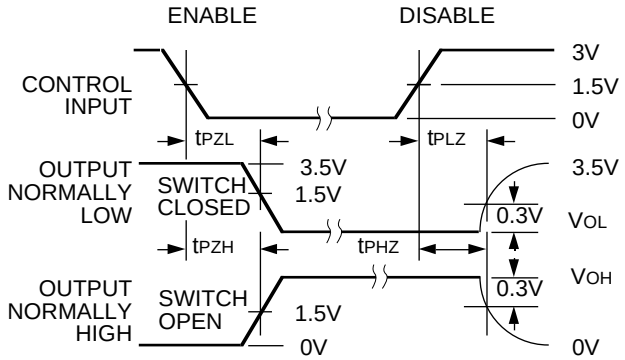

3032 lnk 06

## PROPAGATION DELAY




3032 lnk 07

## ENABLE AND DISABLE TIMES

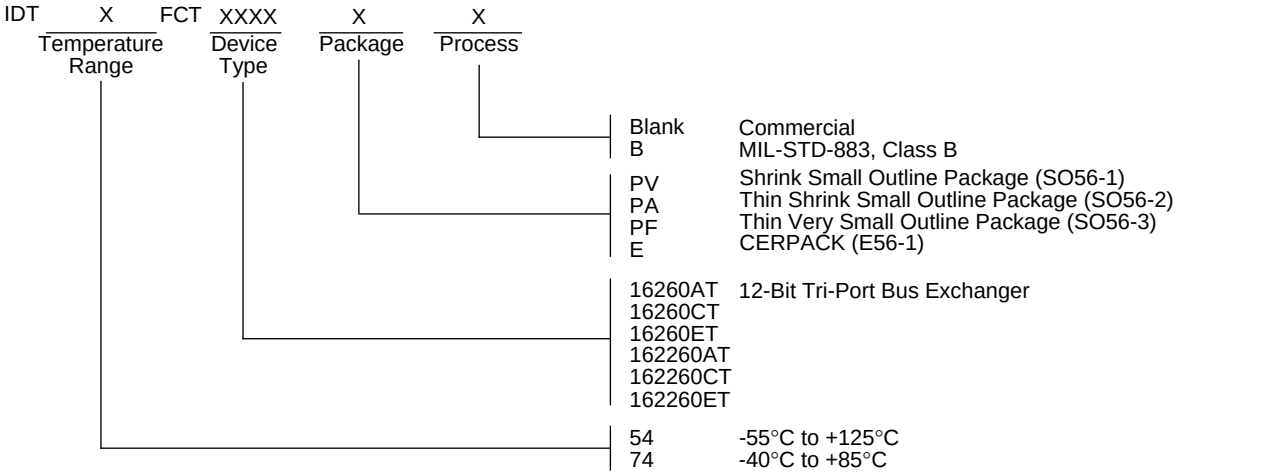



3032 lnk 08

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

## ORDERING INFORMATION

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