

NTGD1100L

Power MOSFET

8 V, ±3.3 A, Load Switch with Level-Shift, P-Channel, TSOP-6

The NTGD1100L integrates a P and N-Channel MOSFET in a single package. This device is particularly suited for portable electronic equipment where low control signals, low battery voltages and high load currents are needed. The P-Channel device is specifically designed as a load switch using ON Semiconductor state-of-the-art trench technology. The N-Channel, with an external resistor (R1), functions as a level-shift to drive the P-Channel. The N-Channel MOSFET has internal ESD protection and can be driven by logic signals as low as 1.5 V. The NTGD1100L operates on supply lines from 1.8 to 8.0 V and can drive loads up to 3.3 A with 8.0 V applied to both V_{IN} and $V_{ON/OFF}$

Features

- Extremely Low $R_{DS(on)}$ Load Switch MOSFET
- Level Shift MOSFET is ESD Protected
- Low Profile, Small Footprint Package
- V_{IN} Range 1.8 to 8.0 V
- ON/OFF Range 1.5 to 8.0 V
- ESD Rating of 3000 V
- Pb-Free Package is Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit	
Input Voltage (V_{DSS} , P-Ch)		V_{IN}	8.0	V	
ON/OFF Voltage (V_{GS} , N-Ch)		$V_{ON/OFF}$	8.0	V	
Continuous Load Current (Note 1)	Steady State	I_L	$T_A = 25^\circ\text{C}$	±3.3	A
			$T_A = 85^\circ\text{C}$	±2.4	
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	0.83	W
			$T_A = 85^\circ\text{C}$	0.43	
Pulsed Load Current	$tp = 10 \mu\text{s}$	I_{LM}	±10	A	
Operating Junction and Storage Temperature		T_J , T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	-1.0	A	
ESD Rating, MIL-STD-883D HBM (100 pF, 1.5 kΩ)		ESD	3.0	kV	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	150	$^\circ\text{C}/\text{W}$
Junction-to-Foot – Steady State (Note 1)	$R_{\theta JF}$	50	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

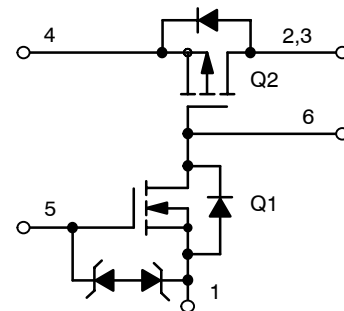


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
8.0 V	40 mΩ @ -4.5 V	±3.3 A
	55 mΩ @ -2.5 V	
	80 mΩ @ -1.8 V	

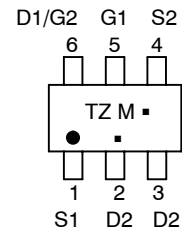
SIMPLIFIED SCHEMATIC



MARKING DIAGRAM & PIN ASSIGNMENT



1
TSOP-6
CASE 318G
STYLE 11



TZ = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTGD1100LT1	TSOP-6	3000/Tape & Reel
NTGD1100LT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	
OFF CHARACTERISTICS							
Q2 Drain-to-Source Breakdown Voltage	V_{IN}	$V_{GS2} = 0\text{ V}, I_{D2} = 250\ \mu\text{A}$	8.0			V	
Forward Leakage Current	I_{FL}	$V_{GS2} = 0\text{ V}, V_{DS2} = 8.0\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA	
			$T_J = 125^\circ\text{C}$		10		
Q1 Gate-to-Source Leakage Current	I_{GSS}	$V_{DS1} = 0\text{ V}, V_{GS1} = \pm 8.0\text{ V}$			± 100	nA	
Q1 Diode Forward On-Voltage	V_{SD}	$I_S = -1.0\text{ A}, V_{GS1} = 0\text{ V}$		-0.7	-1.0	V	
ON CHARACTERISTICS							
Voltage ON/OFF	$V_{ON/OFF}$		1.5		8.0	V	
Q1 Gate Threshold Voltage	V_{GS1}	$V_{GS1} = V_{DS1}, I_D = 50\ \mu\text{A}$	0.6		1.2	V	
Input Voltage	V_{IN}	$V_{GS2} = V_{DS2}, I_D = 250\ \mu\text{A}$	1.8		8.0	V	
Q2 Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{ON/OFF} = 1.5\text{ V}, I_L = 1.0\text{ A}$	$V_{IN} = 4.5\text{ V}$		40	55	$\text{m}\Omega$
			$V_{IN} = 2.5\text{ V}$		55	70	
			$V_{IN} = 1.8\text{ V}$		80	140	
Load Current	I_L	$V_{DROP} \leq 0.2\text{ V}, V_{IN} = 5.0\text{ V}, V_{ON/OFF} = 1.5\text{ V}$		1.0		A	
			$V_{DROP} \leq 0.2\text{ V}, V_{IN} = 2.5\text{ V}, V_{ON/OFF} = 1.5\text{ V}$	1.0			
			$V_{DROP} \leq 0.2\text{ V}, V_{IN} = 1.8\text{ V}, V_{ON/OFF} = 1.5\text{ V}$	1.0			

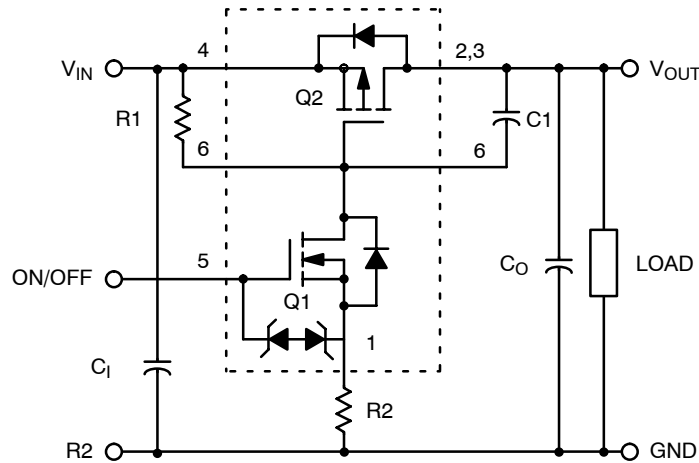


Figure 1. Load Switch Application

Components	Description	Values
R1	Pullup Resistor	Typical 10 k Ω to 1.0 M Ω
R2	Optional Slew-Rate Control	Typical 0 to 100 k Ω
C0	Output Capacitance	Usually < 1.0 μF
C1	Optional In-Rush Current Control	Typical $\leq 1000\ \text{pF}$

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TYPICAL CHARACTERISTICS

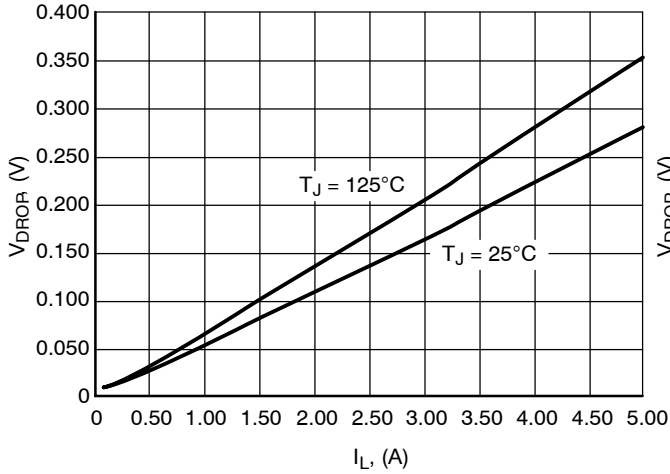


Figure 2. V_{DROP} vs. I_L @ $V_{IN} = 2.5\text{ V}$

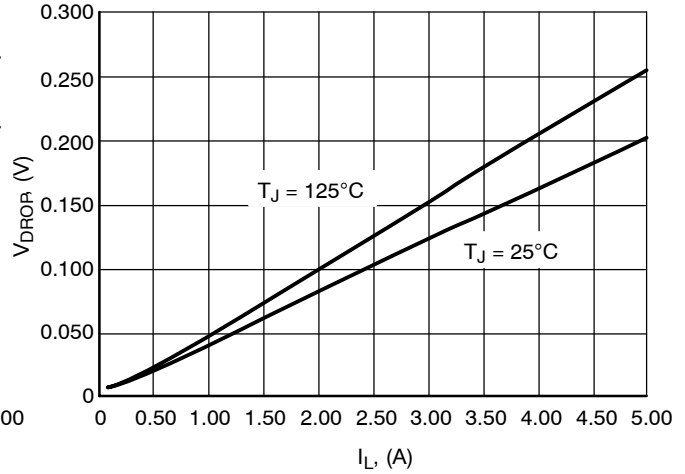


Figure 3. V_{DROP} vs. I_L @ $V_{IN} = 4.5\text{ V}$

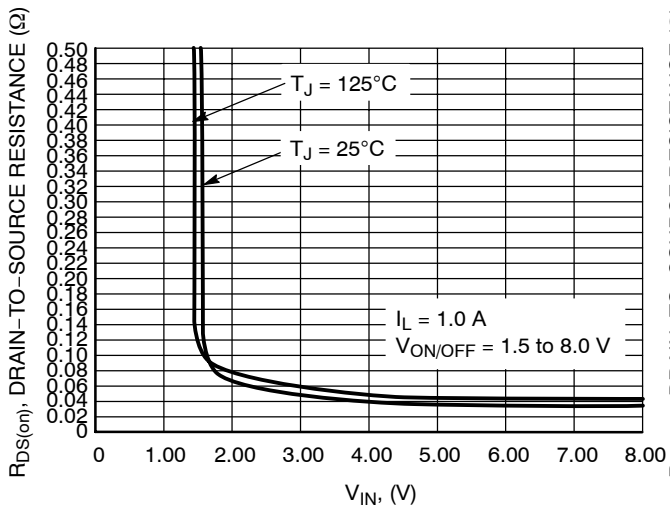


Figure 4. On Resistance vs. Input Voltage

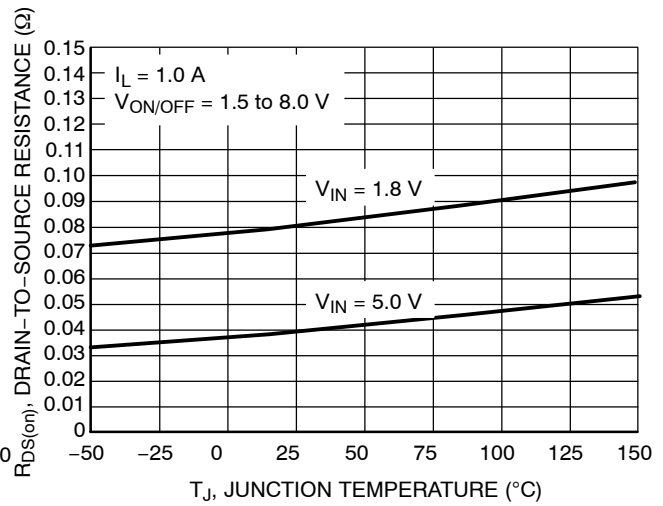


Figure 5. On Resistance Variation with Temperature

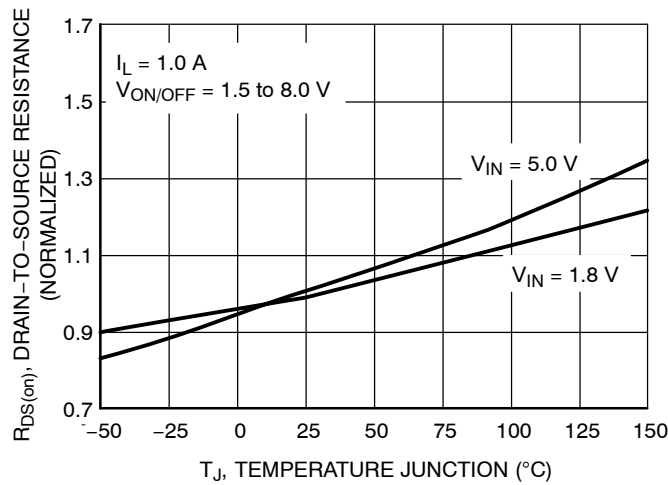
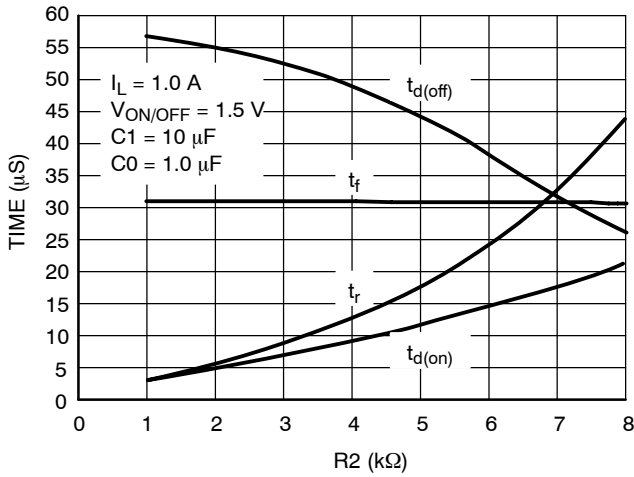


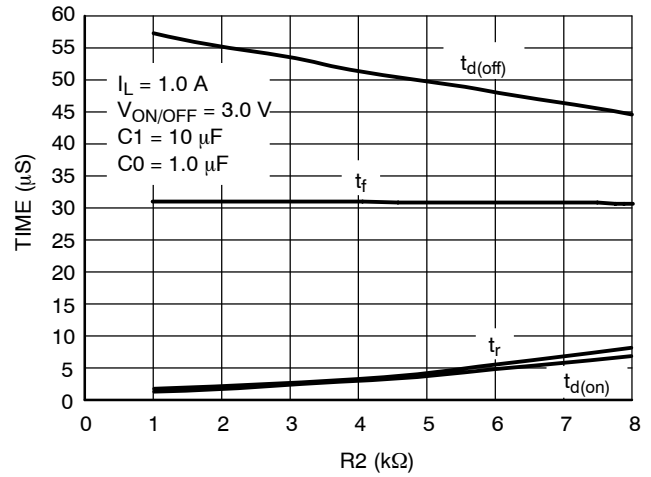
Figure 6. Normalized On Resistance Variation with Temperature

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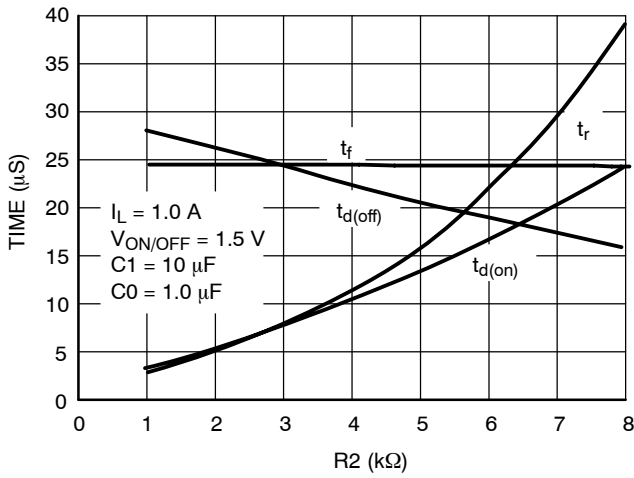
TYPICAL CHARACTERISTICS



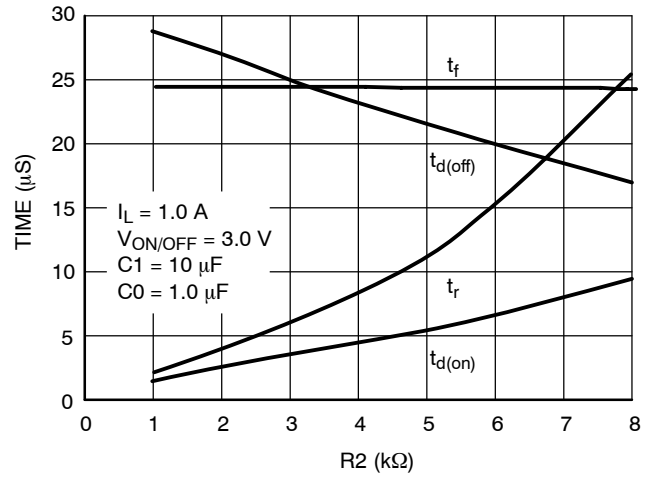
**Figure 7. Switching Variation R2 @
V_{IN} = 4.5 V, R1 = 20 kΩ**



**Figure 8. Switching Variation R2 @
V_{IN} = 4.5 V, R1 = 20 kΩ**



**Figure 9. Switching Variation R2 @
V_{IN} = 2.5 V, R1 = 20 kΩ**



**Figure 10. Switching Variation R2 @
V_{IN} = 2.5 V, R1 = 20 kΩ**

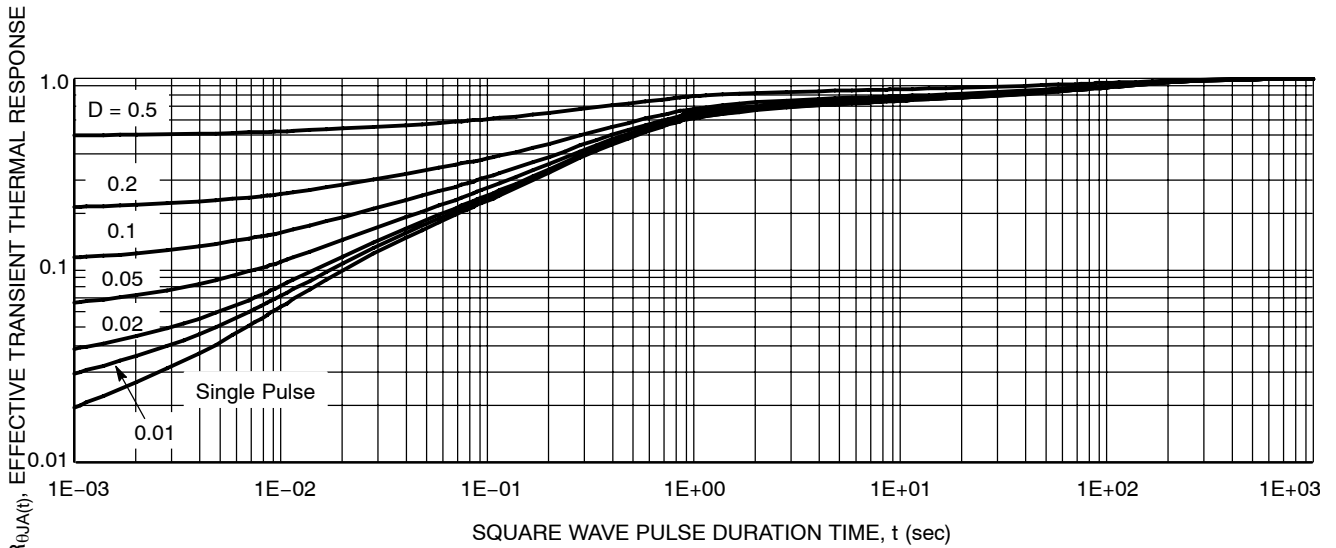
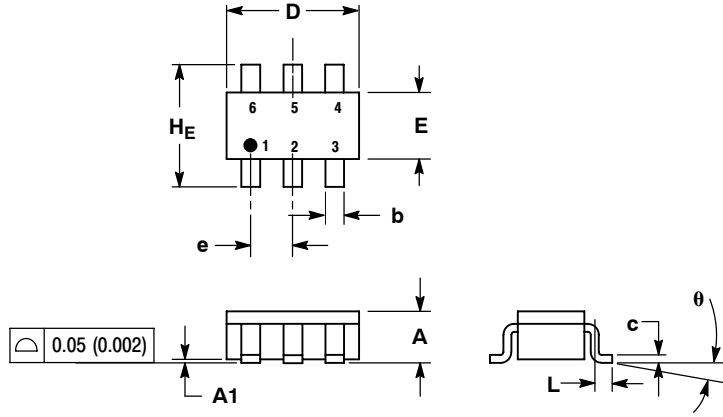


Figure 11. FET Thermal Response Normalized to R_{θJA} at Steady State (1 inch Pad)

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PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE P



NOTES:

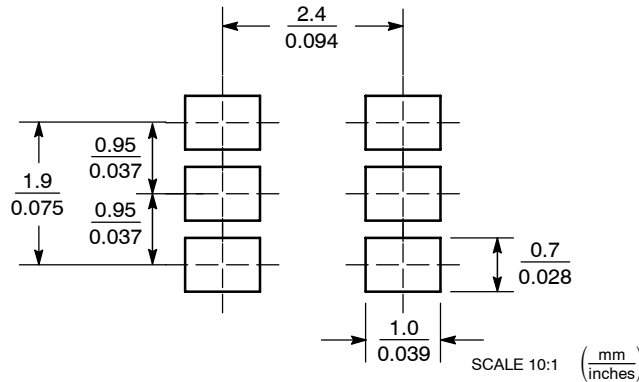
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
theta	0°	-	10°	0°	-	10°

STYLE 11:

- PIN 1. SOURCE 1
- DRAIN 2
- DRAIN 2
- SOURCE 2
- GATE 1
- DRAIN 1/GATE 2

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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