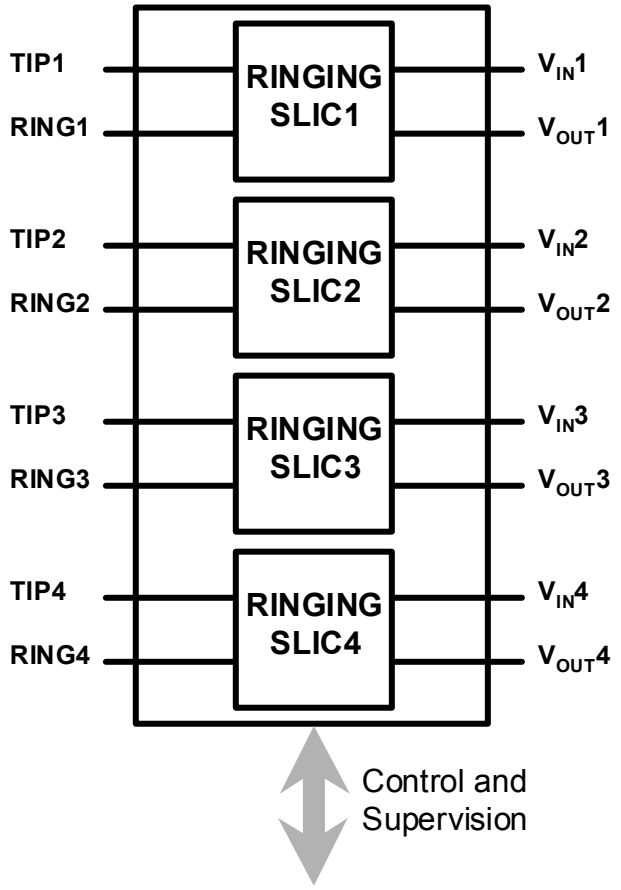
Silver TELECOM

Ag1460
QUAD 5V RINGING SLIC



FEATURES

- Four highly featured SLICs in a 72 pin SIMM or 56 pin DIL format.
- Integral DC-DC converter. No battery voltage supply needed.
- Highly integrated with on board ringing generator.
- Tip/Ring polarity reversal, On-Hook Transmission for caller line ID.
- “Soft Shutdown” over current and thermal protection provides fail-safe operation.
- Minimum number of external components.
- Simplified protection in “on-premise” applications.
- Silver Telecom “design-in” assistance.

DESCRIPTION

The Silver Telecom Ag1460 series comprises four individual single Subscriber Line Interface Circuits (SLICs) in a 72-pin SIMM or 56 pin DIL format. The combination of features and packaging offers extremely efficient use of board area, saving significant system size and cost, maximising time to market for Telephony Systems developers.

The Ag1460 has been designed to work with loop lengths of up to 3.0km (800Ω including telephone), with both resistive and complex line impedances. Its performance to regulatory standards allows use in public and private network applications.

The Ag1460 has integral dc/dc converter and ringing generation thus providing all the line powering requirements from a single supply. The SLIC requires a minimum of external components.

The system interface has been designed for connection to all popular codecs of both the audio and signalling connections.

The Ag1460 is ideal for low line count, short loop length applications, such as ISDN Terminal Adaptors, Internet Telephony (VoIP), Computer Telephony Integration (CTI), Digital Loop Carriers (DLC), Wireless Local Loops (WLL) and Small Office Home Office (SOHO).

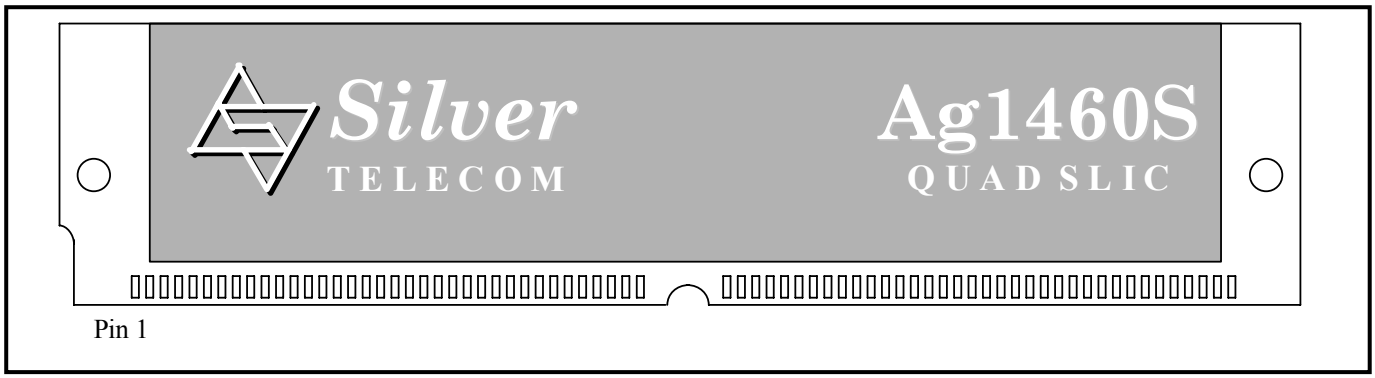


Figure 1: SIL Package

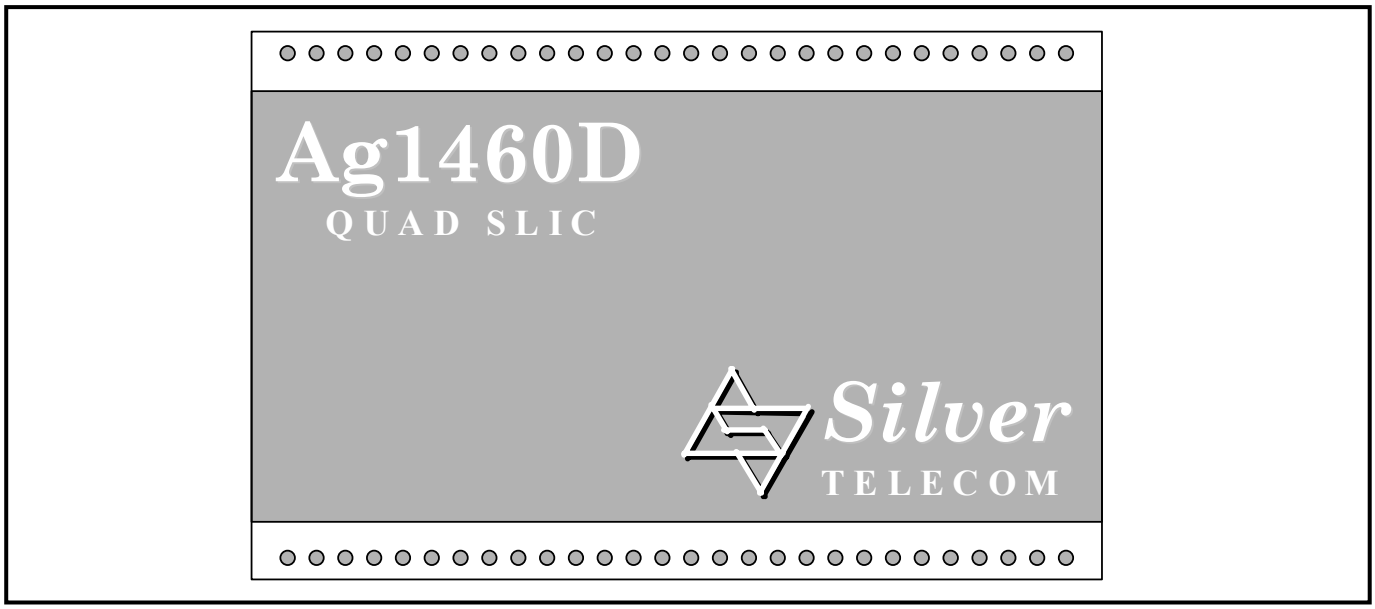


Figure 2: DIL Package

Ordering Information

Ag1460D	Quad +5V Ringing SLIC, fixed 600Ω impedance. 56 pin DIL Package.
Ag1460S	Quad +5V Ringing SLIC, fixed 600Ω impedance. 72 pin SIMM Package.
Ag1460PD	Quad +5V Ringing SLIC, programmable impedance. 56 pin DIL Package.
Ag1460PS	Quad +5V Ringing SLIC, programmable impedance. 72 pin SIMM Package.

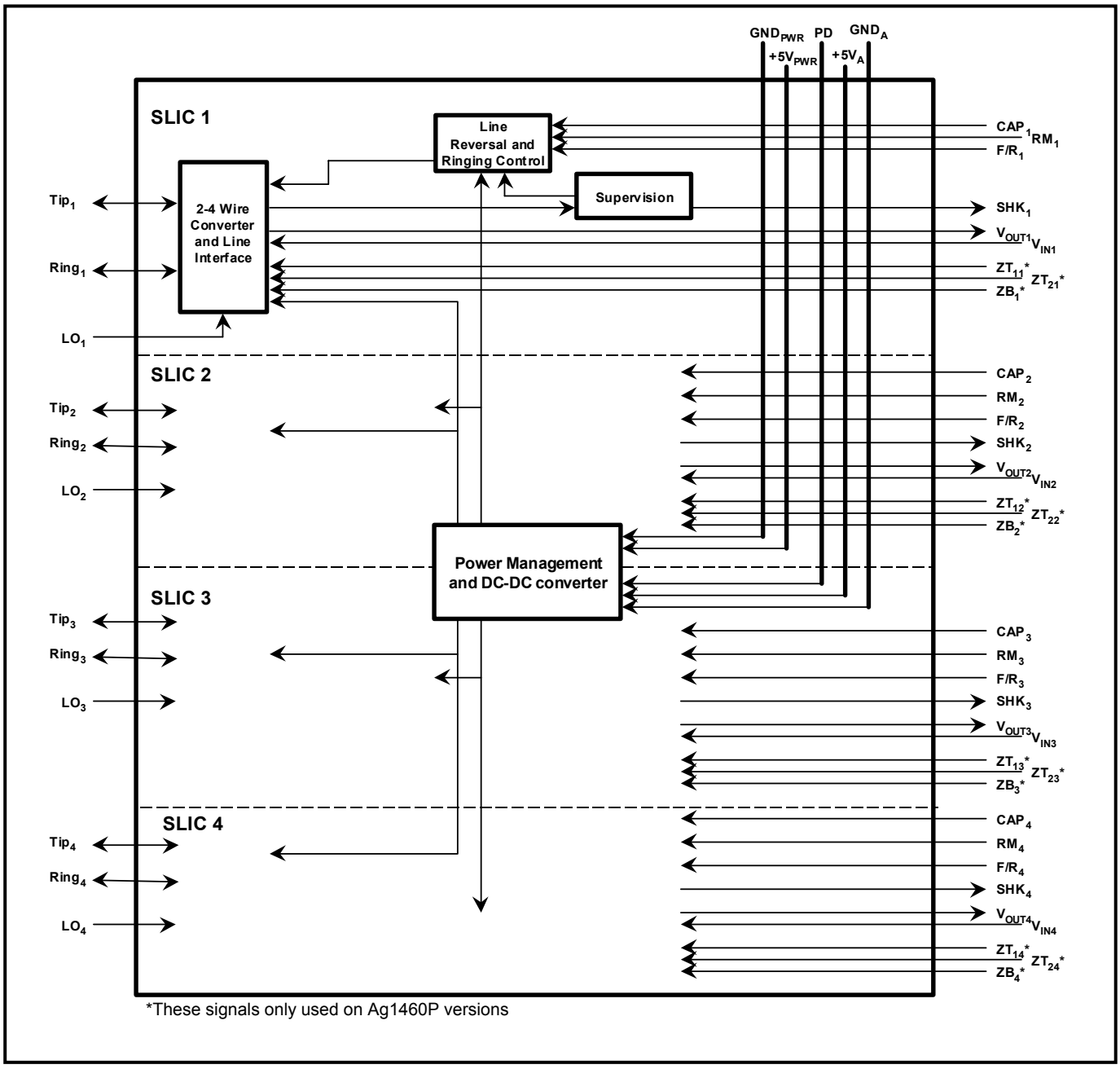


Figure 2: Functional Block Diagram

1.0 Pin Description

1.1 SIMM Format Pin Out

Pin #	Name	Description
1, 19, 38, 56	F/R	**Forward/Reverse.** A logic 0 will reverse the Tip and Ring voltage polarities. F/R is toggled to produce the ringing output.
2, 20, 39, 57	TIP (A)	**Tip.** Connects to the subscriber line Tip.
3, 21, 40, 58	RING (B)	**Ring.** Connects to the subscriber line Ring.
4, 22, 41, 59	LO	**Loop Off.** A logic 1 removes the loop current from the line. Connect to logic 0 for normal operation.
5, 18, 55, 60	$+5V_A$	**Analog Supply.** Each pin must be connected to $+5V_{PWR}$ with 10Ω resistors. Decouple each with 100uF (16V) capacitors.
6, 7, 8, 37, 61, 62, 63	NC	**No Connection.** These pins are not connected internally to the device.
9, 27, 46, 64	V_{IN}	**Audio In.** This is the analog input signal from the Codec (which is output on Tip and Ring). Must be ac coupled with typically 100nF.
10, 28, 47, 65	GND_A	**Analog Ground.** Normally connected to system ground. All 4 pins must be connected to analog ground by separate tracks or ground plane.
11, 29, 48, 66	V_{OUT}	**Audio Out.** This is the analog output signal (from Tip and Ring) to the Codec. Must be ac coupled with typically 100nF.
12, 30, 49, 67	SHK	**Switch Hook.** Indicates Off-Hook when at logic 1. Must be de-bounced
13, 31, 50, 68	CAP	**Slew Rate Capacitor.** A capacitor is fitted between this pin and GND to control the battery reversal and the ringing slew rate. 220nF is recommended.
14, 32, 51, 69	RM	**Ringing Mode.** Sets bias conditions during ringing. Must be set to logic 1 during ringing. Must be set to logic 0 within 500ms of Ring Trip detect and during normal Off Hook condition.
15, 33, 52, 70	ZT_1*	**Terminal Impedance 1.** Connect programming components between ZT_1 and ZT_2 on Ag1460P only.*
16, 34, 53, 71	ZT_2*	**Terminal Impedance 2.** Connect programming components between ZT_1 and ZT_2 on Ag1460P only.*
17, 35, 54, 72	ZB*	**Balance Impedance.** Connect programming components between ZB and V_{IN} on Ag1460P only.*
23, 24, 25, 26	$+5V_{PWR}$	**DC-DC Supply.** +5V input for the integral DC-DC converter. Decouple to GNDPWR with 220uF (10V) low impedance capacitor.
36	PD	**Power Down.** A logic 1 powers off the DC-DC converter. Connect to logic 0 for normal operation.
42, 43, 44, 45	GND_{PWR}	**DC-DC Ground.** Internal ground for the DC-DC converter.

*On Ag1460 these pins are used for internal connection, and must be left unconnected.

1.2 DIL Format Pin Out

Pin #	Name	Description
1, 28, 29, 56	RM	**Ringing Mode.** Sets bias conditions during ringing. Must be set to logic 1 during ringing. Must be set to logic 0 within 500ms of Ring Trip detect and during normal Off Hook condition.
2, 27, 30, 55	V_{OUT}	**Audio Out.** This is the analog output signal (from Tip and Ring) to the Codec. Must be ac coupled with typically 100nF.
3, 26, 31, 54	ZB*	**Balance Impedance.** Connect programming components between ZB and V_{IN} on Ag1460P only.*
4, 25, 32, 53	$+5V_A$	**Analog Supply.** Each pin must be connected to $+5V_{PWR}$ with 10Ω resistors. Decouple each with 100uF (16V) capacitors.
5, 24, 33, 52	SHK	**Switch Hook.** Indicates Off-Hook when at logic 1. Must be de-bounced
6, 23, 34, 51	ZT_1*	**Terminal Impedance 1.** Connect programming components between ZT_1 and ZT_2 on Ag1460P only.*
7, 22, 35, 50	ZT_2*	**Terminal Impedance 2.** Connect programming components between ZT_1 and ZT_2 on Ag1460P only.*
8, 21, 36, 49	V_{IN}	**Audio In.** This is the analog input signal from the Codec (which is output on Tip and Ring). Must be ac coupled with typically 100nF.
9, 20, 37, 48	F/R	**Forward/Reverse.** A logic 0 will reverse the Tip and Ring voltage polarities. F/R is toggled to produce the ringing output.
10, 19, 38, 47	CAP	**Slew Rate Capacitor.** A capacitor is fitted between this pin and GND to control the battery reversal and the ringing slew rate. 220nF is recommended.
11, 18, 39, 46	LO	**Loop Off.** A logic 1 removes the loop current from the line. Connect to logic 0 for normal operation.
12, 17, 40, 45	TIP (A)	**Tip.** Connects to the subscriber line Tip.
13, 16, 41, 44	RING (B)	**Ring.** Connects to the subscriber line Ring.
14	$+5V_{PWR}$	**DC-DC Supply.** +5V input for the integral DC-DC converter. Decouple to GNDPWR with 220uF (10V) low impedance capacitor.
15	GND_{PWR}	**DC-DC Ground.** Internal ground for the DC-DC converter.
42	PD	**Power Down.** A logic 1 powers off the DC-DC converter. Connect to logic 0 for normal operation.
43	GND_A	**Analog Ground.** Normally connected to system ground.

*On Ag1460 these pins are used for internal connection, and must be left unconnected.

1.0 Line Interfacing

As well as being in an electrically demanding environment, the needs of different applications and regulatory standards means that the SLIC must allow flexibility, together with facilities to ensure robust performance. All four of the SLICs on the Ag1460 provide a complete and flexible interface to the telephone line.

1.1 Battery Feed

The Ag1460 has an integral DC-DC converter which generates the battery voltages in the device. This means that only a supply of +5V, and GND is needed, unlike conventional SLICs which will need a battery voltage of anything between -20V and -60V (-75V for ringing). This confers a significant cost, space and time to market benefit on the equipment designer.

The battery feed to the telephone line is generated from the positive supply rail. This provides a -48V battery feed to the line, except during ringing, when this is increased to -72V. The loop current is pre-set to a constant 24mA. If the loop length is such that the constant current feed cannot be maintained (i.e. >3km), then the Ag1460 will revert to a constant voltage source, allowing the loop to be serviced at a reduced loop current.

1.2 Ringing

The ringing signal is generated by switching the appropriate SLIC into ringing mode by setting the RM pin high and then toggling the F/R pin at the required frequency and cadence. The toggling of the F/R pin produces a balanced signal at Tip and Ring. These signal waveforms are shown in figure 3.
During ringing the DC-DC converter automatically

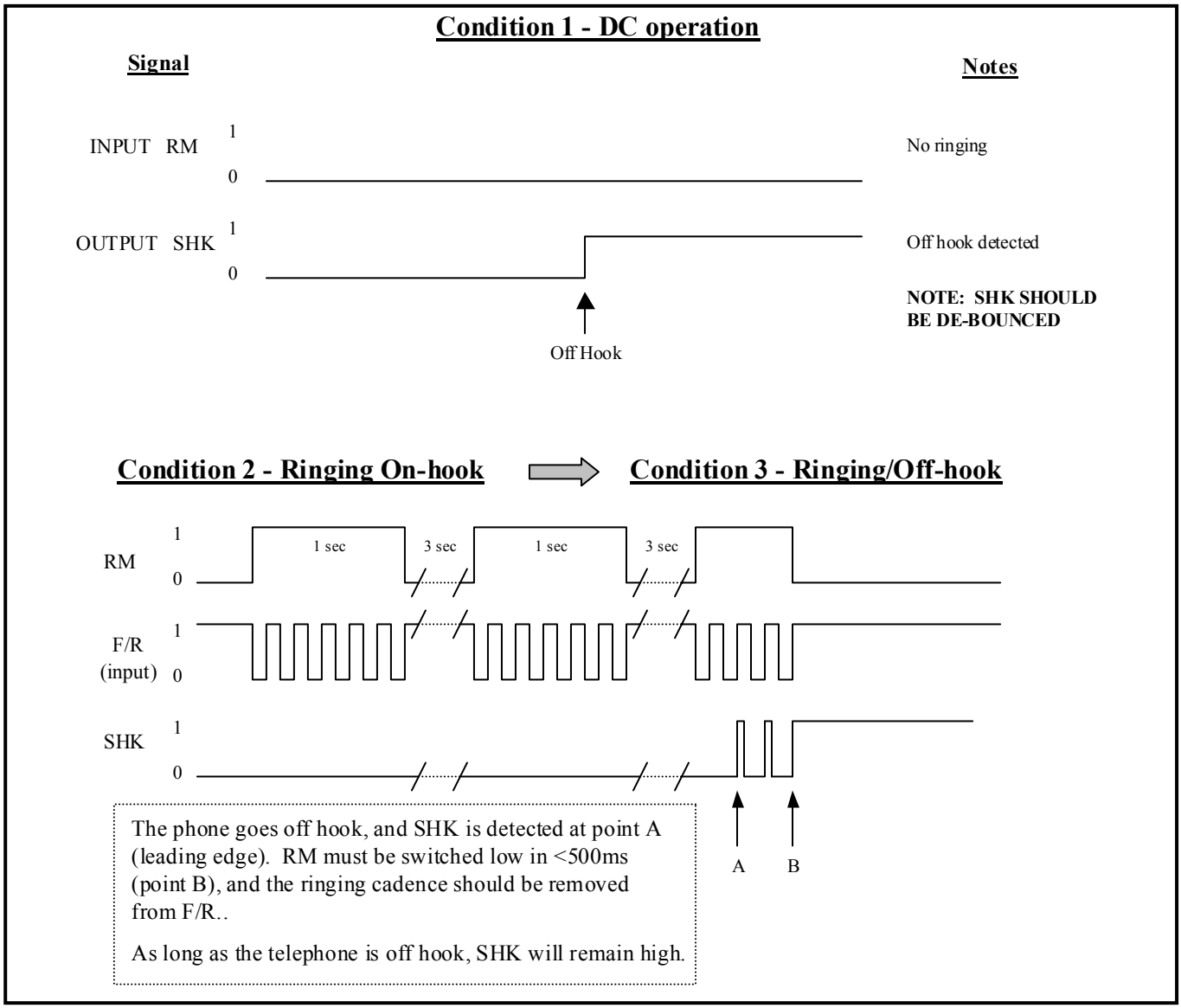


Figure 3: Ringing Signal Waveforms

switches to produce a battery voltage of -72V. This will produce greater than 40V_{RMS} into a REN of 3. The slope of the edges on the ringing waveform is determined by the value of the slew rate capacitor connected between the CAP pin and Ground. A 220nF capacitor is recommended with 20Hz ringing.

When the "off-hook" condition occurs during ringing, the ring-trip circuit on the Ag1460 senses the loop current flowing and signals the off-hook condition on the SHK output (as shown in figure 3). The SHK signal must be "debounced" to remove any spurious pulses by the controlling processor. On detection of SHK the ringing signal must be removed from the F/R pin and RM taken to a logic 0 within 500ms to avoid excessive power dissipation in the line driver circuit. The ring-trip function will operate up to a maximum loop resistance of 800Ω (including telephone), which corresponds to around 3km loop length.

To keep within the power rating of the on-board DC-DC converter, it is important that only one SLIC channel is ringing at any time. This can be met by using a ringing cadence of 1 second ON, 3 seconds OFF. The active ringing channel is then sequenced so that all four SLIC channels may be in the ringing mode, but only one is supplying ringing current at any one time.

1.3 Loop Off and Power Down

The loop current can be removed from the line by switching the LO input to a logic 1. This can be used as a power denial to the line or to present a very high impedance to the line. Typically used when carrying out maintenance on the line, or to suspend service during a line fault, etc.

The DC-DC converter can be switched off by applying a logic 1 to the PD input. This reduces the current consumption to a nominal 10mA. The SLIC takes 50ms to power up from this powered down state. When using the power down state it is recommended that the SLIC is polled (powered up periodically) to check for SHK (the subscriber has gone off hook).

Since the DC-DC converter supplies the power to all four SLICs on the Ag1460, all four SLICs will be powered down when the PD signal is applied.

2.0 The 2-4 Wire (hybrid) Conversion.

Each individual SLIC of the Ag1460 transmits and receives balanced 2-wire analog signals at the Tip and Ring connections. These are converted to a ground referenced output at V_{OUT} and from a ground referenced input at V_{IN}.

V_{OUT} and V_{IN} are normally connected to a Codec for conversion to and from a digital Pulse Code Modulated (PCM) stream.

2.1 The 2 Wire Impedance.

For the Ag1460, the input impedance, Zin, of each SLIC is set to 600Ω. For countries where the line impedance is 600Ω e.g. North America, no external adjustment is required. For countries where an alternative line impedance is used the Codec filter characteristics can be programmed to give the required matching.

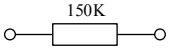
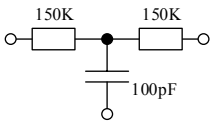
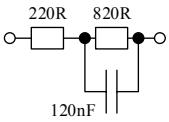
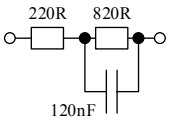
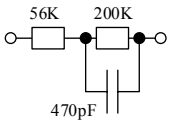
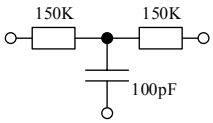
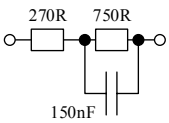
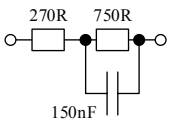
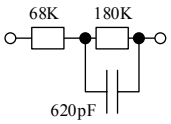
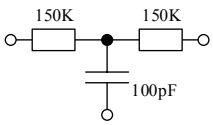
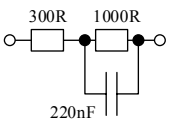
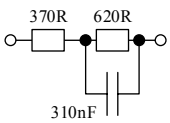
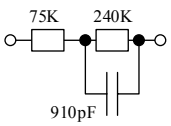
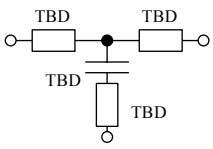
Country	Termination Impedance	Balance Impedance	Z_T	Z_B
USA	600R	600R		
Germany Spain South Africa				
Europe CTR21				
UK				

Table 1: Impedance Programming for Ag1460P

The Codec manufacturer can provide information on how Codec programming is done. Programmable Codecs require information about the transfer characteristics of the SLIC with which they are working, which is contained in a .CIR netlist. A .CIR netlist can be obtained by contacting either Silver Telecom or your local representative, to allow the Codec programming coefficients to be generated.

If a simple (non-programmable) Codec is being used, the Ag1460P provides programming of Zin through hardware. The input impedance, Zin, of the SLIC can be set to the required value by connecting the appropriate impedance across pins ZT_1 and ZT_2. The scaling factor is 250 so a resistor of value 150kohms will give an impedance of 600R tip to ring.

In this way the requirements of many countries may be met with one common linecard layout. Different values of the ZT components are only parts requiring change. Typical combinations are shown in table 1.

2.2 Network Balance Impedance.

The network balance impedance, Zb, of each SLIC is set to 600Ω for the standard Ag1460. For countries where the network balance impedance is 600Ω e.g. North America, no external adjustment is required. For countries where an alternative network balance impedance is used the Codec filter characteristics can be programmed to give the required matching. The .CIR netlist is again needed to allow the Codec programming coefficients to be generated.
If a simple Codec is being used the Ag1460P is available, providing programming of ZB through hardware. The network balance impedance, ZB, of the SLIC is set to the required value by connecting the appropriate impedance between pins V_{IN} and ZB. Where the input and balance impedances are the same, a resistor value of 300k should be used with a 100pF capacitor in a "T" configuration as shown in Table 1. Where the impedances are different, then no simple relationship exists.

Some typical examples are shown in Table 1. For countries which are not shown, please contact Silver Telecom.

2.3 Transmit and Receive Gain.

The gain in both the transmit direction (Tip/Ring to V_{OUT}) and the receive direction (V_{IN} to Tip/Ring) is set to 0dB. Normally any gain adjustments required by the user can be made by programming the Codec.

2.4 Tip & Ring Polarity Reversal.

The Ag1460 can reverse the battery voltage polarity at Tip and Ring via the F/R pin.

If F/R is held at logic 1 (forward) the d.c. voltage at Tip is positive with respect to Ring. If F/R is taken to logic 0 the voltage polarity is reversed. The F/R pin should not be left floating, and if not used should be tied high.

2.5 On Hook Transmission.

The Ag1460 is capable of on-hook transmission. This means analog signals can be transmitted from V_{in} through Tip and Ring and onto the line even when no loop current is flowing. This can be used when sending Caller Line Identification (CLI) information or for other "no ring" calls.

The Ag1460 will provide on hook transmission with a high impedance on Tip/Ring or where specific loads are demanded by Network Operators.

3.0 Switch Hook Detect Level

When the subscriber goes "off-hook" loop current will begin to flow. If this current is above the detection threshold (10mA) the switch hook output, SHK, will switch to logic 1. It is recommended that software or hardware de-bouncing of the switch hook signal is used. This is to avoid short pulses due to contact bounce, which can cause a false switch hook output, triggering the incorrect system response.

During loop disconnect dialling; SHK will pulse between logic 1 and logic 0 to indicate the digits being dialled. Again it is recommended that software de-bouncing is used to avoid false detection of digits.

4.0 Protection of the Ag1460 SLIC

4.1 Thermal Protection

Should any SLIC be operated incorrectly, for example by accidentally shorting Tip and Ring to each other or to ground, there is a danger the power dissipation could exceed the maximum rating. In this case a thermal cut-off will ensure the device gradually powers down safely by reducing the loop current. Once the problem has been corrected the loop current will return to its normal level.

This feature means that the SLIC can be used even when a thermal overload has occurred.

4.2 Lightning and Power Cross Protection.

It is usual for the Ag1460 to be used in "on-premise" applications, such as SOHO, CTI and VoIP. In this case power cross and lightning protection is not required, however in most 'off-premise' applications, a subscriber circuit will be required to withstand over voltage conditions which could be caused by lightning or overhead power cables striking the telephone cables. It is therefore normal in "off-premise"

applications to provide primary and secondary protection circuits to prevent damage to the SLIC.

The Ag1460 has been designed to be able to use low cost protection components and a typical circuit is shown in Figure 4. This circuit is suitable for most "on-premise" applications.

With some additional components, the Ag1460 will meet UL60950 requirements: a series element should be added - a combination of a fuse (e.g. 350mA, Bussman C515 or Littelfuse 220003) and a surge resistor (25Ω typically). Alternatively a Teccor F1250T or F0500T fuse may be used without a surge resistor.

For ITU-T K20 power cross protection, a PTC thermistor (eg. type JH330L) of 30R is suitable. The lightning protection is provided by steering diodes connected to 0V and upgrading D1 to a Tranzorb device (Motorola or Semitron 1.5KE82A). For lightning and power cross protection, D1 should be upgraded further (5KP75). Just one Tranzorb is needed per linecard.

5.0 Approvals.

It can be seen from the Electrical Characteristics given on subsequent pages that the SLIC has been designed to meet the equipment standards of as many major public telephone authorities as possible.

It is the responsibility of the equipment designer to ensure that their system meets the requirements of the relevant regulatory bodies. Every effort is made to ensure that Silver Telecom products are compliant with the latest standards.

6.0 A Typical Application.

The Ag1460 has been designed to interface to any Codec, and is shown in a typical application in figure 4. For examples of the interface to various codecs, either visit the Silver Telecom web-site at www.silvertel.com, or contact Silver Telecom or their local representative.

The status outputs from the SLIC are passed to the micro-controller. These signals can then be processed as necessary by the system software. Control over the ringing and reversals functions is achieved via the RM and F/R pins.

The audio signals which are on the 4 wire side of the connection are coupled by 100nF capacitors to avoid d.c. level problems between the two devices.

The Ag1460 provides for a 2 wire impedance and a network balance impedance of 600Ω. For other impedances a DSP codec can be used which can be programmed using applications information available from the codec manufacturer. The necessary transfer function parameters for the Ag1460 are available from Silver Telecom.

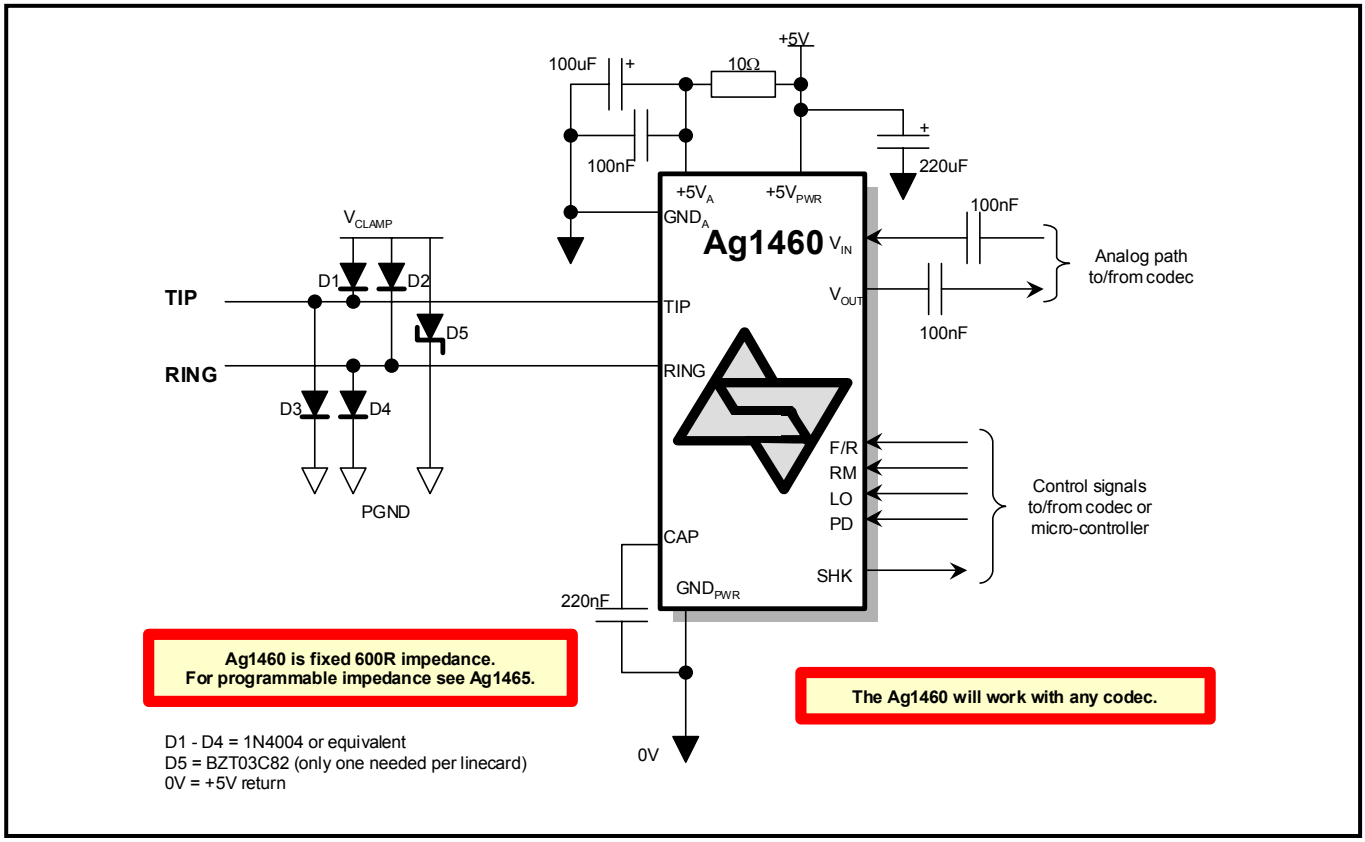


Figure 4: Typical On-Premise Application
(only one channel shown for clarity)

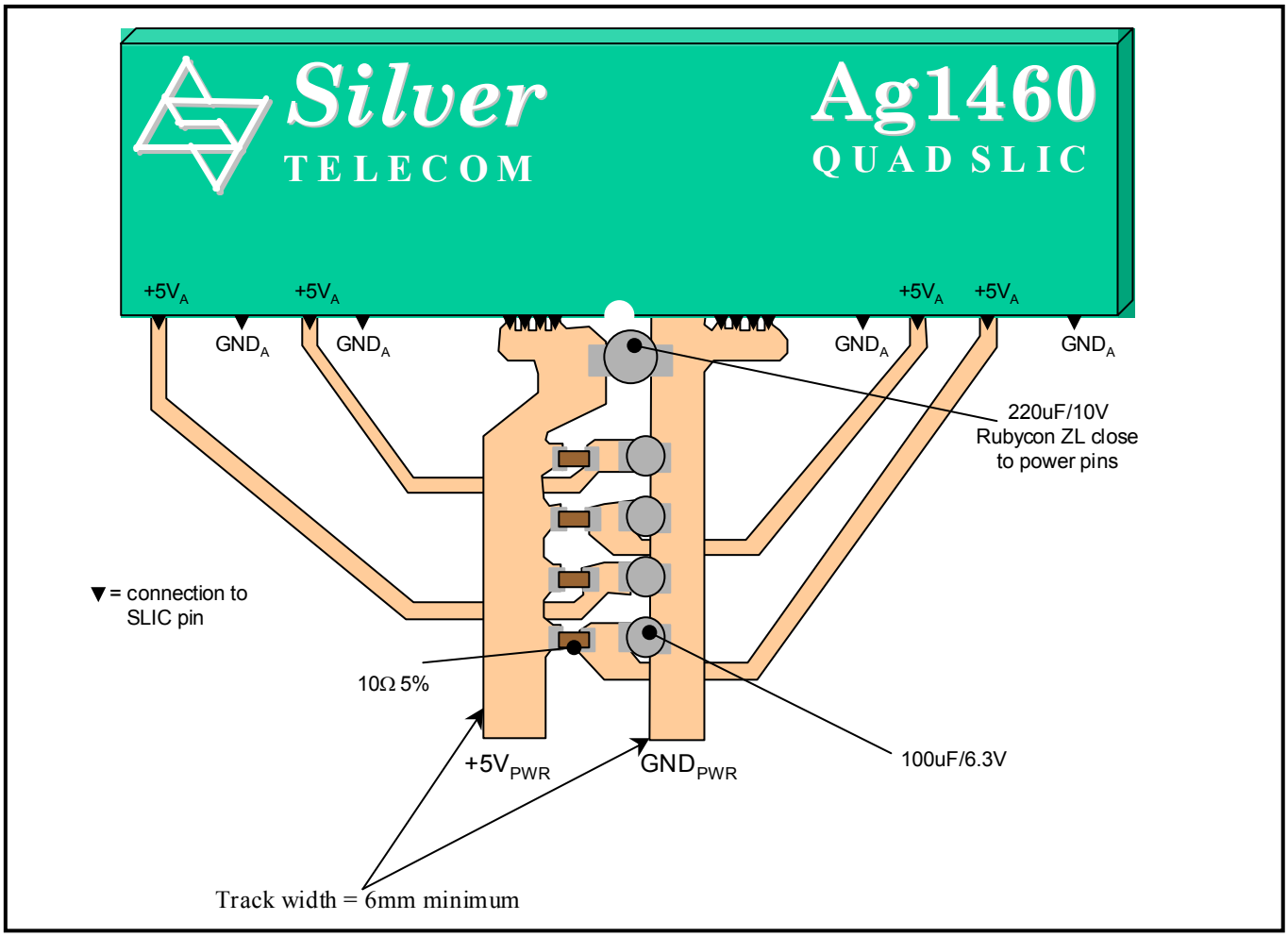


Figure 5: Layout Considerations.

If a simple Codec, without programmable filtering characteristics, is to be used, then the Ag1460P can provide user hardware programmable line and network balance impedances. Contact Silver Telecom for other applications circuits.

7.0 Layout Considerations.

Figure 5 gives an example of the tracking needed for the Ag1460. Tracks to the $+5V_{PWR}$ and GND_{PWR} should be made as thick as possible. Also to maximise the performance of the device signal tracks should be kept as short as possible. Finally, as is common in all designs, decoupling capacitors should be placed adjacent to the supply and ground pins.

8.0 Electrical Characteristics.

Absolute Maximum Ratings*

All Voltages are with respect to ground unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V_{CC}	-0.3	5.5	V
2	Maximum Power Dissipation per SLIC, Off Hook @ 25°C	P_{SLIC}		1.3	W
3	Storage Temperature	T_S	-40	+85	°C

*Exceeding the above ratings may cause permanent damage to the product. Functional operation under these conditions is not implied. Maximum ratings assume free air flow.

Recommended Operating Conditions*

All Voltages are with respect to ground unless otherwise stated.

	Parameter	Symbol	Min	Typ	Max	Units
1	DC Supply Voltage	V_{CC}	4.75	5.0	5.25	V
2	Operating Temperature	T_{OP}	0	25	70	°C

*Typical figures are at 25°C with nominal +5V supplies and are for design use only.

DC Electrical Characteristics.

	Characteristic	Sym	Min	Typ*	Max	Units	Test Comments
1	Supply Current (per SLIC), on- hook[1]	I_{VPWR}		200		mA	
2	Maximum DC-DC converter current consumption (3 channels off hook, 1 channel ring trip)	I_{DC}		1500		mA	
3	DC-DC converter current consumption (all channels idle)	P_{DC}		250		mA	
4	Current consumption while powered down	I_{PD}		55	75	mA	
5	Wake-up time			50		ms	
6	Constant current feed to line	I_{LOOP}	21.5	24	26.5	mA	R_{LOOP} = 500Ω
7	Tip/Gnd or Ring/Gnd or Tip&Ring/Gnd overcurrent				35.0	mA	
9	Off-Hook detect Output Low Voltage Output High Voltage	 V_{OL} V_{OH}	 3.15		 0.9	 V V	 @ 0.4mA @ -0.4mA
10	Off-Hook Detect Output Low Voltage Output High Voltage	 V_{OL} V_{OH}	 3.5		 0.4	 V V	 @ 50uA @ -50uA
11	Control Inputs, F/R, LO, PD Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	 4.0		 0.3	 V V	
12	Control Inputs, F/R, LO, PD Input low current Input high current	 I_{IL} I_{IH}	 -0.5		 0.5	 mA mA	
13	Switch Hook Detect Threshold			10.0		mA	
14	Load on V_{out}		10.0			kohm	100nF coupling

1) All DC Electrical Characteristics are over the Recommended Operating Conditions with V_{CC} at +5.0V ±5%, unless otherwise stated.

2) Operating currents are dependant on the users application.

*Typical figures are at 25°C with nominal 5V supply and are for design aid only.

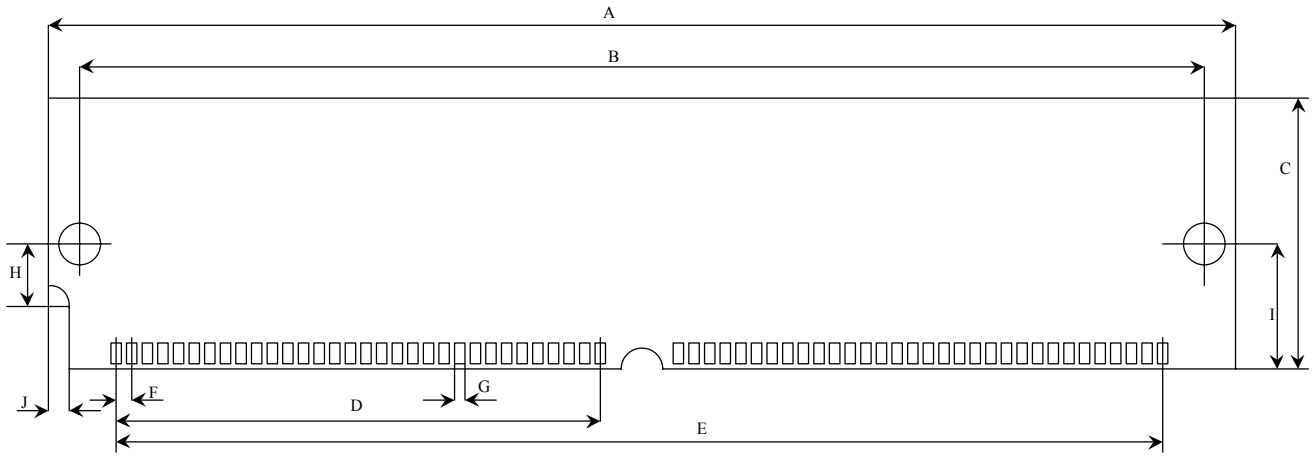
AC Electrical Characteristics.

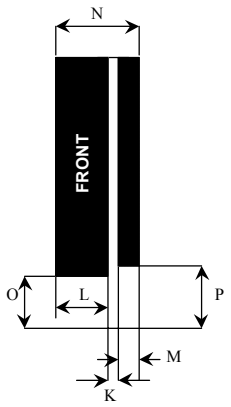
	Characteristic	Sym	Min	Typ*	Max	Units	Test Comments
1	SHK Detect Time			5.0		ms	No Ringing
2	Ring Trip Capability			3.0		km	24 AWG line
3	Input Impedance at V_{in}			150		kohm	
4	Output impedance at V_{out}				10	ohm	
5	Ringing Capability $40V_{rms}$ into REN=3 $40V_{rms}$ into REN=1	D_{RING}			 2.8 3.0	 km km	
6	Absolute Voltage Gain, 2 Wire to V_{out}		-0.5	0	0.5	dB	Off-Hook
7	Absolute Voltage Gain V_{in} to 2Wire		-0.5	0	0.5	dB	Off-Hook
8	Relative Gain, Referenced to 1kHz. 2Wire - V_{out}, V_{in} - 2Wire		-0.25		0.25	dB	Over frequency range 200 to 3400 Hz
9	Total Harmonic Distortion @ 2Wire and V_{out}	THD		0.1	1.0	%	@0dBm, 1kHz
10	Overload Distortion @2 Wire and V_{out}	OD		0.5	5.0	%	@+3dBm, 1kHz
11	Common Mode Rejection Ratio @ 2 Wire	CMRR	40	46		dB	200-3400Hz
12	Idle Channel Noise	N_C		8.0	12.0	dBrnC	@2 Wire & V_{OUT}
13	Power Supply Rejection Ratio at 2 Wire and V_{out}	PSRR	25	32		dB	Ripple 0.1V, 1kHz on V_{CC}
14	Return Loss	RL	18	35		dB	200-3400Hz
15	Transhybrid Loss	THL	18 21	35 35		dB dB	200-3400Hz 500-2500Hz
16	Longitudinal to Metallic Balance		46	53		dB	200-3400Hz
17	Tip-Ring Reversal Settling Time				50	ms	To within +20% of set I_{LOOP}
18	Crosstalk			-70			1kHz, 0dBm

3) All AC Electrical Characteristics are over the Recommended Operating Conditions with V_{CC} at +5.0V $\pm$5%, unless otherwise stated.
4) Gain, Transhybrid Loss and Total Harmonic distortion parameters measured with 600Ω termination.
*Typical figures are at 25°C with nominal 5V supply and are for design aid only.

9.0 Mechanical Specification

9.1 SIMM Package





Dimension	Millimetres (Inches)
A	**107.7 (4.240)**
B	**101.19 (3.984)**
C	**36.00 (1.417)**
D	**44.50 (1.750)**
E	**95.25 (3.750)**
F	**1.27 (0.050)**
G	**1.04 (0.041)**
H	**5.84 (0.230)**
I	**10.16 (0.400)**
J	**2.00 (0.079)**
K	**1.27 (0.050)**
L	**5.50 (0.217)**
M	**2.30 (0.091)**
N	**9.07 (0.357)**
O	**3.40 (0.134)**
P	**4.70 (0.185)**

9.2 DIL Package