

Document Title

256K x16 bit 2.3 ~ 2.7V Super Low Power FCMOS Slow SRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Initial Draft	Dec.20.2000	Preliminary
01	Changed Logo	Mar.23.2001	Preliminary
02	Changed lsb1 values Changed part No Q -> L	Jun.07.2001	Preliminary
03	Changed Package Size (6.1mm -> 6.0mm)	Aug.07.2001	Preliminary

Preliminary

DESCRIPTION

The HY62LF16404D is a high speed, super low power and 4Mbit full CMOS SRAM organized as 256K words by 16bits. The HY62LF16404D uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

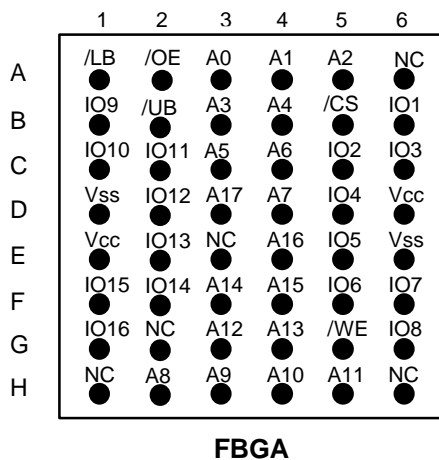
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup
 - 1.5V(min) data retention
- Standard pin configuration
 - 48-ball FBGA

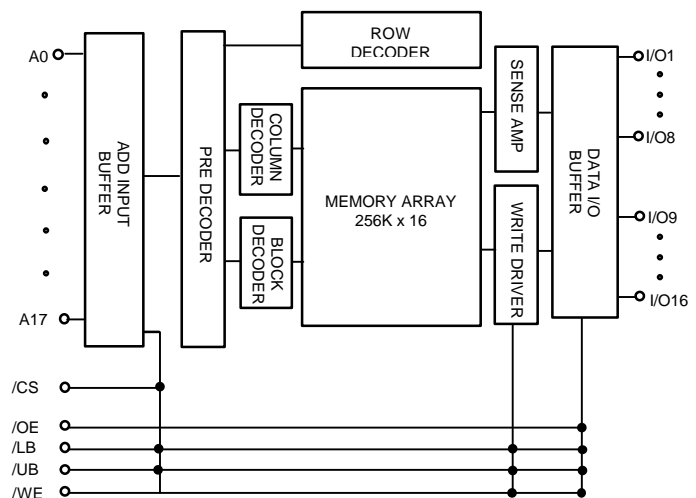
Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)		Temperature (°C)
				LL	SL	
HY62LF16404D-I	2.3~2.7	70/85	3	10	5	-40~85

Note 1. Blank : Commercial, I : Industrial
 2. Current value is max.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	I/O1~I/O16	Data Inputs/Outputs
/WE	Write Enable	A0~A17	Address Inputs
/OE	Output Enable	Vcc	Power (2.3~2.7)
/LB	Lower Byte Control (I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control (I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY62LF16404D-DF(I)	70/85	LL-part	I	FBGA
HY62LF16404D-SF(I)	70/85	SL-part	I	FBGA

Note 1. Blank : Commercial, I : Industrial

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit	Remark
V _{IN} , V _{OUT}	Input/Output Voltage	-0.3 to 3.0	V	
V _{CC}	Power Supply	-0.3 to 4.0	V	
T _A	Operating Temperature	40 to 85	°C	HY62LF16404D-I
T _{STG}	Storage Temperature	-55 to 150	°C	
P _D	Power Dissipation	1.0	W	
T _{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O Pin		Power
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	X	X	H	H				
L	H	H	L	X	Output Disabled	High-Z	High-Z	Active
			X	L				
L	H	L	L	H	Read	DOUT	High-Z	Active
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Active
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

Note:

- H=V_{IH}, L=V_{IL}, X=don't care (V_{IL} or V_{IH})
- /UB, /LB(Upper, Lower Byte enable)
 These active LOW inputs allow individual bytes to be written or read.
 When /LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.
 When /UB is LOW, data is written or read to the upper byte, I/O 9 -I/O 16.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ	Max.	Unit
Vcc	Supply Voltage	2.3	2.5	2.7	V
Vss	Ground	0	0	0	V
VIH	Input High Voltage	2.0	-	Vcc+0.3	V
VIL	Input Low Voltage	-0.3 ¹	-	0.6	V

Note : 1. Undershoot : VIL = -1.5V for pulse width less than 30ns
 2. Undershoot is sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to 85°C

Sym	Parameter	Test Condition	Min	Typ ¹	Max	Unit
ILI	Input Leakage Current	Vss ≤ VIN ≤ Vcc	-1	-	1	uA
ILO	Output Leakage Current	Vss ≤ VOUT ≤ Vcc, /CS = VIH or /OE = VIH or /WE = VIL or /UB = VIH, /LB = VIH	-1	-	1	uA
Icc	Operating Power Supply Current	/CS = VIL, VIN = VIH or VIL, Ii/O = 0mA			3	mA
ICC1	Average Operating Current	/CS = VIL, VIN = VIH or VIL, Cycle Time = Min, 100% Duty, Ii/O = 0mA			25	mA
		/CS ≤ 0.2V, VIN ≤ 0.2V or VIN ≥ Vcc-0.2V, Cycle Time = 1us, 100% Duty, Ii/O = 0mA			3	mA
ISB	Standby Current (TTL Input)	/CS = VIH or /UB, /LB = VIH VIN = VIH or VIL			0.3	mA
ISB1	Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V or /UB, /LB ≥ Vcc - 0.2V VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	SL	0.2	5	uA
			LL	0.2	10	uA
VOL	Output Low	IOL = 0.5mA	-	-	0.4	V
VOH	Output High	IOH = -0.5mA	2.0	-	-	V

Note

1. Typical values are at Vcc = 2.5V TA = 25°C
2. Typical values are not 100% tested

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance(Add, /CS,/LB,/UB, /WE, /OE)	VIN = 0V	8	pF
COU	Output Capacitance(I/O)	VIO = 0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

T_A = -40°C to 85°C, unless otherwise specified

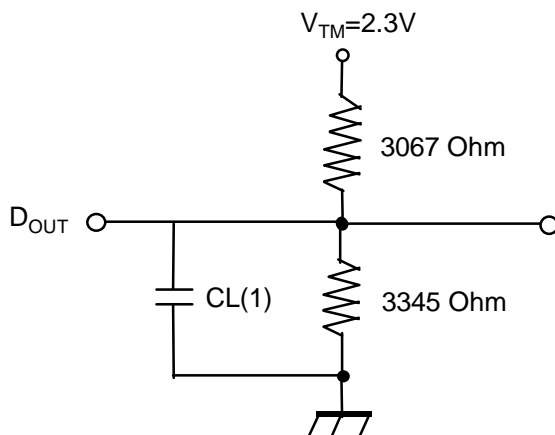
#	Symbol	Parameter	70ns		85ns		Unit
			Min.	Max.	Min.	Max.	
READ CYCLE							
1	t _{RC}	Read Cycle Time	70	-	85	-	ns
2	t _{AA}	Address Access Time	-	70	-	85	ns
3	t _{ACS}	Chip Select Access Time	-	70	-	85	ns
4	t _{OE}	Output Enable to Output Valid	-	35	-	40	ns
5	t _{BA}	/LB, /UB Access Time	-	70	-	85	ns
6	t _{CLZ}	Chip Select to Output in Low Z	10	-	10	-	ns
7	t _{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
8	t _{BLZ}	/LB, /UB Enable to Output in Low Z	10	-	10	-	ns
9	t _{CHZ}	Chip Deselection to Output in High Z	0	30	0	30	ns
10	t _{OHZ}	Out Disable to Output in High Z	0	30	0	30	ns
11	t _{BHZ}	/LB, /UB Disable to Output in High Z	0	30	0	30	ns
12	t _{OH}	Output Hold from Address Change	10	-	10	-	ns
WRITE CYCLE							
13	t _{WC}	Write Cycle Time	70	-	85	-	ns
14	t _{CW}	Chip Selection to End of Write	60	-	70	-	ns
15	t _{AW}	Address Valid to End of Write	60	-	70	-	ns
16	t _{BW}	/LB, /UB Valid to End of Write	60	-	70	-	ns
17	t _{AS}	Address Set-up Time	0	-	0	-	ns
18	t _{WP}	Write Pulse Width	50	-	60	-	ns
19	t _{WR}	Write Recovery Time	0	-	0	-	ns
20	t _{WHZ}	Write to Output in High Z	0	20	0	25	ns
21	t _{DW}	Data to Write Time Overlap	30	-	35	-	ns
22	t _{DH}	Data Hold from Write Time	0	-	0	-	ns
23	t _{OW}	Output Active from End of Write	5	-	5	-	ns

AC TEST CONDITIONS

T_A = -40°C to 85°C, unless otherwise specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.1V
Output Load	t _{CLZ} , t _{OLZ} , t _{BLZ} , t _{CHZ} , t _{OHZ} , t _{BHZ} , t _{WHZ} , t _{OW}
	Others
	CL = 5pF + 1TTL Load
	CL = 30pF + 1TTL Load

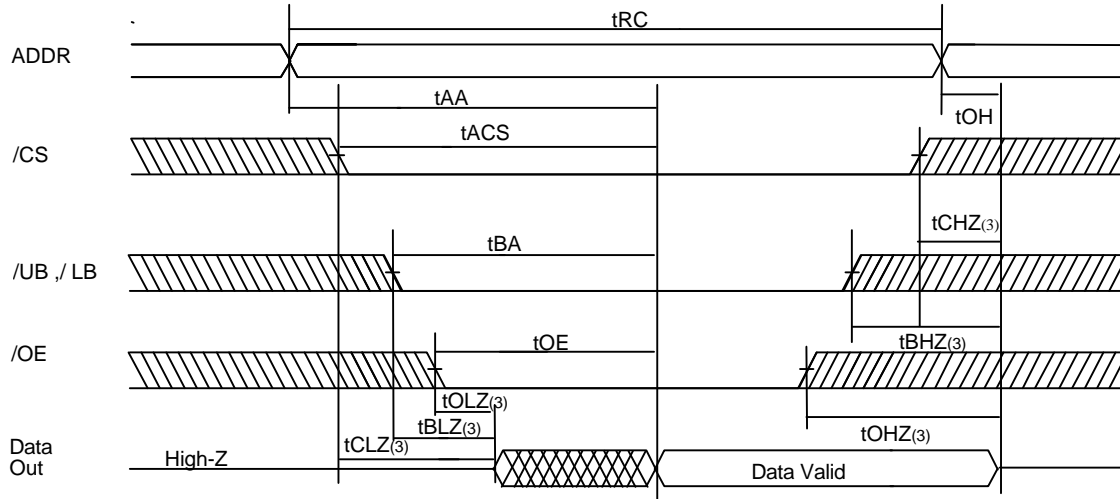
AC TEST LOADS



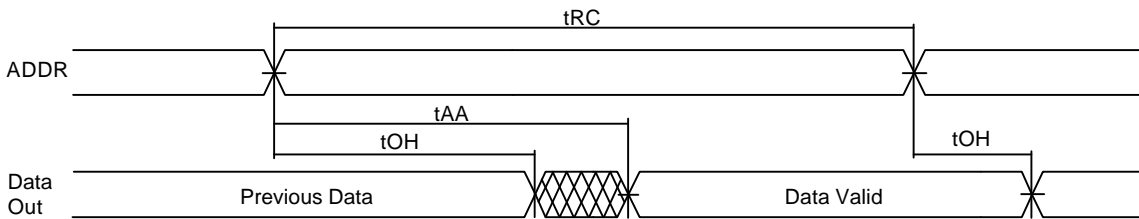
Note 1. Including jig and scope capacitance:

TIMING DIAGRAM

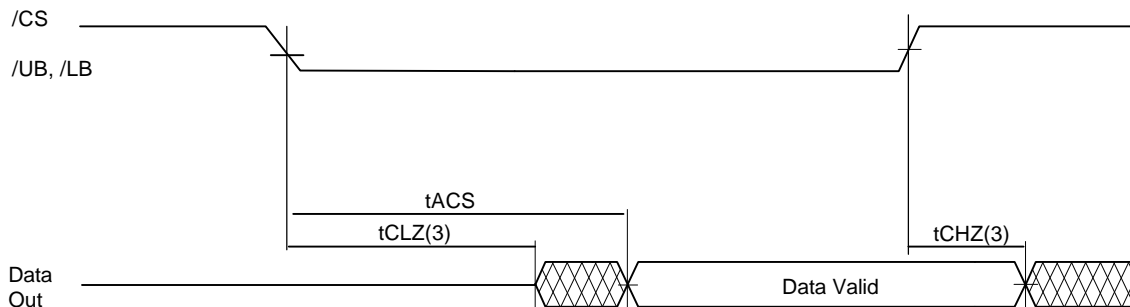
READ CYCLE 1 (Note 1,4)



READ CYCLE 2 (Note 1,2,4)



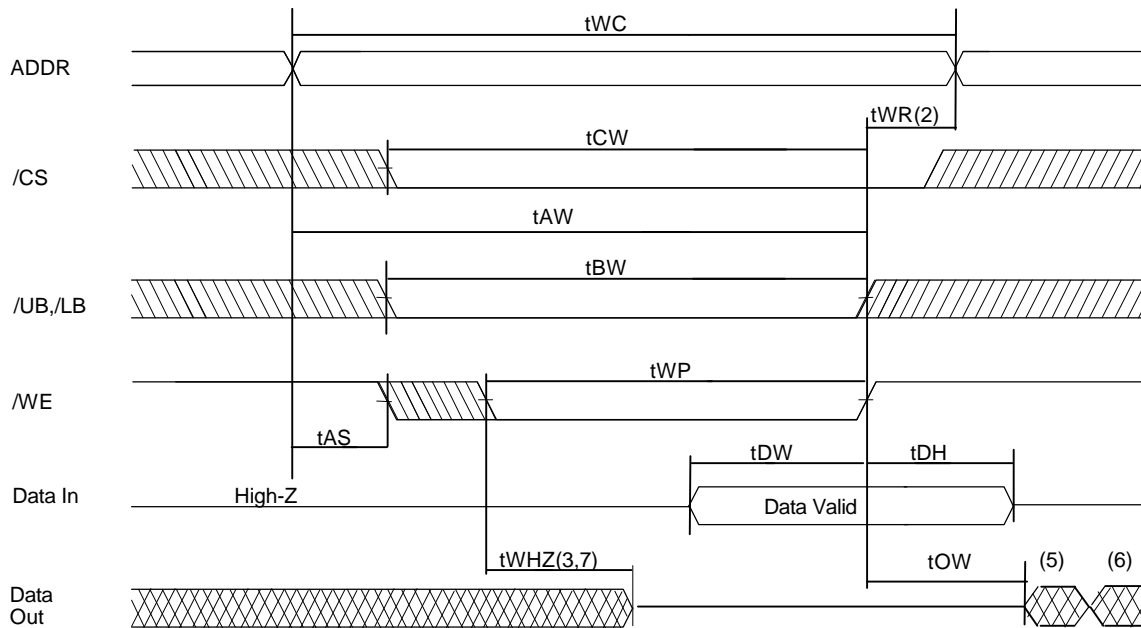
READ CYCLE 3 (Note 1,2,4)



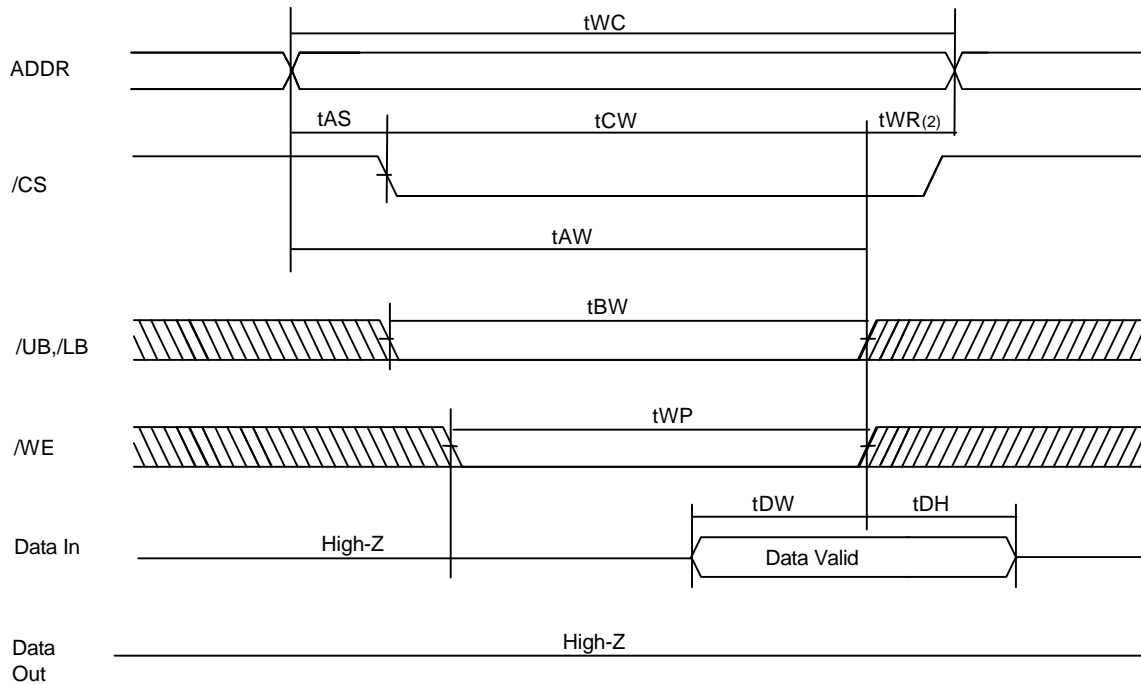
Notes:

1. A read occurs during the overlap of a low /OE, a high /WE, a low /CS and /UB and/or /LB .
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active
/UB and /LB in high for the standby, low for active

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,8) (/CS Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS and a low /UB and/or /LB .
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured $\pm 200\text{mV}$ from steady state.
This parameter is sampled and not 100% tested.
8. /CS in high for the standby, low for active
/UB and /LB in high for the standby, low for active

DATA RETENTION ELECTRIC CHARACTERISTIC

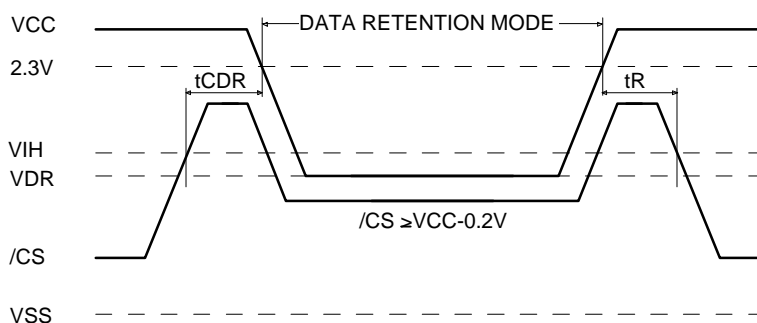
TA = -40°C to 85°C

Symbol	Parameter	Test Condition	Min	Typ ¹	Max	Unit	
VDR	Vcc for Data Retention	/CS \geq Vcc - 0.2V or /UB, /LB \geq Vcc - 0.2V, VIN \geq Vcc - 0.2V or VIN \leq Vss + 0.2V	1.5	-	2.7	V	
Iccdr	Data Retention Current	Vcc=1.5V, /CS \geq Vcc - 0.2V or /UB, /LB \geq Vcc - 0.2V VIN \geq Vcc - 0.2V or VIN \leq Vss + 0.2V	SL	-	0.2	6	μA
			LL	-	0.2	12	μA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns	
tR	Operating Recovery Time		tRC	-	-	ns	

Notes:

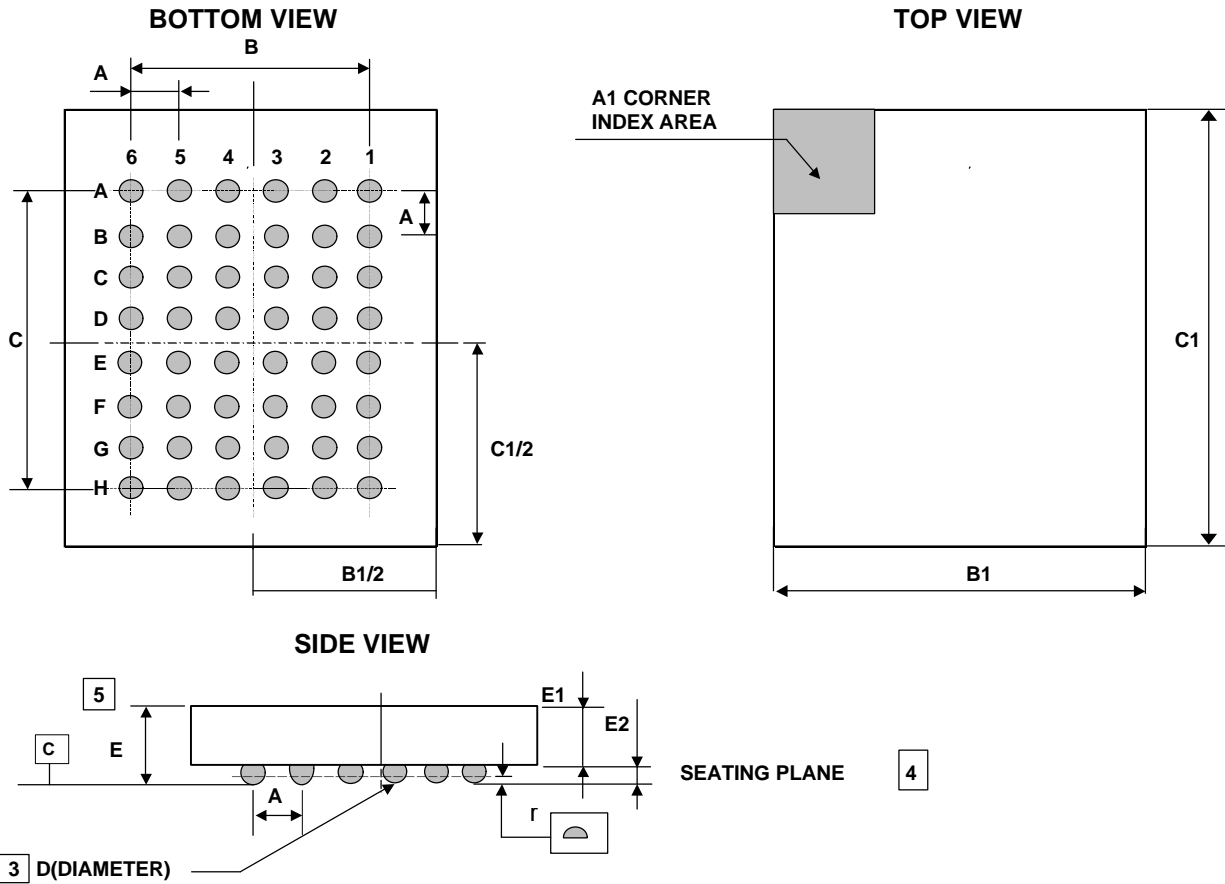
1. Typical values are under the condition of TA = 25°C.
2. Typical Value are sampled and not 100% tested

DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

48ball Fine Pitch Ball Grid Array Package (F)



Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1	5.9	6.0	6.1
C	-	5.25	-
C1	7.9	8.0	8.1
D	0.3	0.35	0.4
E	0.9	1.0	1.10
E1	-	0.75	-
E2	0.20	0.25	0.30
r	-	-	0.08

Note

1. DIMENSIONING AND TOLERANCING PER ASME Y14. 5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION "D" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

MARKING INFORMATION

Package	Marking Example
FBGA	

Index

• HYQF6404D	: Part Name
• c	: Power Consumption - D : Low Low Power - S : Super Low Power
• ss	: Speed - 70 : 70ns - 85 : 85ns
• t	: Temperature - I : Industrial (-40 ~ 85 °C)
• y	: Year (ex : 0 = year 2000, 1= year 2001)
• ww	: Work Week (ex : 12 = work week 12)
• p	: Process Code
• xxxxx	: Lot No.
• KOR	: Origin Country
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item