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Connecting **everything**®

BCM1255
PRODUCT Brief

DUAL-CORE 64-BIT MIPS® PROCESSOR (NEW!)

FEATURES

- **Two 64-bit MIPS® CPUs, scalable from 800 MHz–1.2 GHz**
  - Quad issue in-order pipeline with dual-execute and dual-memory pipes
  - Enhanced skew pipeline enables a zero load-to-use penalty
  - 32-KB instruction cache and 32-KB data cache (ECC protected)

- **Fast on-chip multiprocessor bus**
  - Connects the CPUs, L2 cache, memory controller, and I/O bridges
  - Runs at half the CPU core frequency and is 256 bits wide

- **On-chip L2 cache**
  - 512 KB shared by two CPUs and I/O agents
  - Eight-way associative, ECC protected
  - Any way can be programmed as fast on-chip RAM

- **DDR memory controller**
  - Memory bandwidth as high as 100 Gbps
  - Configurable as 2x64-bit or 4x32-bit wide channels
  - Runs up to 400-MHz clock rate, 800-MHz data rate
  - Support for DDR1, DDR2, and FCRAM

- **Integrated network and system I/O**
  - Four Gigabit-Ethernet MACs configurable as packet FIFO interfaces
  - 64-bit PCI-X interface at 133 MHz
  - Generic I/O for direct connect to boot ROM, flash memory
  - Two SMBus serial configuration interfaces
  - PCMCIA control interface and up to 16 interrupts
  - Four UART interfaces

- **On-chip debug capability**
  - EJTAG
  - Bus trace unit (internal logic analyzer)

- **Support for leading operating systems, including VxWorks®, Linux®, QNX®, and NetBSD**

- **Evaluation board platform available with samples (includes tools, firmware, and software drivers)**

SUMMARY OF BENEFITS

- **Industry-leading performance**
  - 2.5 Dhrystone MIPS/MHz per CPU
  - 10 Million packets per second of L3 forwarding
  - 128 Gbps on-chip bus bandwidth, with 100 Gbps memory bandwidth and 31 Gbps 1/0 bandwidth

- **Low-power dissipation of 13W @ 1 GHz**

- **High functional integration, reducing overall system cost**

- **Programming ease and flexibility based on MIPS64™ instruction set architecture (ISA)**

- **Software compatible with BCM1250 and BCM112x**

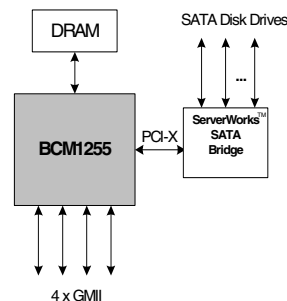- **Broad tools and system software support**

APPLICATIONS

- Because of its world-class performance, power efficiency, and integration, the **BCM1255** processor is ideal for a broad variety of applications, including:
  - Enterprise-class routers and switches
  - Multifunction security platforms (VPN/SSL/IDS)
  - Compact NAS platforms
  - SAN routers/gateways/switches
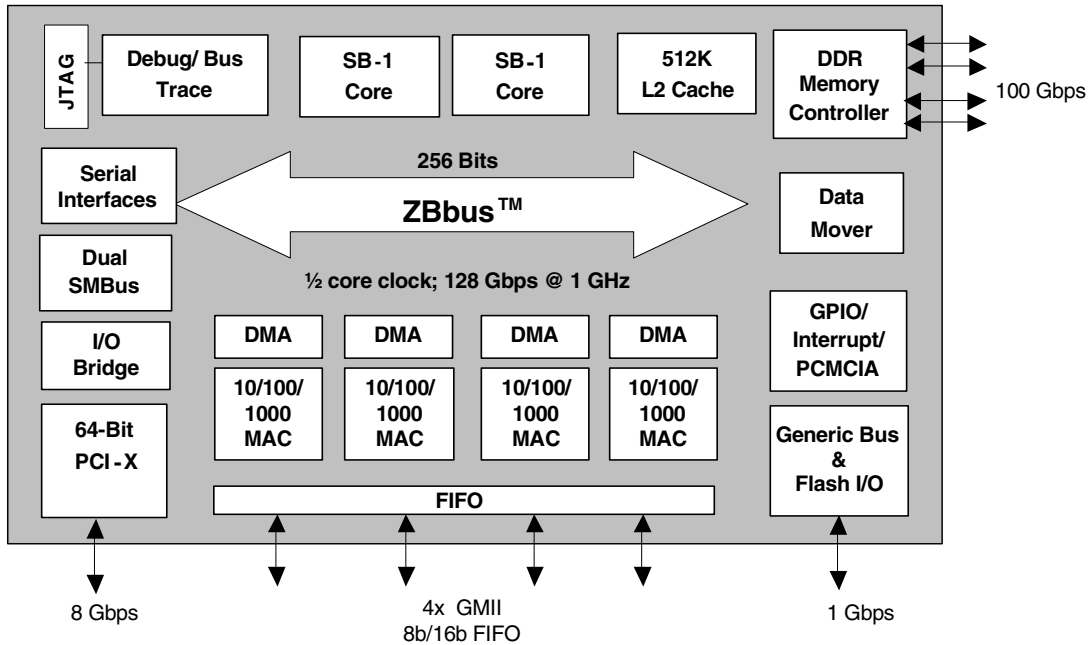 - Video servers and systems

VPN/Firewall Application — DRAM, BCM1255, GMII Control path, GMII Data path, GMII, FIFO, BCM5841, 2 Gbps Full-Duplex IPSec
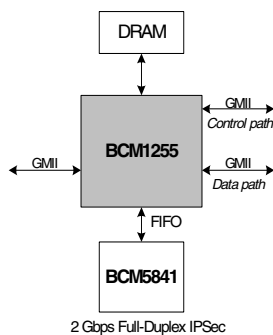
Storage System or Video Server — DRAM, BCM1255, PCI-X, ServerWorks™ SATA Bridge, SATA Disk Drives, 4 x GMII

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The **BCM1255** device is an MIPS64 processor core-based system-on-a-chip (SOC) that offers industry-leading performance, high functional integration, and low-power levels required by next-generation computing, storage, and networking applications.

The **BCM1255** is a chip multiprocessor (CMP) system consisting of two Broadcom SB-1 high-performance MIPS64 CPUs, a shared 512-KB L2 cache, a DDR memory controller, and integrated I/O. All major blocks of the processor are connected together via the ZBbus, a high-speed, split-transaction multiprocessor bus. The bus implements the standard MESI protocol to ensure coherency between the two CPUs, L2 cache, I/O agents, and memory. Four Gigabit-Ethernet MACs (10/100/1000) enable easy interfacing to LANs or control backplanes. To enable higher data rates (or in cases where Ethernet protocol processing is not required), the Gigabit-Ethernet MACs can be configured as 8-bit and/or 16-bit packet FIFOs. The **BCM1255** also integrates a 64-bit, 133-MHz PCI-X local bus for direct connection to I/O devices. Four serial ports are available for use as UARTs for console ports.

To enable low-chip count systems, the **BCM1255** also includes a configurable generic bus that allows glueless connection of a boot ROM or flash memory and simple I/O peripherals. On-chip debug, trace, and performance monitoring functions assist both hardware and software designers in debugging and tuning the system. The system can be run in either big-endian or little-endian mode.

Implementation of MIPS64 ISA

The SB-1 CPU core is a high-performance implementation of the standard MIPS64 ISA that incorporates the MIPS-3D and MIPS-MDMX application-specific extensions (ASEs). The core supports a 4-issue enhanced skew pipeline and can dispatch up to two memory and two ALU (integer, floating point, MDMX, or MIPS-3D) instructions per cycle.

Next Generation Broadband Processors

	BCM1255	BCM1280	BCM1455	BCM1480
# of CPUs	2	2	4	4
L2 Cache	512 KB	1 MB	1 MB	1 MB
DDR2 Support	Yes	Yes	Yes	Yes
# of MACs	4 GMII	4 GMII	4 GMII	4 GMII
PCI-X	1 x 64-bit	1 x 64-bit	1 x 64-bit	1 x 64-bit
# of SPI-4/HT Ports	0	3	0	3

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