FAIRCHILD SEMICONDUCTOR®

March 2006
Advance Information

# FHP3194
# 4:1 High Speed Multiplexer

## Features at ±5V

- 0.1dB gain flatness to 155MHz
- 7.5ns channel switching time
- 0.02%/0.03° differential gain/phase error
- 335MHz full power -3dB bandwidth at G=2
- 1600V/µs slew rate
- 60mA output current (easily drives three video loads)
- 70dB channel to channel isolation
- 13mA supply current
- 4mA supply current in disable mode
- 3mA supply current in shutdown mode
- Fully specified at ±5V supplies
- Lead (Pb) - free SOIC-14 and TSSOP-14 packages

## Applications

- Video switchers and routers
- Multiple Input HDTV switching
- Picture in picture video switch
- Multi-channel ADC Driver

## Description

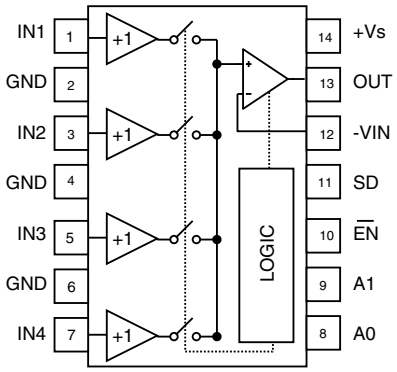
The FHP3194 is a 4:1 analog multiplexer designed for high speed video applications. The output amplifier is a high-speed current feedback amplifier that offers stellar large signal performance of 335MHz -3dB bandwidth and 80MHz 0.1dB bandwidth. The gain of the output amplifier is selectable thru 2 external resistors ($R_f$ and $R_g$), allowing further flexibility. The $2V_{pp}$ bandwidth performance, 1600V/µs slew rate, and 0.02% / 0.03° differential gain and phase exceed the requirements of high definition television (HDTV) and other multimedia applications. The output amplifier also provides ample output current to drive multiple video loads.

Two address bits (A0 and A1) are used to select one of the four buffered inputs. The FHP3194 offers excellent 7.5ns switching times and better than 70dB channel isolation.

The FHP3194 offers both shutdown and disable capability. During shutdown, the FHP3194 consumes only 3mA of supply current and provides maximum input to output isolation. During disable mode, only the output amplifier is disabled reducing output glitches and allowing for multiplexer expansion.

## Functional Block Diagram

FHP3194 SOIC / TSSOP



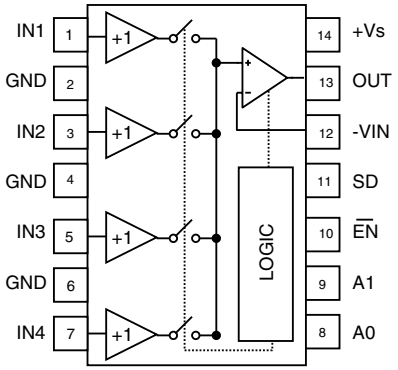

## Ordering Information

| Part Number | Package | Pb-Free | Operating Temperature Range | Packing Method |
|---|---|---|---|---|
| FHP3194IM14X | SOIC-14 | Yes | -40°C to +85°C | Reel |
| FHP3194IMTC14X | TSSOP-14 | Yes | -40°C to +85°C | Reel |

Moisture sensitivity level for all parts is MSL-1.

## Pin Configurations

FHP3194 SOIC / TSSOP




## Pin Assignments

| Pin# | Pin | Description |
|---|---|---|
| 1 | IN1 | Input, Channel 1 |
| 2 | GND | Must be connected to ground |
| 3 | IN2 | Input, Channel 2 |
| 4 | GND | Must be connected to ground |
| 5 | IN3 | Input, Channel 3 |
| 6 | -Vs | Negative Supply |
| 7 | IN4 | Input, Channel 4 |
| 8 | A0 | Logic Input A0 |
| 9 | A1 | Logic Input A1 |
| 10 | $\overline{EN}$ | Enable pin, “1” = Disable, “0” = Enable |
| 11 | SD | Shutdown pin, “1” = Shutdown, “0” = Active |
| 12 | -VIN | Inverting Input of output amplifier |
| 13 | OUT | Output |
| 14 | +Vs | Positive Supply |

## Truth Table

| A0 | A1 | $\overline{EN}$ | SD | OUT |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | CH4 |
| 0 | 1 | 0 | 0 | CH3 |
| 1 | 0 | 0 | 0 | CH2 |
| 0 | 0 | 0 | 0 | CH1 |
| X | X | 1 | 0 | Disable |
| X | X | X | 1 | Shutdown |

## Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_S$ | Supply Voltage | 0 | 12.6 | V |
| CMIR | Input Voltage Range | $-V_S$ - 0.5V | $+V_S$ + 0.5V | V |

## Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_C$ | Operating Temperature Range | -40 | | +85 | °C |
| $V_S$ | Supply Voltage Range | 5 | | 12 | V |

## Reliability Information

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Junction Temperature | | | 150 | °C |
| Storage Temperature Range | -65 | | 150 | °C |
| Lead Temperature (Soldering, 10s) | | | 300 | °C |
| 14-Lead SOIC[1] | | 128 | | °C/W |
| 14-Lead TSSOP[1] | | 130 | | °C/W |

Note:

1. Package thermal resistance (ΘJA), JDEC standard, multi-layer test boards, still air.

## ESD Protection

| Package | SOIC-14 | TSSOP-14 |
|---|---|---|
| Human Body Model (HBM) | TBD | TBD |
| Charge Device Model (CDM) | TBD | TBD |

## Electrical Characteristics at ±5V

$T_c$ = 25°C, $V_s$ = ± 5V, $R_f$ = 499Ω, $R_L$ = 150Ω, G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | **Frequency Domain Response** | | | | | |
| UGBW | -3dB Bandwidth | G = +1, $V_{OUT}$ = 0.2$V_{pp}$ | | TBD | | MHz |
| $BW_{ss}$ | -3dB Bandwidth | No Peaking, G = +2, $V_{OUT}$ = 0.2$V_{pp}$ | | 380 | | MHz |
| $BW_{Ls}$ | Full Power Bandwidth | No Peaking, G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 335 | | MHz |
| $BW_{0.1dBSS}$ | 0.1dB Gain Flatness | G = +2, $V_{OUT}$ = 0.2$V_{pp}$ | | 155 | | MHz |
| $BW_{0.1dBLS}$ | 0.1dB Gain Flatness | G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 80 | | MHz |
| | **Time Domain Response** | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 2V step; (10% to 90%) | | 1 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 2V step | | 15 | | ns |
| OS | Overshoot | $V_{OUT}$ = 0.2V step | | 5.7 | | % |
| SR | Slew Rate | 4V step. G = -1 | | 1600 | | V/µs |
| | **Distortion / Noise Response** | | | | | |
| HD2 | 2nd Harmonic Distortion | 2$V_{pp}$, 5MHz | | -70 | | dBc |
| HD3 | 3rd Harmonic Distortion | 2$V_{pp}$, 5MHz | | -79 | | dBc |
| THD | Total Harmonic Distortion | 2$V_{pp}$, 5MHz | | -81 | | dB |
| DG | Differential Gain | NTSC (3.58MHz) | | 0.02 | | % |
| DP | Differenital Phase | NTSC (3.58MHz) | | 0.03 | | ° |
| $e_n$ | Input Voltage Noise | > 1MHz | | 7 | | nV/Hz |
| $i_{n+}$ | Input Current Noise (+) | > 1MHz | | 22 | | pA/Hz |
| $i_{n-}$ | Input Current Noise (-) | > 1MHz | | 16 | | pA/Hz |
| $X_{TALK}$ | All Hostile Crosstalk | Channel-to-channel 5MHz/30MHz | | -85 / -65 | | dB |
| | **DC Performance** | | | | | |
| $V_{IO}$ | Input Offset Voltage[1] | | -9 | 1 | +9 | mV |
| $dV_{IO}$ | Average Drift | | | 8.5 | | µV/°C |
| $V_{IOM}$ | Input Offset Voltage Matching[1] | Channel to channel | -5 | TBD | 5 | mV |
| $I_{bn}$ | Input Bias Current non-inverting[1] | Pins 1,3,5,7 | -16 | 4 | 16 | µA |
| $dI_{bn}$ | Average Drift | | | 16 | | nA/°C |
| $I_{bi}$ | Input Bias Current inverting[1] | Pin 12 | -20 | 13 | 20 | µA |
| $dI_{bn}$ | Average Drift | | | 85 | | nA/°C |
| GM | Gain Matching | Channel-to-channel | | 0.05 | | % |
| PSRR | Power Supply Rejection Ratio[1] | DC | 54 | 60 | | dB |
| $I_S$ | Supply Current[1] | | | 13 | 18 | mA |
| $I_{EN}$ | Disable Supply Current[1] | Disable Mode | | 4 | 6 | mA |
| $I_{SD}$ | Shutdown Supply Current[1] | Shutdown Mode | | 3 | 5 | mA |
| | **Switching Characteristics** | | | | | |
| | Switching Time | Channel-to-Channel | | | | |
| | 50% Logic to 10% Output Settling | IN0, IN2 = +0.5V; IN1, IN3 = -0.5V | | 7.5 | | ns |
| | 50% Logic to 10% Output Settling | IN0, IN2 = +0.5V; IN1, IN3 = -0.5V | | 9.1 | | ns |
| | 50% Logic to 10% Output Settling | IN0, IN2 = +0.5V; IN1, IN3 = -0.5V | | 25 | | ns |
| | Channel Switching Transient (Glitch) | All inputs grounded | | 104 | | $mV_{pp}$ |

**Notes:**

1. 100% tested at 25°C

## Electrical Characteristics at ±5V continued

$T_c$ = 25°C, $V_s$ = ±5V, $R_f$ = 499Ω, $R_L$ = 150Ω, G = 2; unless otherwise noted.

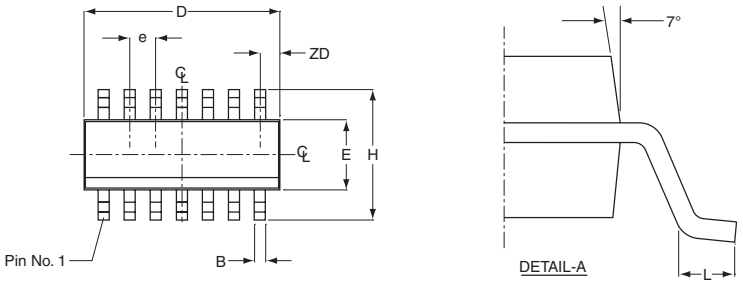
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | **Digital Inputs** | | | | | |
| $V_{IH}$ | Logic High Threshold | A0, A1, EN, and SD pins | 2.0 | | | V |
| $V_{IL}$ | Logic Low Threshold | A0, A1, EN, and SD pins | | | 0.08 | V |
| $I_{IH}$ | Logic Pin Input Current High | A0, A1, EN, and SD pins; Logic Input = 2.0V | | TBD | | µA |
| $I_{IL}$ | Logic Pin Input Current Low | A0, A1, EN, and SD pins; Logic Input = 0V | | TBD | | µA |
| | **Disable Characteristics** | | | | | |
| $EN_{ISO}$ | Disable Isolation | 5MHz / 30MHz | | -88 / -72 | | dB |
| $SD_{ISO}$ | Shutdown Isolation | 5MHz / 30MHz | | -92 /-77 | | dB |
| $CH_{ISO}$ | Channel-to-Channel Isolation | 5MHz | | -70 | | dB |
| $ENT_{ON}$ | Turn on time (Disable to ON) | | | 17 | | ns |
| $ENT_{OFF}$ | Turn off time (ON to Disable) | | | 120 | | ns |
| $SDT_{ON}$ | Turn on time (Shutdown to ON) | | | 20 | | ns |
| $SDT_{OFF}$ | Turn off time (On to Shutdown) | | | 115 | | ns |
| | **Input Characteristics** | | | | | |
| $R_{IN}$ | Input Resistance | | | TBD | | MΩ |
| $C_{IN}$ | Input Capacitance | | | TBD | | pF |
| CMIR | Input Common Mode Voltage Range | | | ±2.8 | | V |
| CMRR | Common Mode Rejection Ratio[1] | DC, $V_{CM}$ = ±1V | 50 | 52 | | dB |
| | **Output Characteristics** | | | | | |
| $V_O$ | Output Voltage Swing[1] | $R_L$ = 2kΩ | | ±3.8 | | V |
| | | $R_L$ = 150Ω | ±3.2 | ±3.7 | | V |
| $I_{OUT}$ | Linear Output Current | | | ±60 | | mA |
| $I_{SC}$ | Short Circuit Output Current | $V_O$ = GND | | ±100 | | mA |
| $R_{OUT}$ | Output Resistance | enabled | | TBD | | mΩ |
| | | disabled | | TBD | | MΩ |
| $C_{OUT}$ | Output Capacitance | | | TBD | | pF |

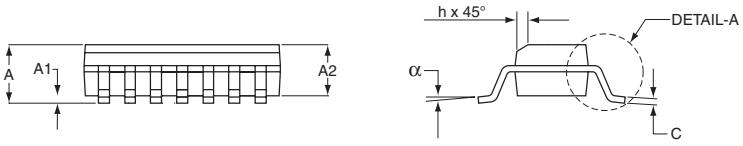
**Notes:**

1. 100% tested at 25°C

# Mechanical Dimensions

## 14-Lead Small Outline Package (SOIC)



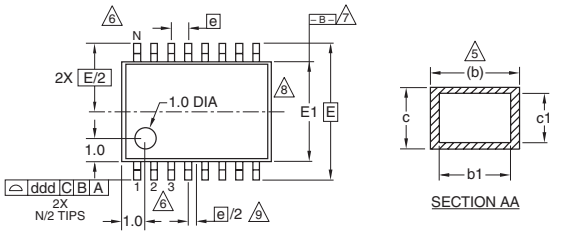



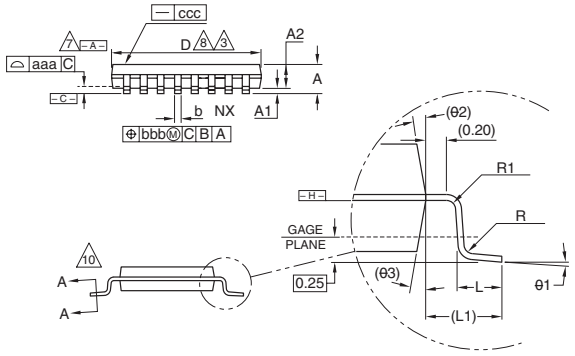

| SOIC-14 | | |
|---|---|---|
| **SYMBOL** | **MIN** | **MAX** |
| A1 | .0040 | .0098 |
| B | .014 | .018 |
| C | .0075 | .0098 |
| D | .337 | .344 |
| E | .150 | .157 |
| e | .050 BSC | |
| H | .2284 | .2440 |
| h | .0099 | .0196 |
| L | .016 | .050 |
| A | .060 | .068 |
| | 0° | 8° |
| ZD | 0.20 ref | |
| A2 | .054 | .062 |

**NOTE:**

1. All dimensions are in inches.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed o.152mm (.006) per side (d).

## 14-Lead Outline Package (TSSOP)




| TSSOP-14 | | | |
|---|---|---|---|
| **SYMBOL** | **MIN** | **NOM** | **MAX** |
| A | – | – | 1.10 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.85 | 0.90 | 0.95 |
| L | 0.50 | 0.60 | 0.75 |
| R | 0.09 | – | – |
| R1 | 0.09 | – | – |
| b | 0.19 | – | 0.30 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.09 | – | 0.20 |
| c1 | 0.09 | – | 0.16 |
| θ1 | 0° | – | 8° |
| L1 | 1.0 REF | | |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.05 | | |
| ddd | 0.20 | | |
| e | 0.65 BSC | | |
| θ2 | 12° REF | | |
| θ3 | 12° REF | | |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.4 BSC | | |
| e | 0.65 BSC | | |
| N | 14 | | |

**NOTES:**

1 All dimensions are in millimeters (angle in degrees).

2 Dimensioning and tolerancing per ASME Y14.5–1994.

3 Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .

4 Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.

5 Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar connot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.

6 Terminal numbers are shown for reference only.

7 Datums – A – and – B – to be determined at datum plane – H –.

8 Dimensions "D" and "E1" to be determined at datum plane – H –.

9 This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.

10 Cross sections A – A to be determined at 0.10 to 0.25mm from the leadtip.

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Rev. I18