

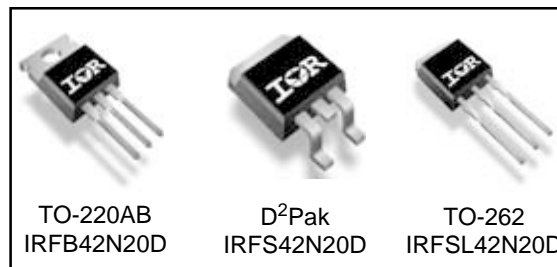
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	I_D
200V	0.055Ω	42.6A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	42.6	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	30	
I _{DM}	Pulsed Drain Current ①	170	
P _D @ T _A = 25°C	Power Dissipation ②	3.8	W
P _D @ T _C = 25°C	Power Dissipation	300	
	Linear Derating Factor	2	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	TBD	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input DC-DC Active Clamp Reset Forward Converter

Notes ① through ④ are on page 6

IRFB/IRFS/IRFSL42N20D

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	TBD	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.055	Ω	$V_{GS} = 10V, I_D = 25.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	TBD	—	—	S	$V_{DS} = 25V, I_D = 25.5A$
Q_g	Total Gate Charge	—	103	—	nC	$I_D = 25.5A$ $V_{DS} = 160V$ $V_{GS} = 10V$ ④
Q_{gs}	Gate-to-Source Charge	—	26	—		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	48	—		
$t_{d(on)}$	Turn-On Delay Time	—	TBD	—	ns	$V_{DD} = 100V$ $I_D = 25.5A$ $R_G = \text{TBD}\Omega$ $V_{GS} = 10V$ ④
t_r	Rise Time	—	TBD	—		
$t_{d(off)}$	Turn-Off Delay Time	—	TBD	—		
t_f	Fall Time	—	TBD	—		
C_{iss}	Input Capacitance	—	3470	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ ⑥
C_{oss}	Output Capacitance	—	560	—		
C_{rss}	Reverse Transfer Capacitance	—	120	—		
C_{oss}	Output Capacitance	—	TBD	—		
C_{oss}	Output Capacitance	—	TBD	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	TBD	—		

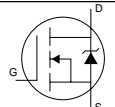
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	TBD	mJ
I_{AR}	Avalanche Current①	—	25.5	A
E_{AR}	Repetitive Avalanche Energy①	—	30	mJ

Thermal Resistance

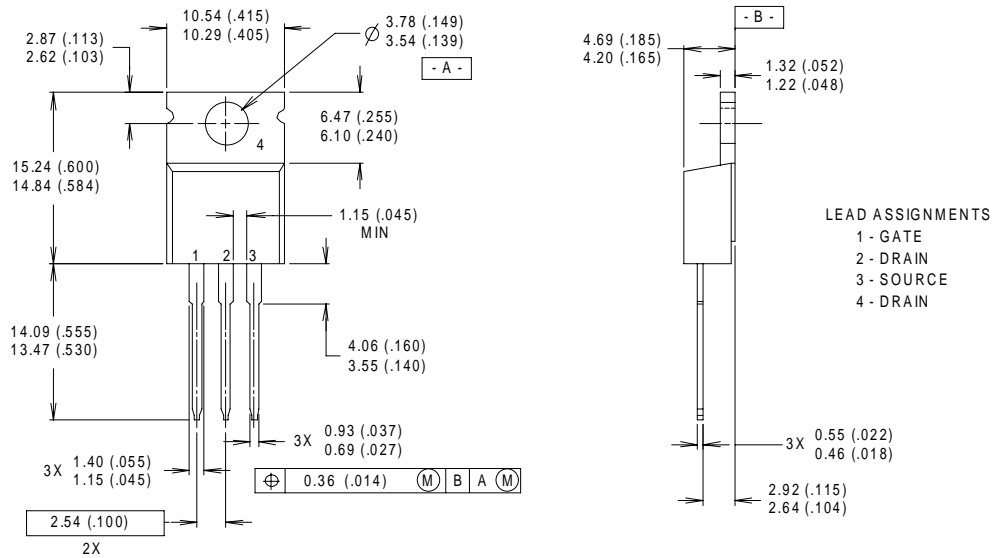
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	42.6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	170		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 25.5A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	TBD	TBD	ns	$T_J = 25^\circ\text{C}, I_F = 25.5A$
Q_{rr}	Reverse Recovery Charge	—	2.4	3.6	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



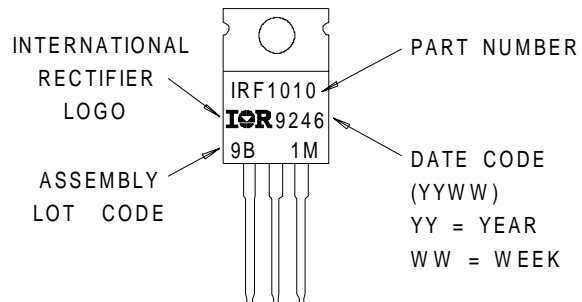
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

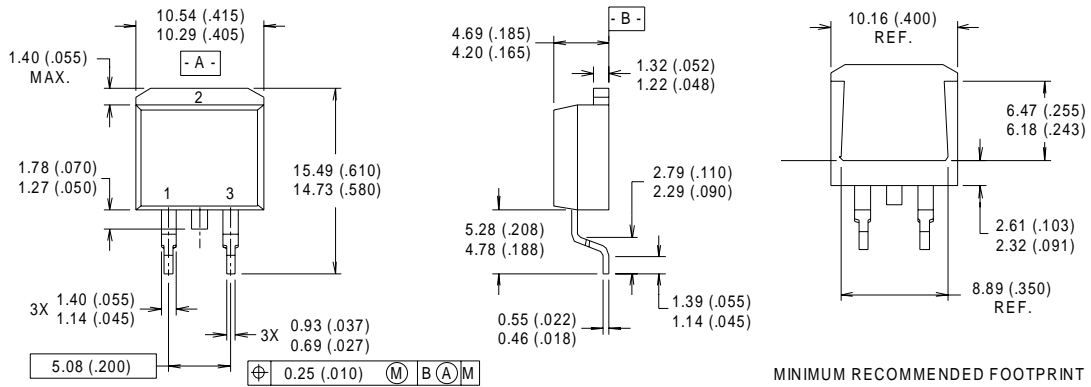
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



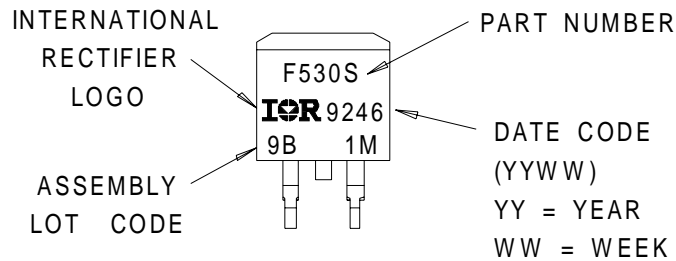
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

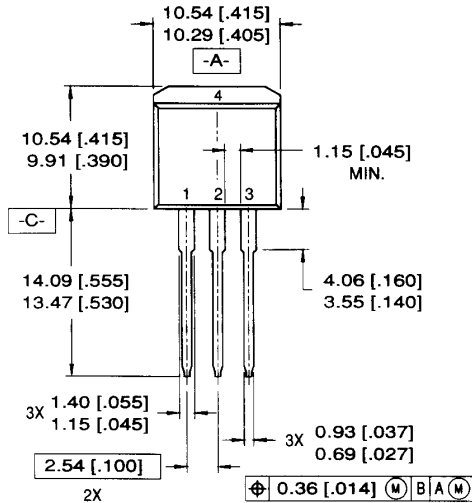
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

D²Pak Part Marking Information

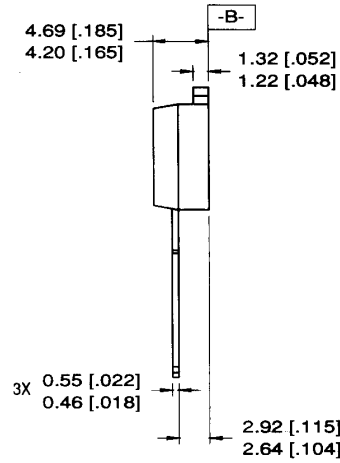


TO-262 Package Outline



LEAD ASSIGNMENTS

- 1 = GATE 3 = SOURCE
- 2 = DRAIN 4 = DRAIN

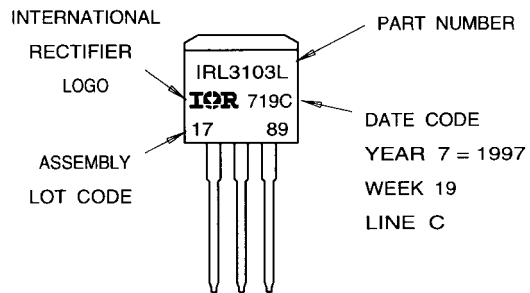


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

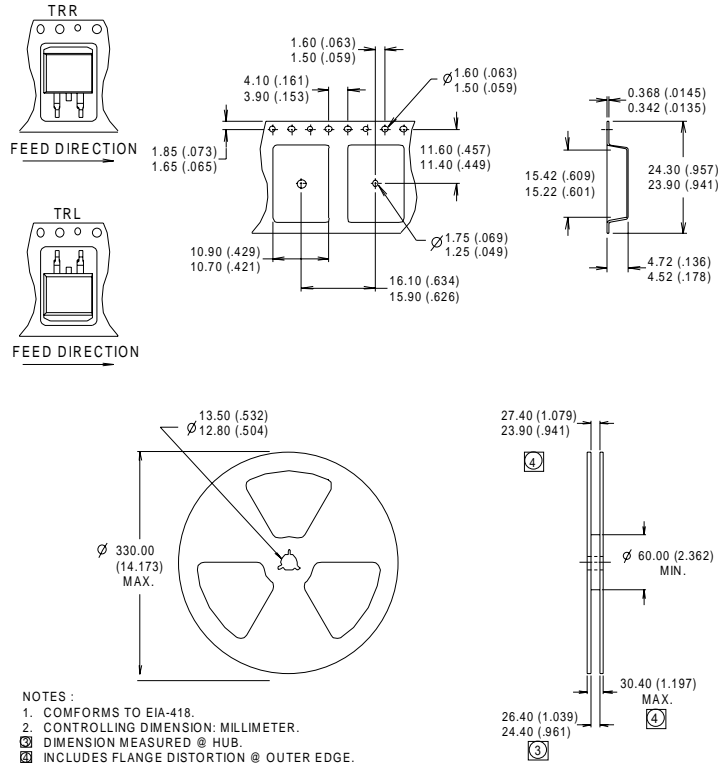


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D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = \text{TBDmH}$
 $R_G = \text{TBD}\Omega$, $I_{AS} = 25.5\text{A}$.
- ③ $I_{SD} \leq 25.5\text{A}$, $di/dt \leq \text{TBD}\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

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Data and specifications subject to change without notice. 9/00