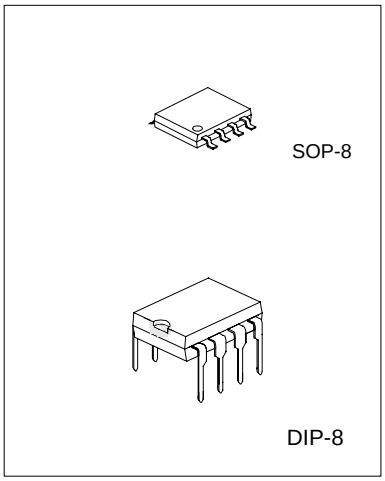
CURRENT MODE PWM CONTROL CIRCUITS



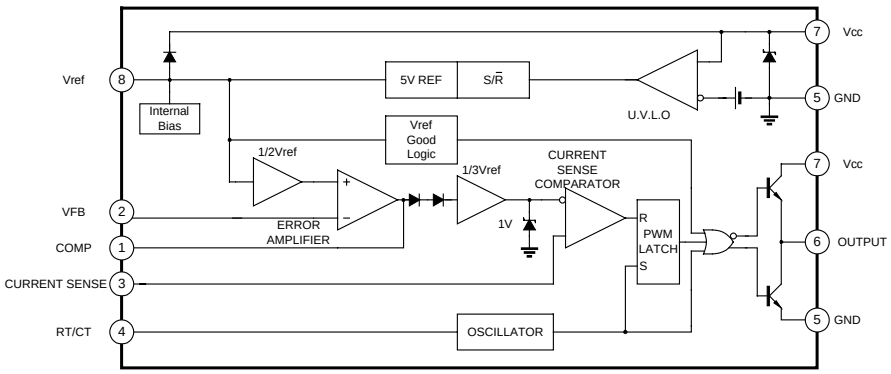
DESCRIPTION

The @vic AV3842A/3843A provide the necessary functions to implement off-line or DC to DC fixed frequency current mode , controlled switching circuits with a minimal external part count

FEATURES

*Low external part count.
*Low start up current (Typical 0.12mA)
*Automatic feed forward compensation
*Pulse-by-Pulse current limiting
*Under-voltage lockout with hysteresis
*Double pulse Suppression
*High current totem pole output to drive MOSFET directly
*Internally trimmed band gap reference
*500kHz operation

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage(Low Impedance Source)	V_{CC}	30	V
Supply Voltage(Icc<30mA)	Vcc	Self Limiting	V
Output Current (Peak)	Io	+-1	A
Output Energy(capacity Load)		5	µJ
Analog Inputs(pin 2,3)	$V_{I(ANA)}$	-0.3 ~ +6.3	V
Error Amplifier Output Sink Current	$I_{SINK(EA)}$	10	mA
Power Dissipation	PD DIP-8	at T_{amb}<=25°C 1.0	W
	SOP-8	at T_{amb}<=25°C 0.5	W
Lead Temperature(Soldering 10 Sec)	Tlead	300	°C

(continued)

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	Tstg	-65 ~ +150	°C
Operating junction temperature	Tj	+150	°C

Note 1: Ta>25°C, P_D derated with 8mW/°C.

ELECTRICAL CHARACTERISTICS (0°C <=Ta<=70°C, V_{CC}=15V, R_T=10kΩ, C_T=3.3nF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Output Voltage	V_{REF}	Tj=25°C,Io=1mA	4.9	5	5.1	V
Line Regulation	ΔV_{REF}	12<=V_{IN}<=25V		6	20	mV
Load Regulation	ΔV_{REF}	1<=Io=20mA		6	25	mV
Temperature Stability		(Note 2)		0.2	0.4	mV/°C
Total Output Variation		Line, Load, Temp(note 2)	4.82		5.18	V
Output Noise Voltage	Vosc	10Hz<=f<=10kHz,Tj=25°C (note 2)		50		uV
Long Term Stability		Ta=25°C,1000Hrs(note 2)		5	25	mV
Output Short Circuit	I_{SC}		-30	-100	-180	mA
Oscillator Section						
Initial Accuracy	f	Tj=25°C	47	52	57	kHz
Voltage Stability	Δf/ΔVcc	12<=Vcc<=25V		0.2	1	%
Temperature Stability		Tmin<=T_A<=Tmax(note 2)		5		%
Amplitude	Vosc	Vpin 4 peak to peak		1.7		V
Error Amplifier Section						
Input Voltage	$V_{I(EA)}$	Vpin 1=2.5V	2.42	2.50	2.58	V
Input Bias Current	I_{BIAS}			-0.3	-2	μA
A_{VOL}		2 <=Vo<=4V	60	90		dB
Unity Gain Bandwidth		Tj=25°C (note 2)	0.7	1		MHz
PSRR		I2<=Vcc<=25V	60	70		dB
Output Sink Current	Isink	Vpin 2=2.7V,Vpin 1=1.1V	2	6		mA
Output Source Current	Isource	Vpin 2=2.3V,Vpin 1=5V	-0.5	-0.8		mA
Vout High	V_{OH}	Vpin 2=2.3V, RL=15kΩ to GND	5	6		V
Vout Low	V_{OL}	Vpin 2=2.7V,Vpin 1=1.1V		0.7	1.1	V
Current Sense section						
Gain	G_V	(note 3,4)	2.85	3	3.15	V/V
Maximum Input signal	$V_{I(MAX)}$	Vpin 1=5V(note 3)	0.9	1	1.1	V
PSRR		12<=Vcc<=25V		70		dB
Input Bias Current	I_{BIAS}			-2	-10	μA
Delay to Output		Vpin 3=0 to 2V		150	300	ns
Output Section						
Output Low Level	V_{OL}	Isink=20mA		0.1	0.4	V
		Isink=200mA		1.5	2.2	V
Output High Level	V_{OH}	Isource=20mA	13	13.5		V
		Isource=200mA	12	13.5		V
Rise Time	t_R	Tj=25°C,C_L=1nF(note 2)		50	150	ns
Fall Time	t_F	Tj=25°C,C_L=1nF(note 2)		50	150	ns
Under-Voltage Lockout Output Section						
Start Threshold	$V_{TH(ST)}$	UTC3842A	14.5	16	17.5	V
		UTC3843A	7.8	8.4	9	V
Min. Operating Voltage	$V_{OPR(min)}$	After Turn On UTC3842A	8.5	10	11.5	
		UTC3843A	7	7.6	8.2	V
PWM Section						

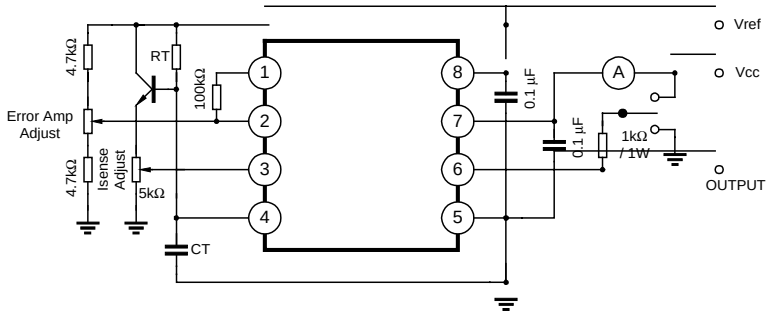
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Duty Cycle	D(MAX)		95	97	100	%
Minimum Duty Cycle	D(MIN)				0	%
Total Standby Current						
Start-up Current	IST			0.12	0.3	mA
Operating Supply Current	ICC(opr)	Vpin 2=Vpin 3=0V		11	17	mA
Vcc Zener Voltage	Vz	Icc=25mA		34		V

note 2:These parameters, although guaranteed ,are not 100% tested in production.
note 3:Parameters measured at trip point of latch with Vpin 2=0.
note 4:Gain defined as:

$$A=\frac{\Delta Vpin\ 1}{\Delta Vpin\ 3}\ ;\ 0<=Vpin3<=0.8V$$

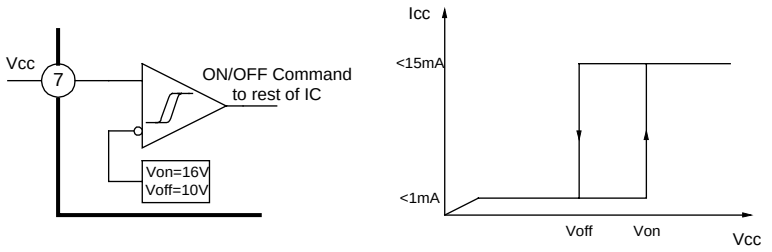
note 5:Adjust Vcc above the start threshold before setting at 15V.

OPEN-LOOP LABORATORY TEST FIXTURE



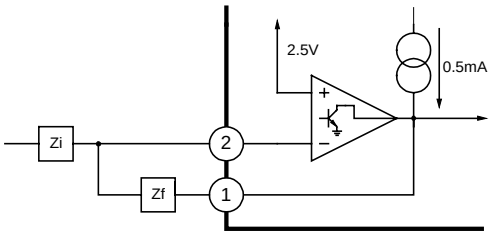
High peak current associated with capacity loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in single point GND. The transistor and 5kΩ potentio-meter are used to sample the oscillator waveform and apply an adjustable Ramp to Pin 3.

UNDER-VOLTAGE LOCKOUT



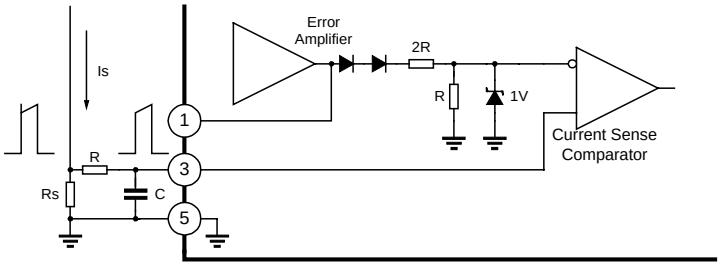
During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

ERROR AMPLIFIER CONFIGURATION



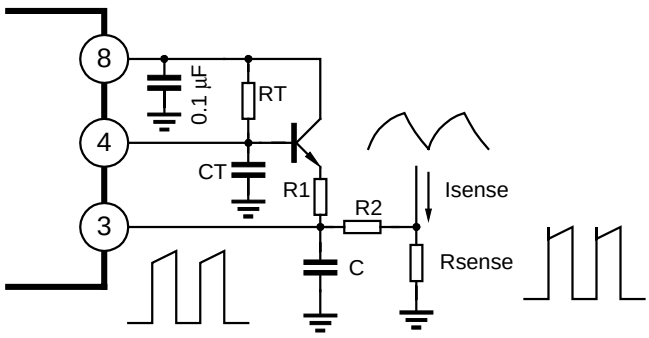
Error amplifier can source or sink up to 0.5mA

CURRENT SENSE CIRCUIT



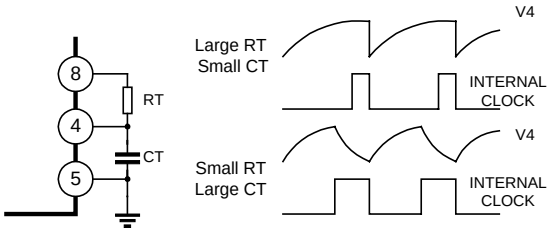
Peak current (Is) determined by the formula:
Ismax=10V/Rs.
A small RC filter be required to suppress switch transients.

SLOPE COMPENSATION

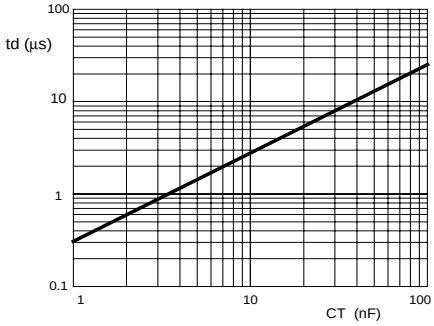


A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%.Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.

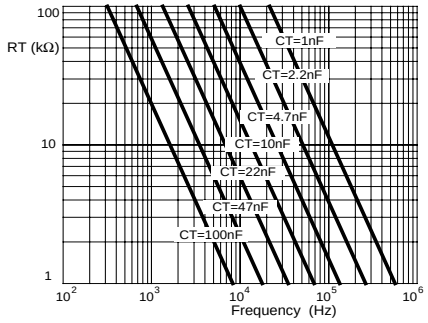
OSCILLATOR SECTION



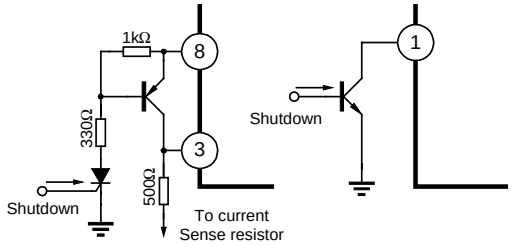
Dead time VS C_T(R_T>5kΩ)



Timing Resistance Vs Frequency

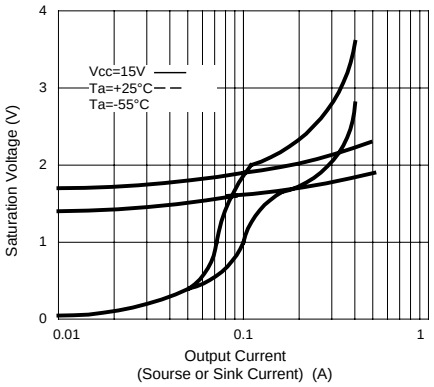


SHUTDOWN TECHNIQUES

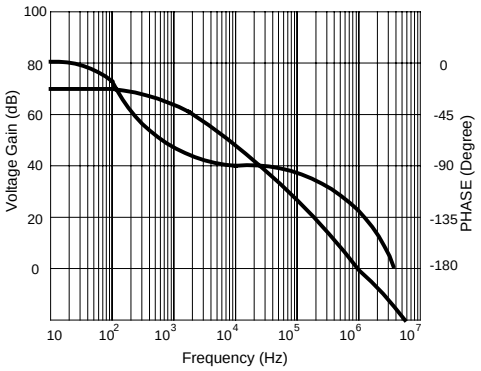


Shutdown UTC UC3842A can be accomplished by two methods; either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high(refer to block diagram).The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed . In one example, an externally latched shut –down may be accomplished by adding an SCR which be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.

TYPICAL PERFORMANCE CHARACTERISTICS

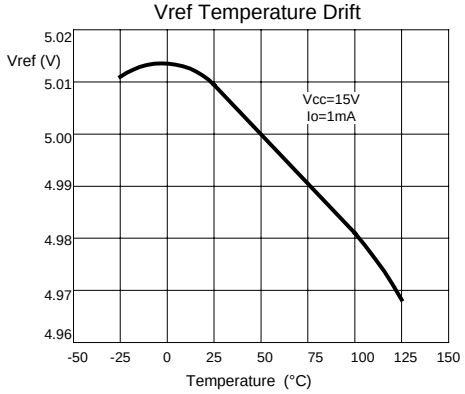


Output Saturation Characteristics

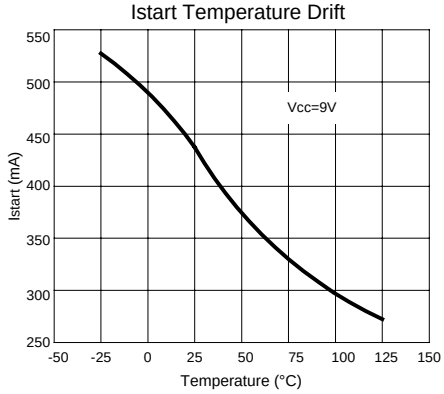


Error Amplifier Open-Loop Frequency Response

Vref Temperature Drift



Istart Temperature Drift



Icc Temperature Drift