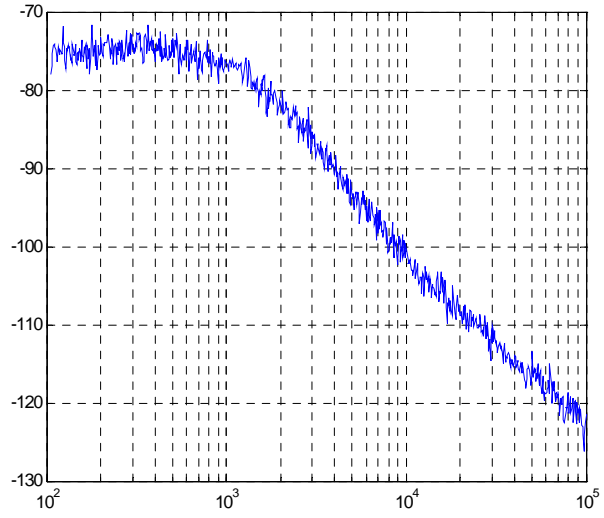




**PHASE NOISE (1 Hz BW, typical)**

**£(f) (dBc/Hz)**



**OFFSET (Hz)**

FEATURES
• Frequency Range: 102.4 - 102.4 MHz
• Step Size: 50 KHz
• cPLL - Style Package
APPLICATIONS
• Telecommunications
• Satellite
• Telemetry

PERFORMANCE SPECIFICATIONS	VALUE	UNITS
Frequency Range	102.4 - 102.4	MHz
Phase Noise @ 10 kHz offset (1 Hz BW, typ.)	-100	dBc/Hz
Harmonic Suppression (2nd, typ.)	-10	dBc
Sideband Spurs (typ.)	-65	dBc
Power Output	0±2	dBm
Load Impedance	50	Ω
Step Size	50	KHz
Charge Pump Output Current	1250	μA
Switching Speed (typ., adjacent channel)	n/a	mSec
Startup Lock Time (typ.)	4	mSec
Operating Temperature Range	-40 to 85	°C
Package Style	cPLL	
POWER SUPPLY REQUIREMENTS		
Supply Voltage (Vcc, nom.)	3	Vdc
Supply Current (Icc, typ.)	21	mA

All specifications are typical unless otherwise noted and subject to change without notice.

APPLICATION NOTES
• AN-107 : How to Solder Z-COMM VCOs / PLLs
• AN-200 : Mounting and Grounding of Z-COMM PLLs
• AN-201 : PLL Fundamentals      AN-202 : PLL Functional Description

**NOTES:**

Reference Oscillator Signal: 5 MHz <math>f\_{osc}</math> <math><100</math> MHz  
 Frequency Synthesizer: Analog Devices - ADF4001

**VCO TUNING CURVE, typ.**

**FREQUENCY (MHz)**

□ 70 °C  
■ 25 °C  
● °C

**TUNING VOLTAGE (Vdc)**

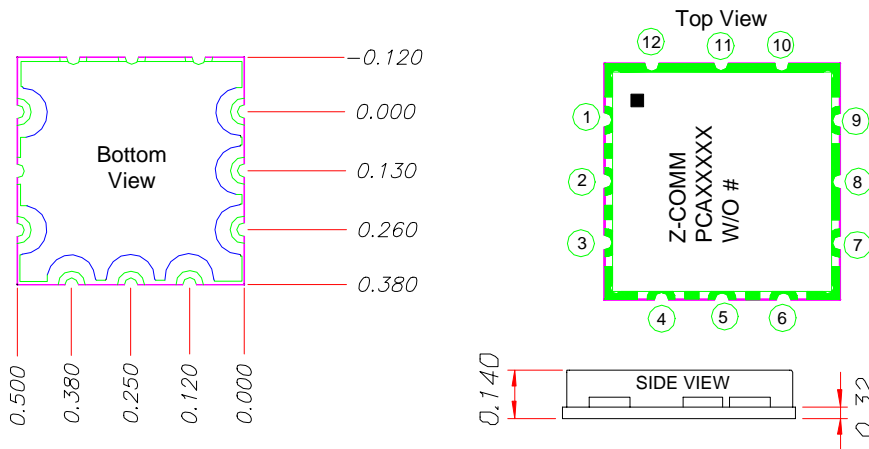
**VCO POWER CURVE, typ.**

**OUTPUT POWER (dBm)**

■ 25 °C

**FREQUENCY (MHz)**

**PHYSICAL DIMENSIONS**



1. The inside radius of all 14 half holes at the perimeter of the board are plated to provide a surface for the attachment of the PLL Module to the motherboard. 5 pads are for grounding, 8 pads are for signal interface.
2. The surface of the shield is tin-plated and may be soldered to. The shield's base metal is brass.
3. The ground plane on the bottom side is ground and attaches to a ground track on the top side of the board as well as to the shield.
4. Unless otherwise noted all dimensions are in inches.
5. Unless otherwise noted all tolerances are as follows:  
.xxx = ± .010

- P1 RF OUTPUT
- P2 REFERENCE OSCILLATOR INPUT
- P3 CLOCK
- P4 DATA
- P5 LOAD ENABLE
- P6 LOCK DETECT
- P7 VCC
- P8 GROUND
- P9 NO CONNECTION
- P10-12 GROUND