Section 19 Electrical Specifications

19.1 Absolute Maximum Ratings

Table 19-1 lists the absolute maximum ratings.

Table 19-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage (except port 7)	V_{in}	–0.3 to V_{CC} + 0.3	V
(port 7)	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recomended operating conditions.

19.2 Electrical Characteristics

19.2.1 DC Characteristics

Table 19-2 lists the DC characteristics.

Table 19-2 DC Characteristics

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%*1, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input High voltage	$\overline{RES}$, $\overline{STBY}$,	V_{IH}	V_{CC} – 0.7	–	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.7	–	V_{CC} + 0.3	V	
	Port 7		2.2	–	AV_{CC} + 0.3	V	
	Other input pins (except port 4)		2.2	–	V_{CC} + 0.3	V	
Input Low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2, MD_1, MD_0	V_{IL}	–0.3	–	0.5	V	
	Other input pins (except port 4)		–0.3	–	0.8	V	
Schmitt trigger input voltage	Port 4	V_{T^-}	1.0	–	2.5	V	
		V_{T^+}	2.0	–	3.5	V	
		V_{T^+}–V_{T^-}	0.4	–	–	V	
Input leakage current	$\overline{RES}$	| I_{in} |	–	–	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2, MD_1, MD_0, port 7		–	–	1.0	µA	
Leakage current in 3-state (off state)	Port 8, ports 6 to 1	| I_{TSI} |	–	–	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Output High voltage	All output pins	V_{OH}	V_{CC} – 0.5	–	–	V	I_{OH} = –200 µA
			3.5	–	–	V	I_{OH} = –1 mA
Output Low voltage	All output pins	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
	$\overline{RES}$		–	–	0.4	V	I_{OL} = 2.6 mA
Input copacitance	All input pins	C_{in}	–	–	20	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C

Note: *1 AV_{CC} must be connected to the power supply even when the A/D converter is not used.

Table 19-2 DC Characteristics (cont)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Current dissipation*1	Normal operation	Icc	–	15	30	mA	f = 6 MHz
			–	20	40	mA	f = 8 MHz
			–	25	50	mA	f = 10 MHz
	Sleep mode		–	9	20	mA	f = 6 MHz
			–	12	25	mA	f = 8 MHz
			–	15	30	mA	f = 10 MHz
	Standby		–	0.01	5.0	µA	Ta ≤ 50°C
			–	–	20.0	µA	Ta > 50°C
Analog supply current	During A/D conversion	AIcc	–	1.0	2.0	mA	
	While waiting		–	0.01	5.0	µA	

Note: *1 Current dissipation values assume that V_{IH} min = V_{CC} – 0.5 V, V_{IL} max = 0.5 V and all output pins are in the no-load state.

Conditions: V_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (Regular Specifications)
AV_{CC} = 5.0 V ±10%*1

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input High voltage	$\overline{RES}$, $\overline{STBY}$,	V_{IH}	V_{CC} × 0.9	–	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.9	–	V_{CC} + 0.3	V	
	Port 7		V_{CC} × 0.7	–	AV_{CC} + 0.3	V	
	Other input pins (except port 4)		V_{CC} × 0.7	–	V_{CC} + 0.3	V	
Input Low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2, MD_1, MD_0	V_{IL}	–0.3	–	V_{CC} × 0.1	V	
	Other input pins (except port 4)		–0.3	–	V_{CC} × 0.15	V	
Schmitt trigger input voltage	Port 4	V_{T^-}	V_{CC} × 0.2	–	V_{CC} × 0.6	V	
		V_{T^+}	V_{CC} × 0.4	–	V_{CC} × 0.7	V	
		V_{T^+}–V_{T^-}	V_{CC} × 0.07	–	–	V	
Input leakage current	$\overline{RES}$	| Iin |	–	–	10.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	$\overline{STBY}$, NMI, MD_2, MD_1, MD_0, port 7		–	–	1.0	µA	

Note: *1 AV_{CC} must be connected to the power supply even when the A/D converter is not used.

Table 19-2 DC Characteristics (cont)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Leakage current in 3-state (off state)	Port 8, ports 6 to 1	$\|I_{TSI}\|$	–	–	1.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
Output High voltage	All output pins	V_{OH}	V_{CC} – 0.4	–	–	V	I_{OH} = –200 µA
			V_{CC} – 0.9	–	–	V	I_{OH} = –1 mA
Output Low voltage	All output pins	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
	$\overline{RES}$		–	–	0.4	V	I_{OL} = 2.6 mA
Input capacitance	All input pins	C_{in}	–	–	20	pF	V_{in} = 0 V, f = 1 MHz, Ta = 25°C
Current dissipation*1	Normal operation	I_{CC}	–	20	28	mA	f = 5 MHz
	Sleep mode		–	12	18	mA	f = 5 MHz
	Standby		–	0.01	5.0	µA	Ta ≤ 50°C
			–	–	20.0	µA	Ta > 50°C
Analog supply current	During A/D conversion	AI_{CC}	–	1.0	2.0	mA	
	While waiting		–	0.01	5.0	µA	

Note: *1 Current dissipation values assume that V_{IH} min = V_{CC} × 0.9 V, V_{IL} max = 0.3 V and all output pins are in the no-load state.

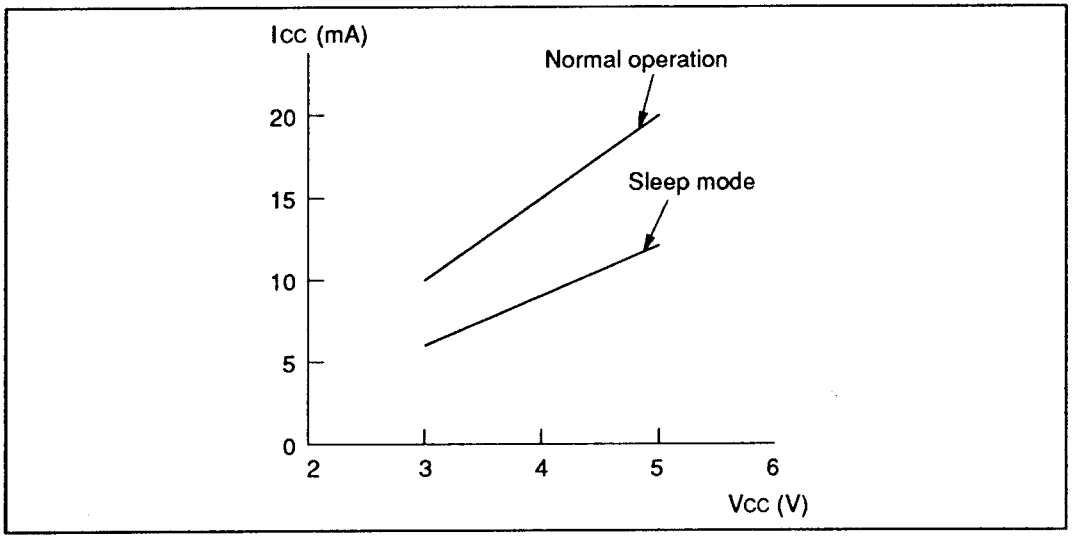

Figure 19-1 Relation between I_{CC} and V_{CC}

Table 19-3 Allowable Output Current Sink Values

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output Low current sink (per pin)	Per output pin	I_{OL}	–	–	2.0	mA
Allowable output Low current sink (total)	Total of all output pins	ΣI_{OL}	–	–	80	mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	–	–	2.0	mA
Allowable output High current sink (total)	Total of all output pins	$\Sigma -I_{OH}$	–	–	25	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 19-3. In particular, when driving a Darlington transistor pair directly, be sure to insert a current-limiting resistor in the output path. See figure 19-2.

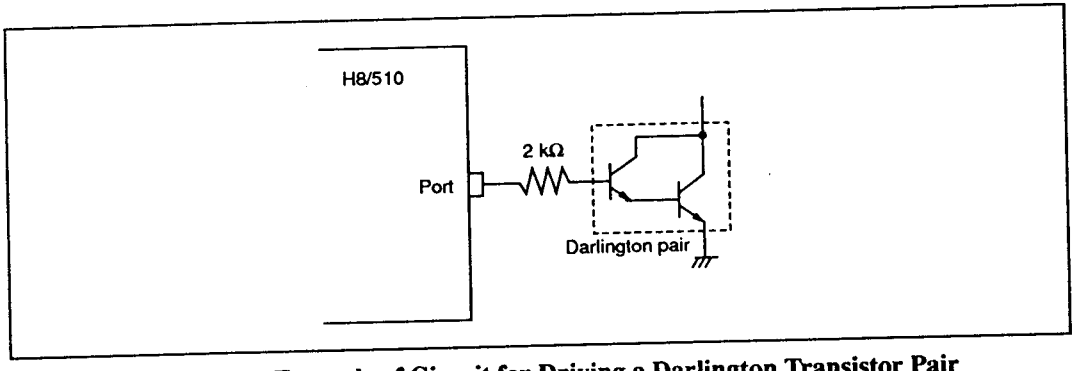

Figure 19-2 Example of Circuit for Driving a Darlington Transistor Pair

19.2.2 AC Characteristics

The AC characteristics of the H8/510 chip are listed in three tables. Bus timing parameters are given in table 20-4, control signal timing parameters in table 20-5, and timing parameters of the on-chip supporting modules in table 20-6.

Table 19-4 Bus Timing

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, ø = 0.5 to 10 MHz, V_{SS} = 0 V
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

		6 MHz		8 MHz		10 MHz			Measurement
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Clock cycle time	t_{cyc}	166.7	2000	125	2000	100	2000	ns	See figures
Clock pulse width Low	t_{CL}	65	–	45	–	40	–	ns	19-4 and 19-5
Clock pulse width High	t_{CH}	65	–	45	–	40	–	ns	
Clock rise time	t_{Cr}	–	15	–	15	–	10	ns	
Clock fall time	t_{Cf}	–	15	–	15	–	10	ns	
Address delay time	t_{AD}	–	50	–	40	–	30	ns	
Address hold time	t_{AH1}	30	–	25	–	15	–	ns	
Read strobe delay time 1	t_{RDD1}	–	50	–	40	–	30	ns	
Read strobe delay time 2	t_{RDD2}	–	50	–	40	–	40	ns	
Read strobe width High 1	t_{ASH1}	110	–	85	–	70	–	ns	
Read strobe width High 2	t_{ASH2}	110	–	85	–	70	–	ns	
Write strobe delay time 1	t_{WRD1}	–	50	–	40	–	30	ns	
Write strobe delay time 2	t_{WRD2}	–	50	–	40	–	30	ns	
Write strobe delay time 3	t_{WRD3}	–	50	–	40	–	30	ns	
Write data strobe pulse width1	t_{WRW1}	150	–	110	–	90	–	ns	
Write data strobe pulse width2	t_{WRW2}	200	–	150	–	120	–	ns	
Address setup time 1	t_{AS1}	25	–	20	–	15	–	ns	
Address setup time 2	t_{AS2}	25	–	20	–	15	–	ns	
Address setup time 3	t_{AS3}	105	–	80	–	65	–	ns	
Read data setup time	t_{RDS}	40	–	30	–	20	–	ns	
Read data hold time	t_{RDH}	0	–	0	–	0	–	ns	
Read data access time 1	t_{ACC1}	–	160	–	125	–	100	ns	
Read data access time 2	t_{ACC2}	–	300	–	230	–	180	ns	
Read data access time 3	t_{ACC3}	–	81.7	–	60	–	55	ns	
Read data access time 4	t_{ACC4}	–	230	–	165	–	135	ns	
Write data delay time	t_{WDD}	–	70	–	60	–	50	ns	
Write data setup time	t_{WDS}	30	–	15	–	10	–	ns	
Write data hold time	t_{WDH}	30	–	25	–	20	–	ns	
Wait setup time	t_{WTS}	40	–	40	–	40	–	ns	See figure 19-6
Wait hold time	t_{WTH}	10	–	10	–	10	–	ns	
Bus request setup time	t_{BRQS}	40	–	40	–	40	–	ns	See figure 19-11
Bus acknowledge delay time 1	t_{BACD1}	–	70	–	60	–	50	ns	
Bus acknowledge delay time 2	t_{BACD2}	–	70	–	60	–	50	ns	
Bus floating delay time	t_{BZD}	–	t_{BACD1}	–	t_{BACD1}	–	t_{BACD1}	ns	

Table 19-4 Bus Timing (cont)

Item	Symbol	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Measurement Conditions
E clock delay time	tED	–	20	–	15	–	15	ns	See figure 19-12
E clock rise time	tER	–	15	–	15	–	15	ns	
E clock fall time	tEF	–	15	–	15	–	15	ns	
Read data hold time (E clock sync)	tRDHE	0	–	0	–	0	–	ns	See figure 19-7
Write data hold time (E clock sync)	tWDHE	50	–	40	–	30	–	ns	

Conditions: V_{CC} = 3.0 V to 5.5 V, ø = 0.5 to 5.0 MHz, V_{SS} = 0 V
T_a = –20 to +75°C (Regular Specifications)

Item	Symbol	5 MHz Min	5 MHz Max	Unit	Measurement Conditions
Clock cycle time	tcyc	200	2000	ns	See figures
Clock pulse width Low	tCL	60	–	ns	19-4 and 19-5
Clock pulse width High	tCH	60	–	ns	
Clock rise time	tCr	–	25	ns	
Clock fall time	tCf	–	25	ns	
Address delay time	tAD	–	80	ns	
Address hold time (read)	tAH1	5	–	ns	
Address hold time (write)	tAH2	20	–	ns	
Read strobe delay time 1	tRDD1	–	80	ns	
Read strobe delay time 2	tRDD2	–	120	ns	
Write strobe delay time 1	tWRD1	–	80	ns	
Write strobe delay time 2	tWRD2	–	80	ns	
Write strobe delay time 3	tWRD3	–	80	ns	
Write data strobe pulse width1	tWRW1	150	–	ns	
Write data strobe pulse width2	tWRW2	220	–	ns	
Address setup time 1	tAS1	30	–	ns	
Address setup time 2	tAS2	30	–	ns	
Address setup time 3	tAS3	130	–	ns	
Read data setup time	tRDS	50	–	ns	
Read data hold time	tRDH	0	–	ns	
Read data access time 1	tACC1	–	180	ns	
Read data access time 2	tACC2	–	350	ns	
Write data delay time	tWDD	–	120	ns	
Write data setup time	tWDS	10	–	ns	
Write data hold time	tWDH	40	–	ns	

Table 19-4 Bus Timing (cont)

Item	Symbol	5 MHz Min	5 MHz Max	Unit	Measurement Conditions
Wait setup time	t_{WTS}	60	–	ns	See figure 19-6
Wait hold time	t_{WTH}	20	–	ns	
Bus request setup time	t_{BRQS}	80	–	ns	See figure 19-11
Bus acknowledge delay time 1	t_{BACD1}	–	80	ns	
Bus acknowledge delay time 2	t_{BACD2}	–	80	ns	
Bus floating delay time	t_{BZD}	–	t_{BACD1}	ns	
E clock delay time	t_{ED}	–	50	ns	See figure 19-12
E clock rise time	t_{ER}	–	25	ns	
E clock fall time	t_{EF}	–	25	ns	
Read data hold time (E clock sync)	t_{RDHE}	30	–	ns	See figure 19-7
Write data hold time (E clock sync)	t_{WDHE}	40	–	ns	

Table 19-5 Control Signal Timing

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, ø = 0.5 to 10 MHz, V_{SS} = 0 V
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

Item	Symbol	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Measurement Conditions
$\overline{RES}$ setup time	t_{RESS}	200	–	200	–	200	–	ns	See figure 19-8
$\overline{RES}$ pulse width	t_{RESW}	6.0	–	6.0	–	6.0	–	t_{cyc}	
$\overline{RES}$ output delay time	t_{RESD}	–	100	–	100	–	100	ns	See figure 19-8
$\overline{RES}$ output pulse width	t_{RESOW}	132	–	132	–	132	–	t_{cyc}	
NMI setup time	t_{NMIS}	150	–	150	–	150	–	ns	See figure 19-10
NMI hold time	t_{NMIH}	10	–	10	–	10	–	ns	
$\overline{IRQ_0}$ setup time	t_{IRQ0S}	50	–	50	–	50	–	ns	
$\overline{IRQ_1}$ setup time	t_{IRQ1S}	50	–	50	–	50	–	ns	
$\overline{IRQ_1}$ hold time	t_{IRQ1H}	10	–	10	–	10	–	ns	
NMI pulse width (for recovery from software standby mode)	t_{NMIW}	200	–	200	–	200	–	ns	
Crystal oscillator settling time (reset)	t_{OSC1}	20	–	20	–	20	–	ms	See figure 19-11
Crystal oscillator settling time (software standby)	t_{OSC2}	10	–	10	–	10	–	ms	See figure 18-1

Table 19-5 Control Signal Timing (cont)

Conditions: V_{CC} = 3.0 V to 5.5 V, ø = 0.5 to 5.0 MHz, V_{SS} = 0 V
T_a = –20 to +75°C (Regular Specifications)

Item	Symbol	5 MHz Min	5 MHz Max	Unit	Measurement Conditions
$\overline{RES}$ setup time	t_{RESS}	300	–	ns	See figure 19-8
$\overline{RES}$ pulse width	t_{RESW}	6.0	–	t_{cyc}	
$\overline{RES}$ output delay time	t_{RESD}	–	150	ns	See figure 19-8
$\overline{RES}$ output pulse width	t_{RESOW}	132	–	t_{cyc}	
NMI setup time	t_{NMIS}	300	–	ns	See figure 19-10
NMI hold time	t_{NMIH}	10	–	ns	
$\overline{IRQ_0}$ setup time	t_{IRQ0S}	100	–	ns	
$\overline{IRQ_1}$ setup time	t_{IRQ1S}	100	–	ns	
$\overline{IRQ_1}$ hold time	t_{IRQ1H}	10	–	ns	
NMI pulse width (for recovery from software standby mode)	t_{NMIW}	200	–	ns	
Crystal oscillator settling time (reset)	t_{OSC1}	20	–	ms	See figure 19-13
Crystal oscillator settling time (software standby)	t_{OSC2}	10	–	ms	See figure 18-1

Table 19-6 Timing Conditions of On-Chip Supporting Modules

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, ø = 0.5 to 10 MHz, V_{SS} = 0 V
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

Item			Symbol	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Measurement Conditions
FRT	Timer output delay time		t_{FTOD}	–	100	–	100	–	100	ns	See figure 19-15
	Timer input setup time		t_{FTIS}	50	–	50	–	50	–	ns	
	Timer clock input setup time		t_{FTCS}	50	–	50	–	50	–	ns	See figure 19-16
	Timer clock pulse width		t_{FTCW}	1.5	–	1.5	–	1.5	–	t_{cyc}	
TMR	Timer output delay time		t_{TMOD}	–	100	–	100	–	100	ns	See figure 19-17
	Timer clock input setup time		t_{TMCS}	50	–	50	–	50	–	ns	See figure 19-18
	Timer clock pulse width		t_{TMCW}	1.5	–	1.5	–	1.5	–	t_{cyc}	
	Timer reset input setup time		t_{TMRS}	50	–	50	–	50	–	ns	See figure 19-19
SCI	Input clock cycle	(Async)	t_{Scyc}	2	–	2	–	2	–	t_{cyc}	See figure 19-20
		(Sync)		4	–	4	–	4	–	t_{cyc}	
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	
	Transmit data delay time	(Sync)	t_{TXD}	–	100	–	100	–	100	ns	See figure 19-21
	Receive data setup time	(Sync)	t_{RXS}	100	–	100	–	100	–	ns	
	Receive data hold time	(Sync)	t_{RXH}	100	–	100	–	100	–	ns	
Port	Output data delay time		t_{PWD}	–	100	–	100	–	100	ns	See figure 19-14
	Input data setup time		t_{PRS}	50	–	50	–	50	–	ns	
	Input data hold time		t_{PRH}	50	–	50	–	50	–	ns	
RFSH	Refresh output delay time 1		t_{RFD1}	–	50	–	45	–	40	ns	See figure 19-22
	Refresh output delay time 2		t_{RFD2}	–	50	–	45	–	40	ns	

Table 19-6 Timing Conditions of On-Chip Supporting Modules (cont)

Conditions: V_{CC} = 3.0 V to 5.5 V, ø = 0.5 to 5.0 MHz, V_{SS} = 0 V
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

Item			Symbol	5 MHz Min	5 MHz Max	Unit	Measurement Conditions
FRT	Timer output delay time		tFTOD	–	150	ns	See figure 19-15
	Timer input setup time		tFTIS	80	–	ns	
	Timer clock input setup time		tFTCS	80	–	ns	See figure 19-16
	Timer clock pulse width		tFTCW	1.5	–	tcyc	
TMR	Timer output delay time		tTMOD	–	150	ns	See figure 19-17
	Timer clock input setup time		tTMCS	80	–	ns	See figure 19-18
	Timer clock pulse width		tTMCW	1.5	–	tcyc	
	Timer reset input setup time		tTMRS	80	–	ns	See figure 19-19
SCI	Input clock cycle	(Async)	tScyc	2	–	tcyc	See figure 19-20
		(Sync)		4	–	tcyc	
	Input clock pulse width		tSCKW	0.4	0.6	tScyc	
	Transmit data delay time	(Sync)	tTXD	–	200	ns	See figure 19-21
	Receive data setup time	(Sync)	tRXS	150	–	ns	
	Receive data hold time	(Sync)	tRXH	150	–	ns	
Port	Output data delay time		tPWD	–	150	ns	See figure 19-14
	Input data setup time		tPRS	80	–	ns	
	Input data hold time		tPRH	80	–	ns	
RFSH	Refresh output delay time 1		tRFD1	–	80	ns	See figure 19-22
	Refresh output delay time 2		tRFD2	–	80	ns	

- **Measurement Conditions for AC Characteristics**

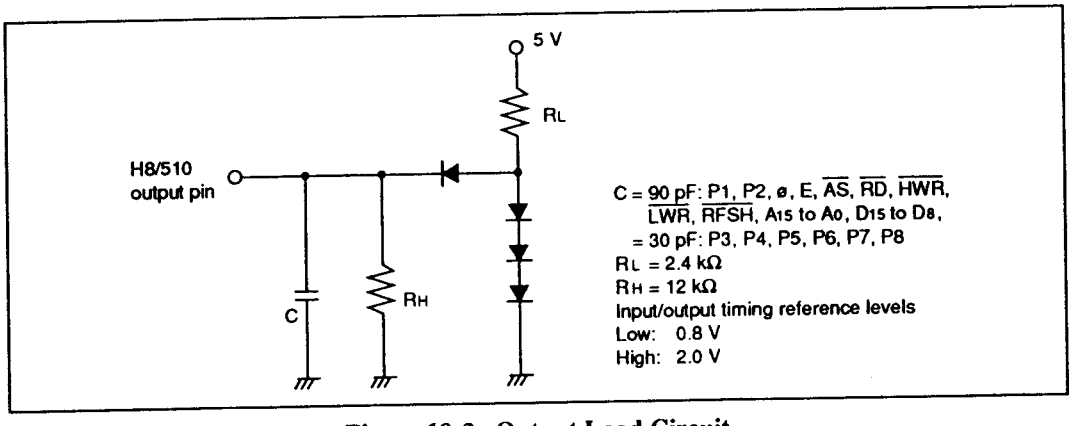

Figure 19-3 Output Load Circuit

19.2.3 A/D Converter Characteristics

Table 19-7 lists the characteristics of the on-chip A/D converter.

Table 19-7 A/D Converter Characteristics

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V,
T_a = –20 to +75°C (Regular Specifications)
T_a = –40 to +85°C (Wide-Range Specifications)

	6 MHz			8 MHz			10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	22.33	—	—	16.75	—	—	13.4	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±3	—	—	±3	—	—	±3	LSB
Offset error	—	—	±2	—	—	±2	—	—	±2	LSB
Full-scale error	—	—	±2	—	—	±2	—	—	±2	LSB
Quantizing error	—	—	±1/2	—	—	±1/2	—	—	±1/2	LSB
Absolute accuracy	—	—	±4	—	—	±4	—	—	±4	LSB

Conditions: V_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to +75°C (Regular Specifications)
AV_{CC} = 5.0 V ± 10%

	5 MHz			
Item	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	Bits
Conversion time	—	—	26.8	µs
Analog input capacitance	—	—	20	pF
Allowable signal-source impedance	—	—	10	kΩ
Nonlinearity error	—	—	±3	LSB
Offset error	—	—	±2	LSB
Full-scale error	—	—	±2	LSB
Quantizing error	—	—	±1/2	LSB
Absolute accuracy	—	—	±4	LSB

19.3 MCU Operational Timing

This section provides the following timing charts:

19.3.1 Bus timing	Figures 19-4 to 19-7
19.3.2 Control Signal Timing	Figures 19-8 to 19-11
19.3.3 Clock Timing	Figures 19-12 and 19-13
19.3.4 I/O Port Timing	Figure 19-14
19.3.5 16-Bit Free-Running Timer Timing	Figures 19-15 and 19-16
19.3.6 8-Bit Timer Timing	Figures 19-17 to 19-19
19.3.7 Serial Communication Interface Timing	Figures 19-20 and 19-21
19.3.8 Refresh Timing	Figures 19-22 and 19-23

19.3.1 Bus Timing

1. Basic Bus Cycle (Two-State Mode)

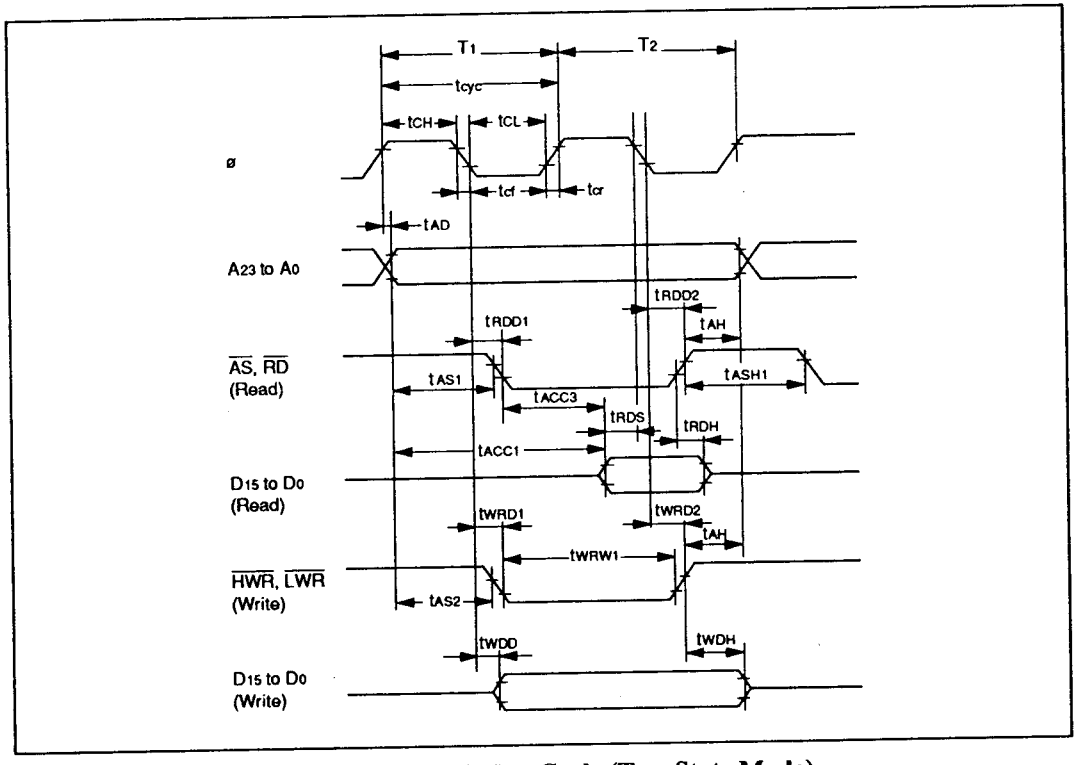

Figure 19-4 Basic Bus Cycle (Two-State Mode)

2. Basic Bus Cycle (Three-State Mode)

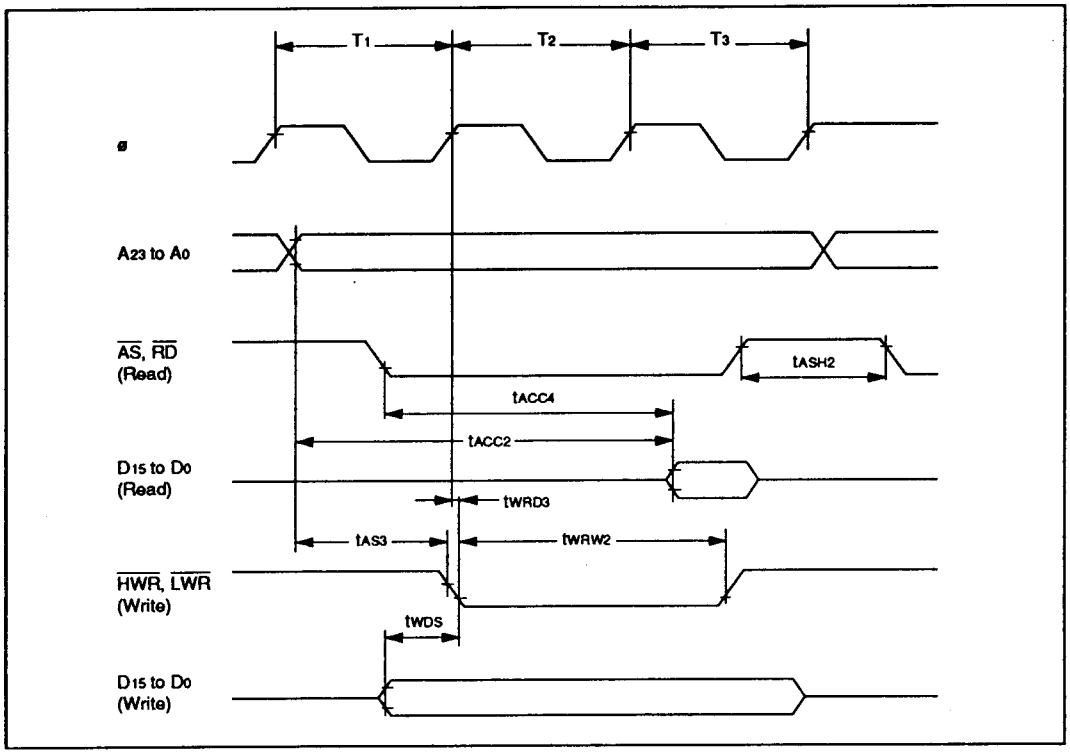

Figure 19-5 Basic Bus Cycle (Three-State Mode)

3. Basic Bus Cycle (Three-State Mode with One Wait State)

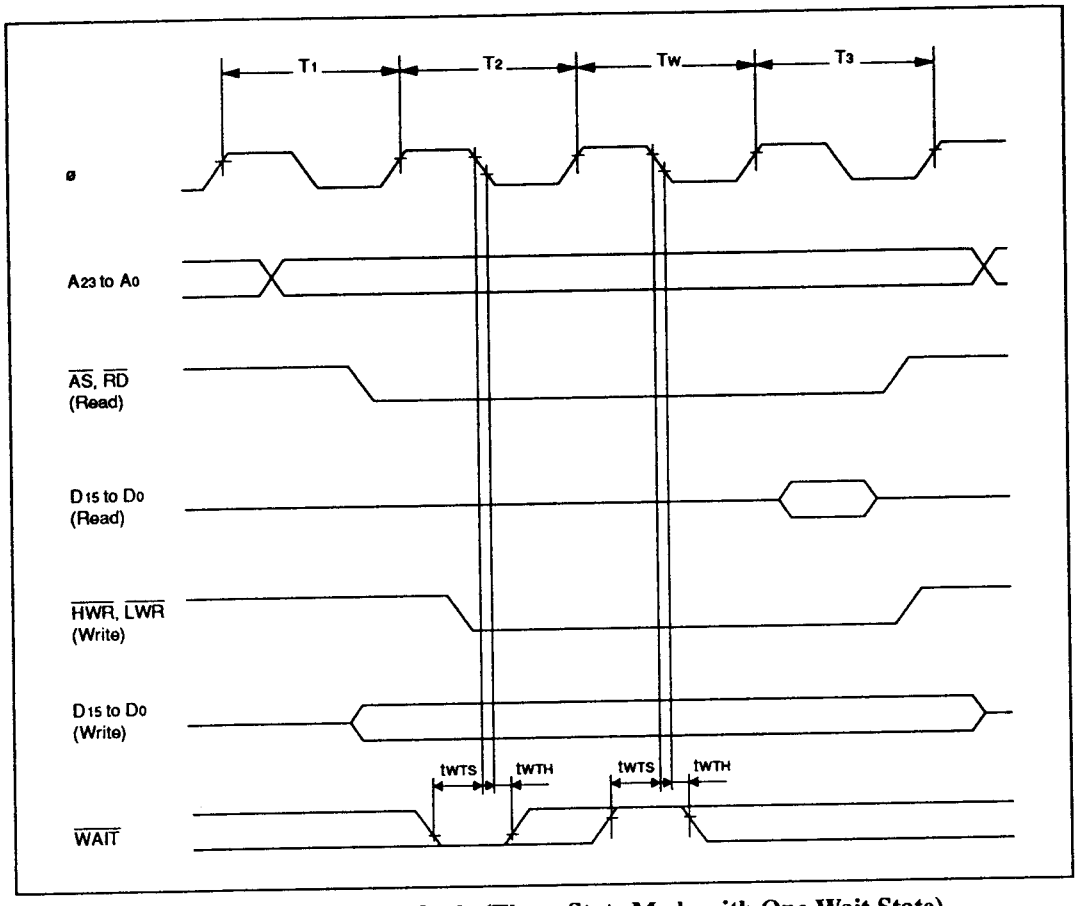

Figure 19-6 Basic Bus Cycle (Three-State Mode with One Wait State)

4. Bus Cycle Synchronized with E Clock

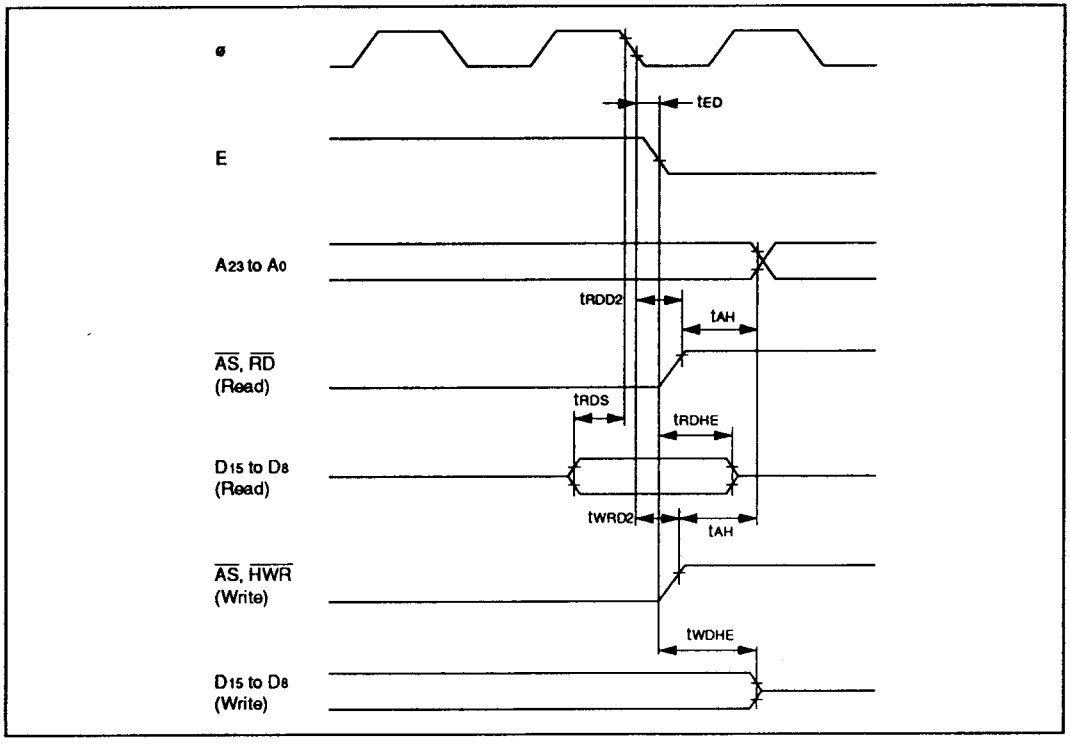

Figure 19-7 Bus Cycle Synchronized with E Clock

19.3.2 Control Signal Timing

1. Reset Input Timing

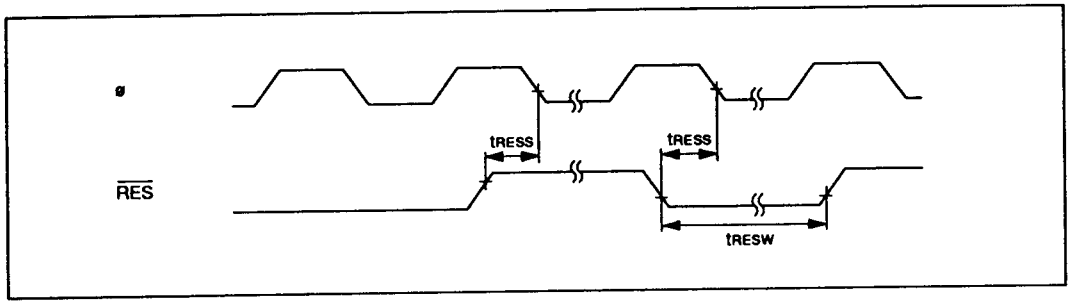

Figure 19-8 Reset Input Timing

2. Reset Output Timing

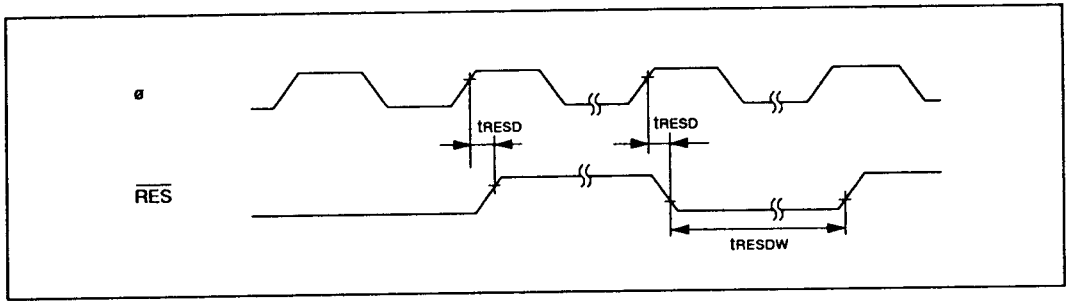

Figure 19-9 Reset Output Timing

3. Interrupt Input Timing

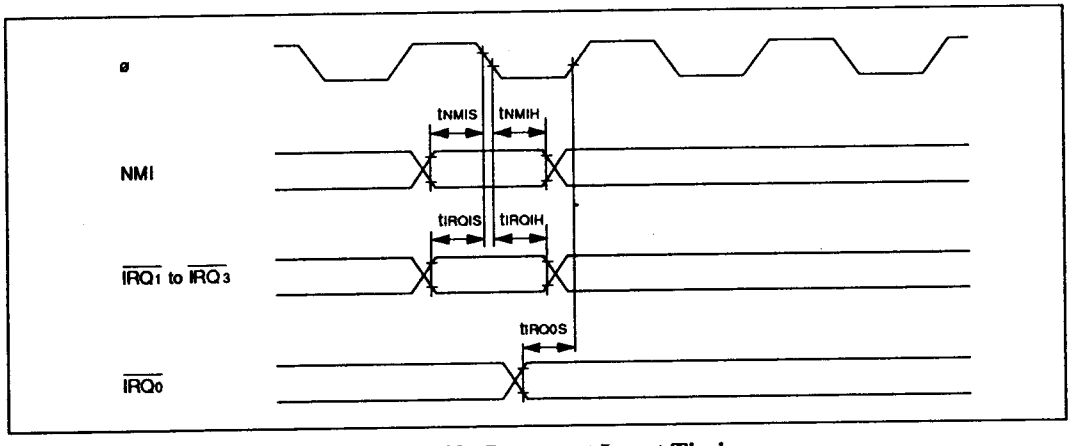

Figure 19-10 Interrupt Input Timing

4. Bus Release State Timing

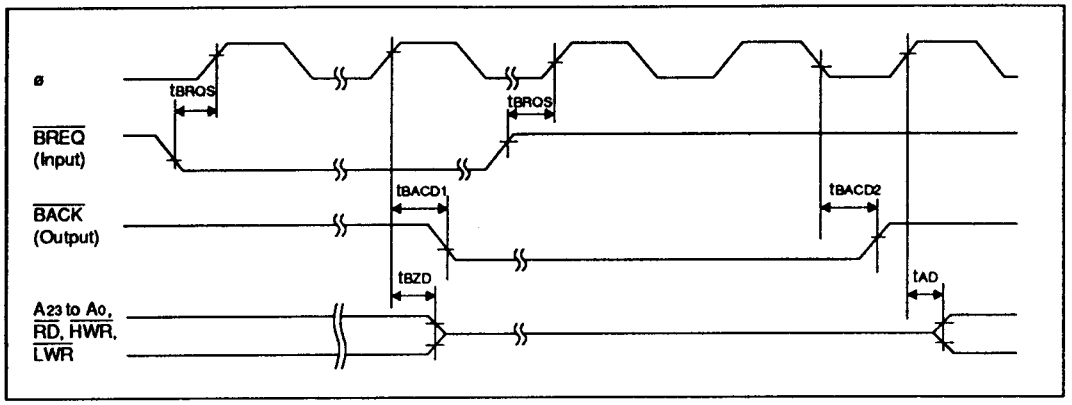

Figure 19-11 Bus Release State Timing

19.3.3 Clock Timing

1. E Clock Timing

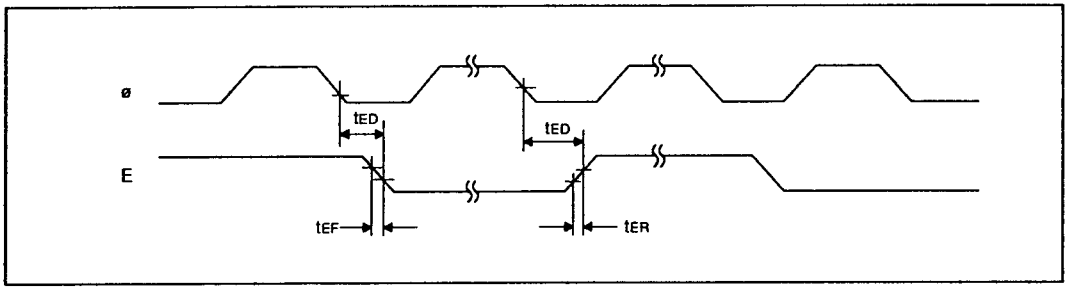

Figure 19-12 E Clock Timing

2. Clock Oscillator Stabilization Timing

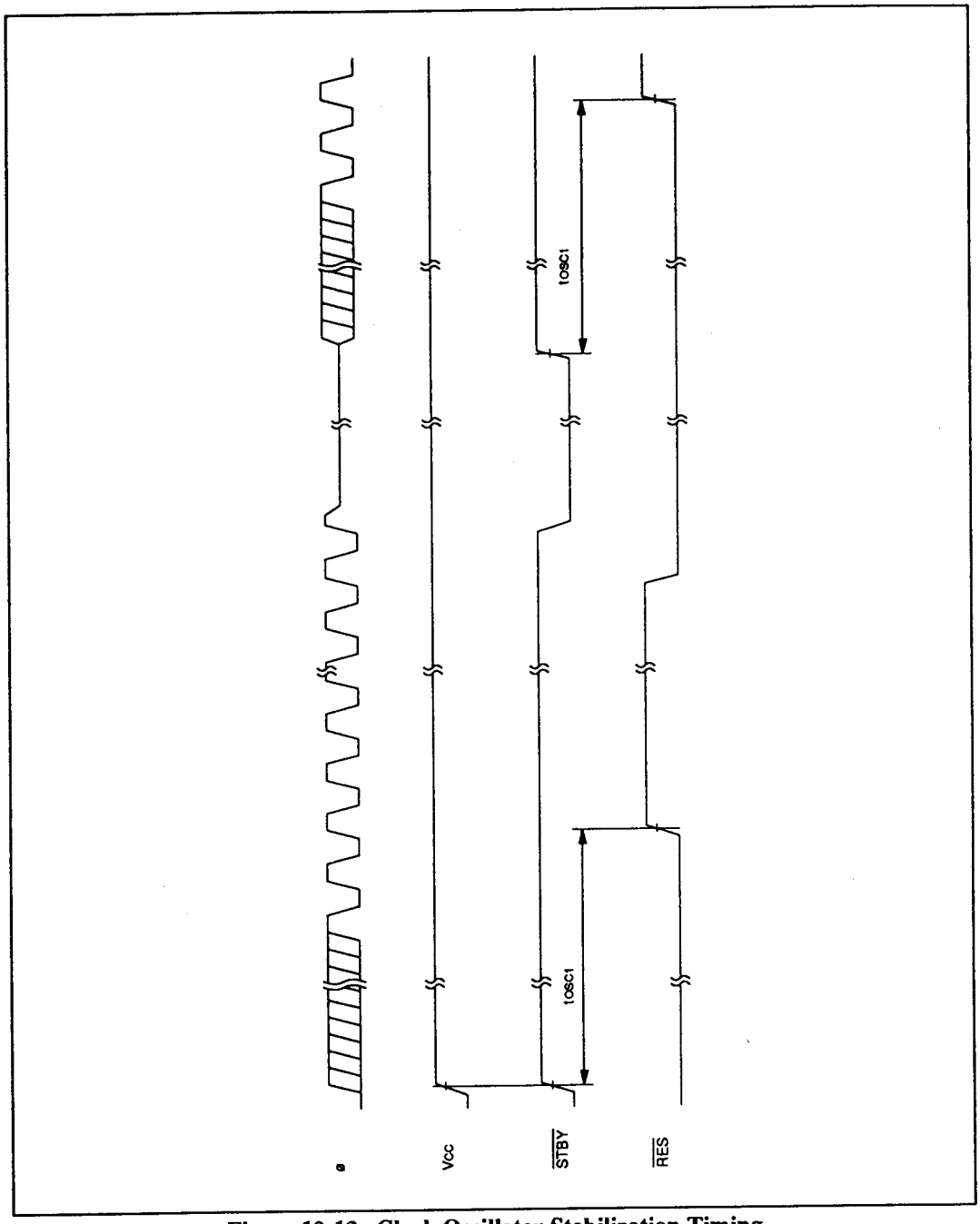

Figure 19-13 Clock Oscillator Stabilization Timing

19.3.4 I/O Port Timing

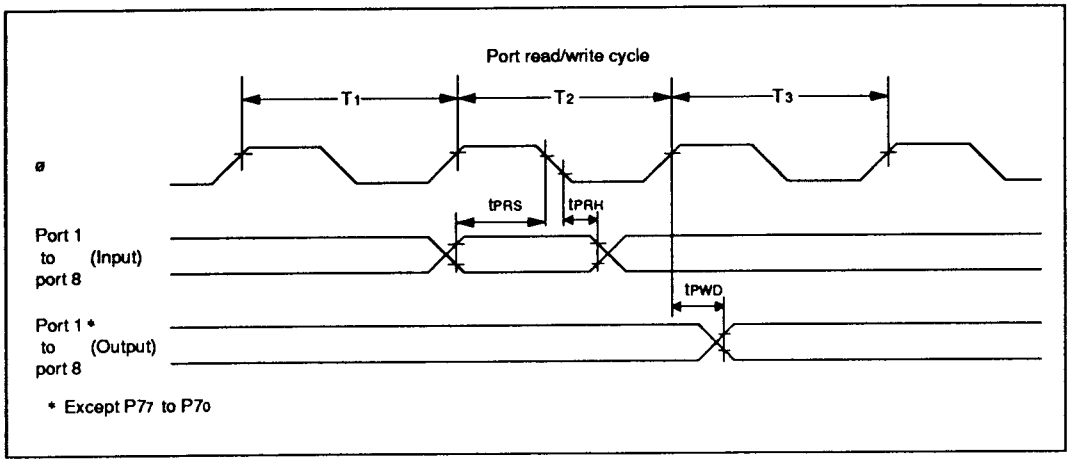

Figure 19-14 I/O Port Input/Output Timing

19.3.5 16-Bit Free-Running Timer Timing

1. Free-Running Timer Input/Output Timing

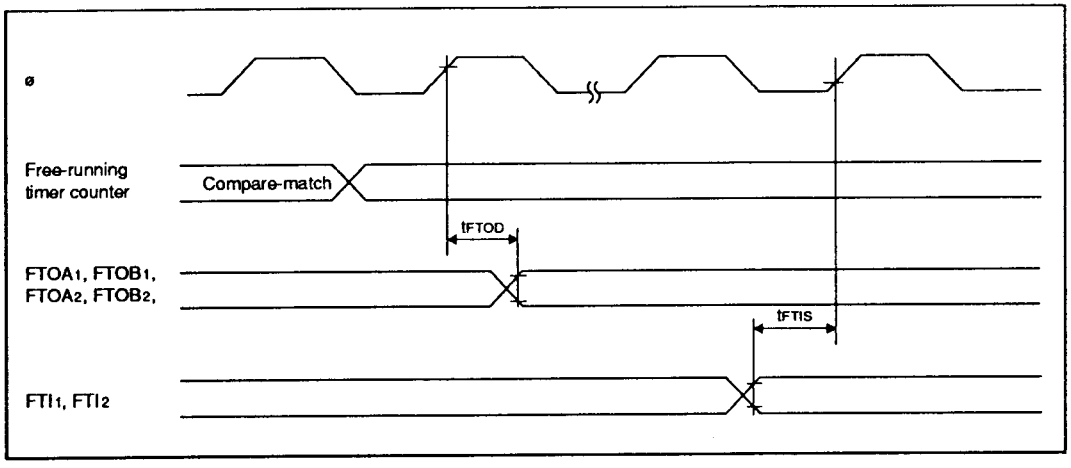

Figure 19-15 Free-Running Timer Input/Output Timing

2. External Clock Input Timing for Free-Running Timers

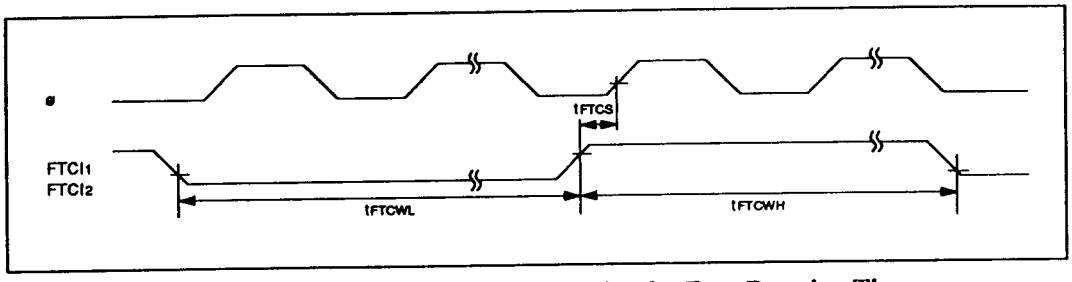

Figure 19-16 External Clock Input Timing for Free-Running Timers

19.3.6 8-Bit Timer Timing

1. 8-Bit Timer Output Timing

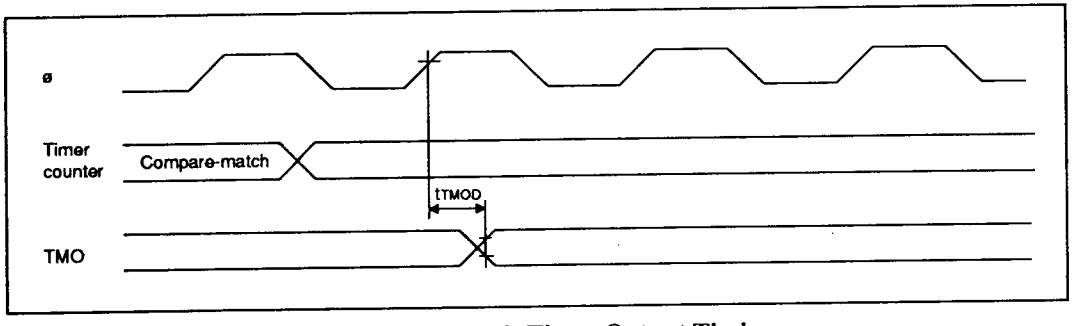

Figure 19-17 8-Bit Timer Output Timing

2. 8-Bit Timer Clock Input Timing

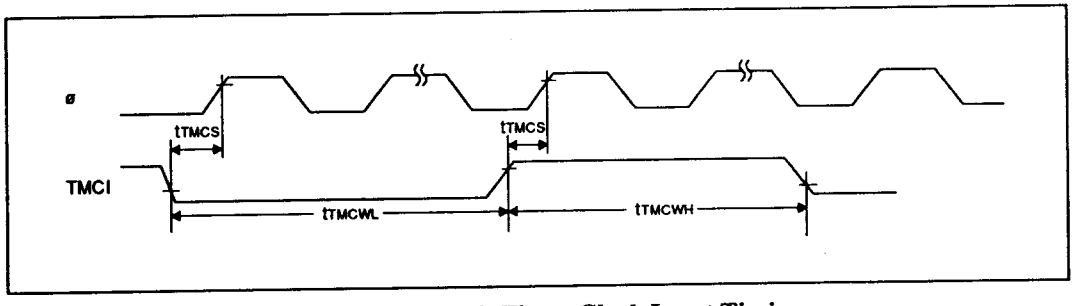

Figure 19-18 8-Bit Timer Clock Input Timing

3. 8-Bit Timer Reset Input Timing

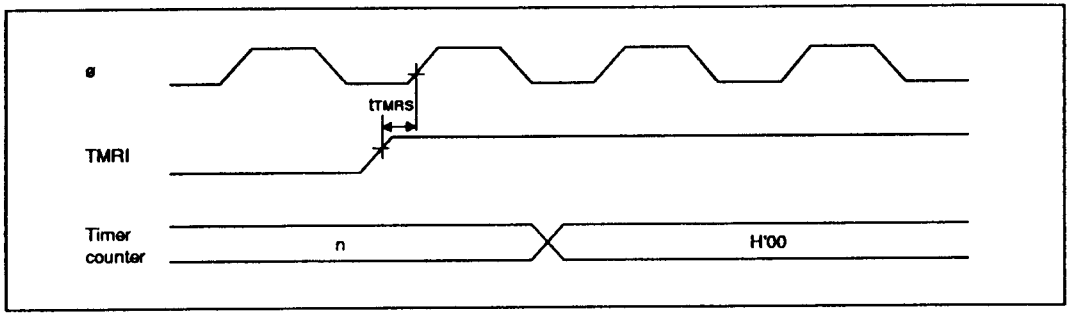

Figure 19-19 8-Bit Timer Reset Input Timing

19.3.7 Serial Communication Interface Timing

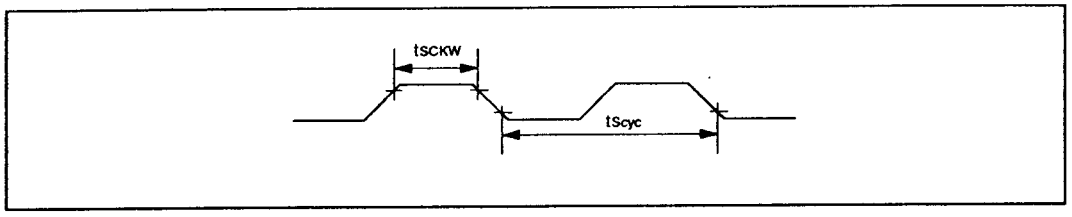

Figure 19-20 SCI Input Clock Timing

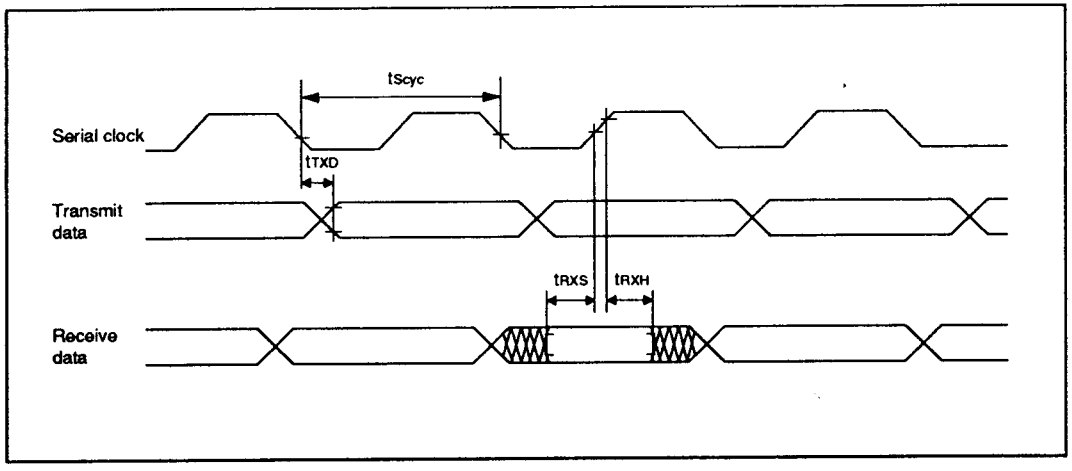

Figure 19-21 SCI Input/Output Timing (Synchronous Mode)

19.3.8 Refresh Timing

1. Basic Refresh Bus Cycle

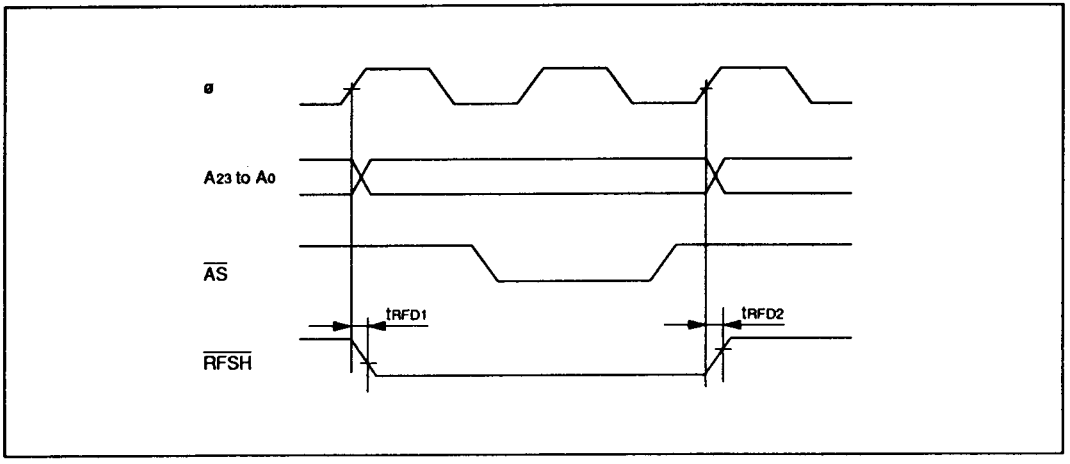

Figure 19-22 Basic Refresh Bus Cycle

2. Refresh Timing (Wait Cycle)

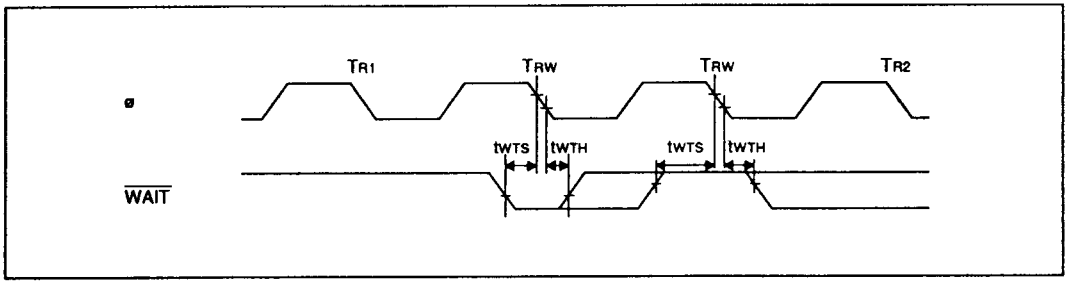

Figure 19-23 Refresh Timing (Wait Cycle)