PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M5278DP,J,FP,VP-20V,-25V

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5278D is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application.These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5278DP,J,FP,VP-20V ..... 20ns(max)
  M5M5278DP,J,FP,VP-25V ..... 25ns(max)
- Low power dissipation Active ..... 132mW(typ)
  Stand-by ..... 330 μW(typ)
- Power down by $\overline{S}$
- Single 3.3V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

APPLICATION

High-speed memory system

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminals is maintained in the high impedance state.

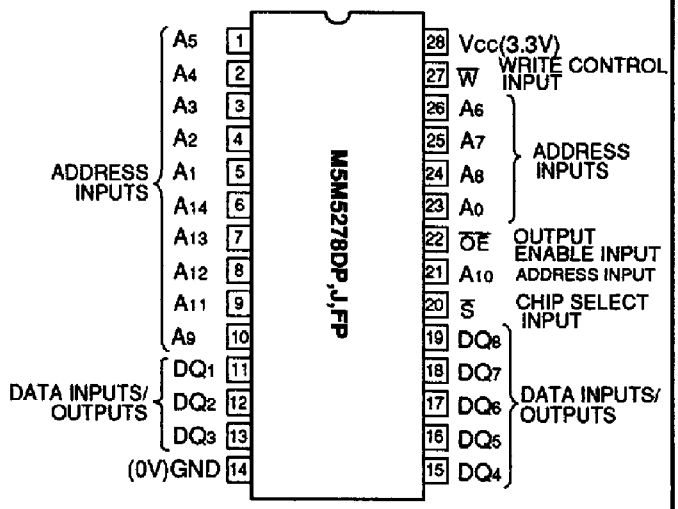
In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low, if the address signals are stable, the data is available at the DQ terminals.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR- ties with other devices.

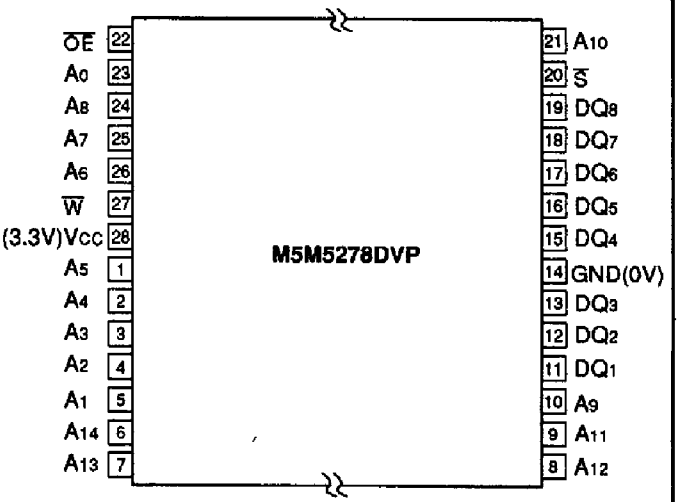
Setting $\overline{OE}$ at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4Y(P)
28P0J(J)
28P2W-C(FP)



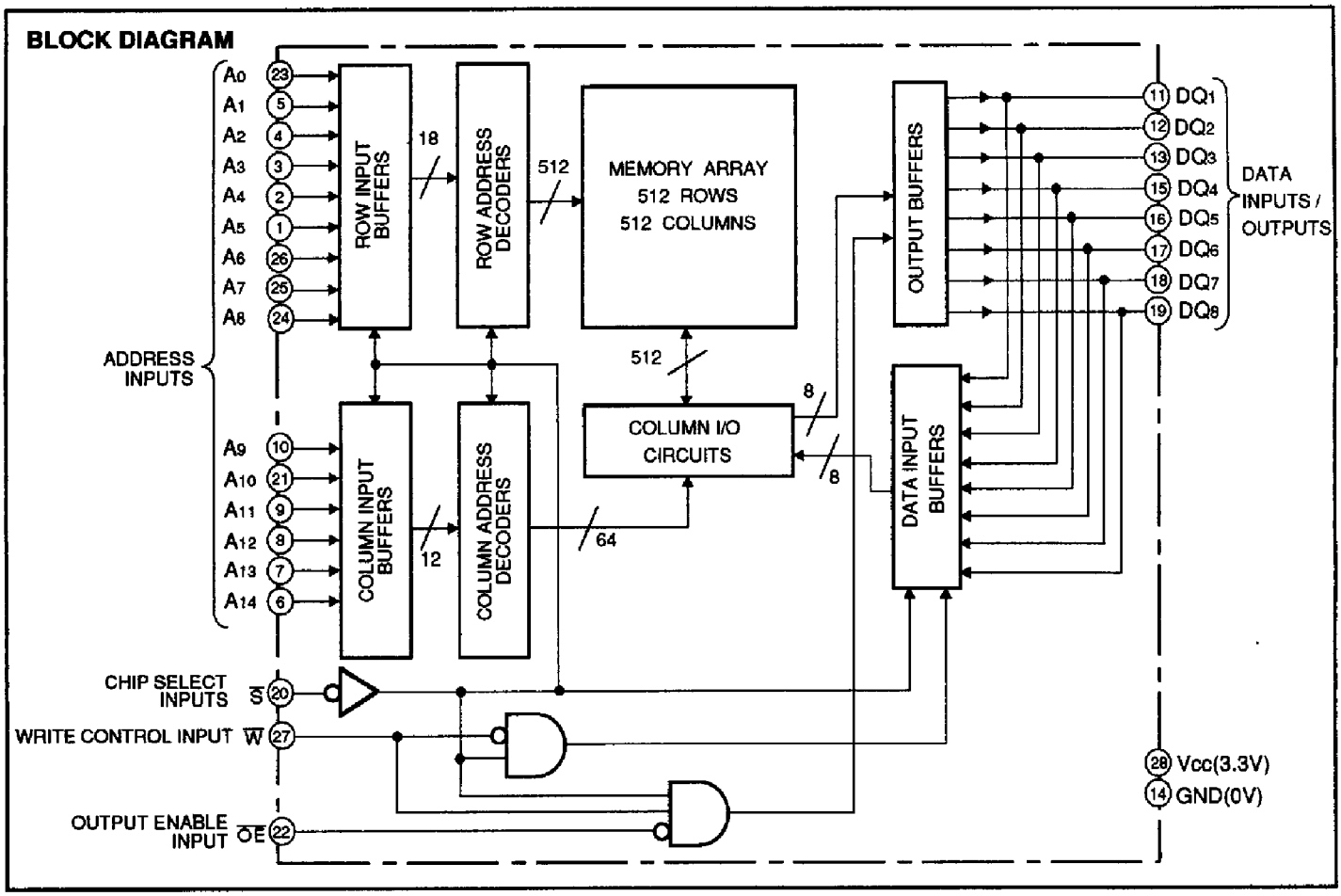
Outline 28P2C-A

MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input /output	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H:VIH L:VIL X:VIH or VIL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0 ~ 70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10 ~ 85	℃
T_{stg}	Storage temperature		− 65 ~ 150	℃

* Pulse width ≦ 10ns, In case of DC: − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=3.3V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High - level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low - level input voltage			−0.3*		0.8	V
V_{OH}	High - level output voltage	I_{OH} = − 4mA		2.4			V
V_{OL}	Low - level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				2	μA
$\|I_{OZ}\|$	Off-state output current	$V_{I(S)} = V_{IH}$, V_O= 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(S)} = V_{IL}$ Output open	AC(20ns cycle)			70	mA
			AC(25ns cycle)			65	
			DC		40	45	
I_{CC2}	Stand-by current	$V_{I(S)} = V_{IH}$	AC(25ns cycle)			20	mA
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			10	
I_{CC3}	Stand-by current	$V_{I(S)}$ = Vcc − 0.2V Other $V_I \leqq$ 0.2V or $V_I \geqq$ Vcc−0.2V				100	μA

Note 1. Current flow into an IC is positive, out is negative.
* − 3.0V in case of AC (Pulse width≦10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I =25mVrms, f=1MHz			5*	pF
C_O	Output capacitance	V_O = GND, V_O=25mVrms, f=1MHz			7*	pF

* C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc=3.3V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ····· V_{OH} = 1.5V, V_{OL} = 1.5V
Output loads ····· Fig1,Fig2

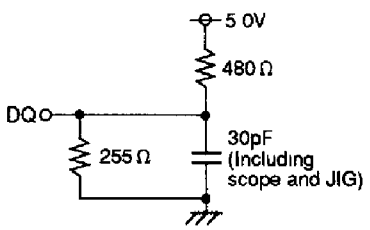


Fig.1 Output load

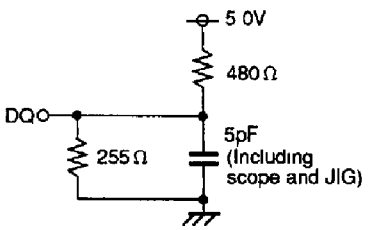


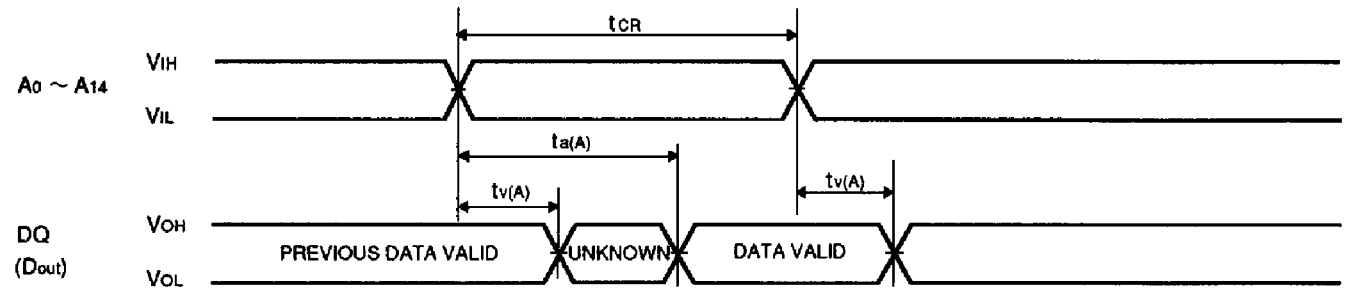
Fig.2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

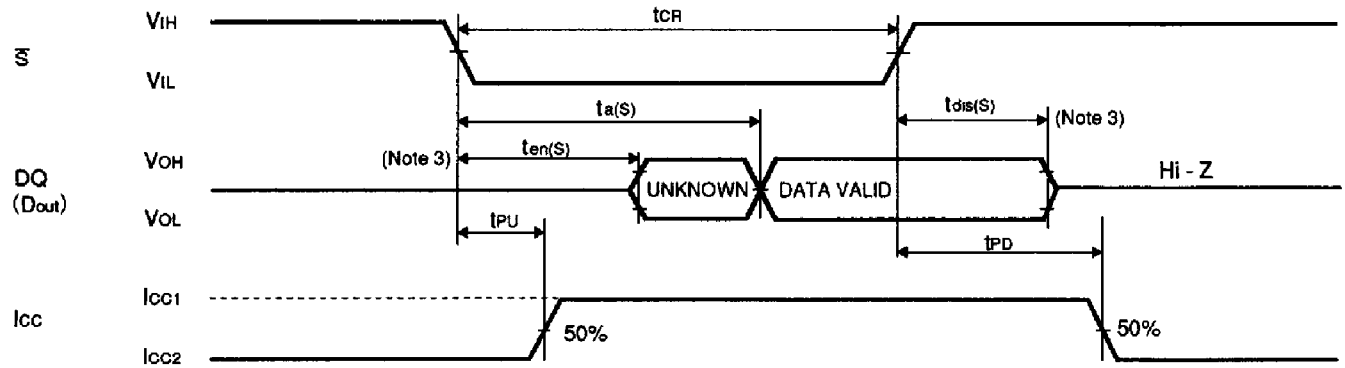
Symbol	Parameter	Limits				Unit
		M5M5278D-20V		M5M5278D-25V		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	20		25		ns
$t_{a(A)}$	Address access time		20		25	ns
$t_{a(S)}$	Chip select access time		20		25	ns
$t_{a(OE)}$	Output enable access time		10		12	ns
$t_{v(A)}$	Data valid time after address change	3		5		ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	3		5		ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	8	0	10	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	8	0	10	ns
t_{PU}	Power-up time after chip selection	0		0		ns
t_{PD}	Power-down time after chip deselection		20		25	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1 <$\overline{W}$=H, $\overline{S}$=L>

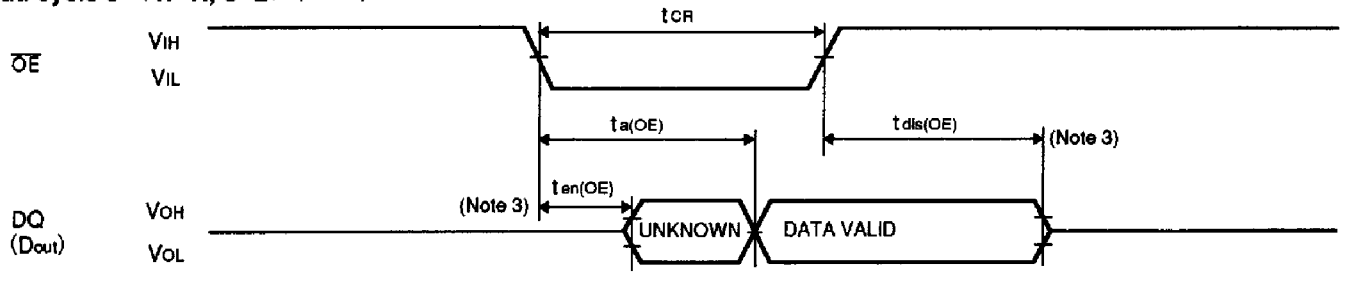


Read cycle 2 <$\overline{W}$=H> (Note 2)



Note 2. Address valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.

Read cycle 3 <$\overline{W}$=H, $\overline{S}$=L> (Note 4)



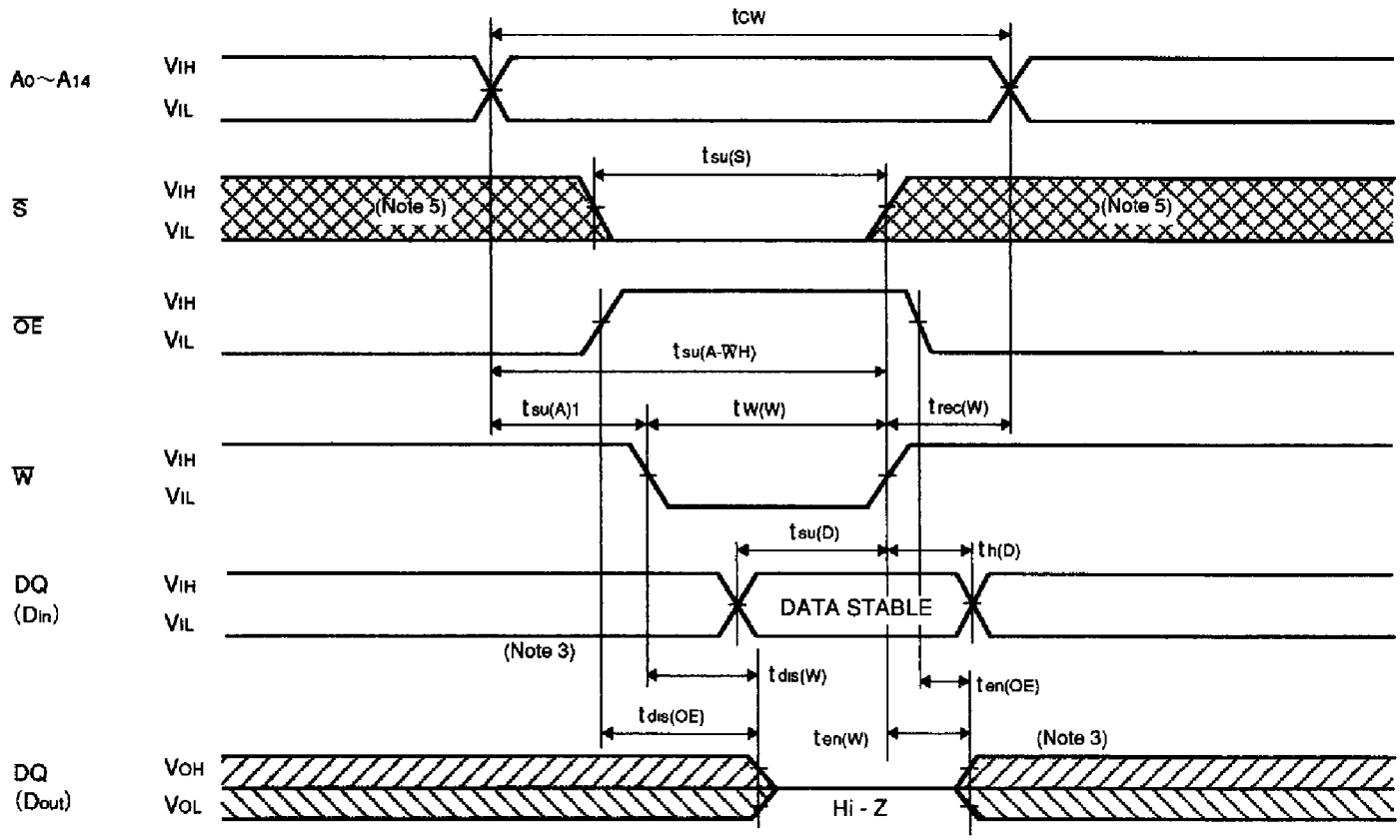
Note 4. Address and $\overline{S}$ valid prior to $\overline{OE}$ transition low by ($t_{a(A)}$ - $t_{a(OE)}$), ($t_{a(S)}$-$t_{a(OE)}$).

(4) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		M5M5278D-20V		M5M5278D-25V		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	20		25		ns
$t_{su(S)}$	Chip select setup time	15		20		ns
$t_{su(A)1}$	Address setup time 1 ($\overline{W}$ CONTROL)	0		0		ns
$t_{su(A)2}$	Address setup time 2 ($\overline{S}$ CONTROL)	0		0		ns
$t_{w(W)}$	Write pulse width	15		20		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{su(D)}$	Data setup time	8		10		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	8	0	10	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		ns
$t_{su(A-WH)}$	Address to $\overline{W}$ high	15		20		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	8	0	10	ns

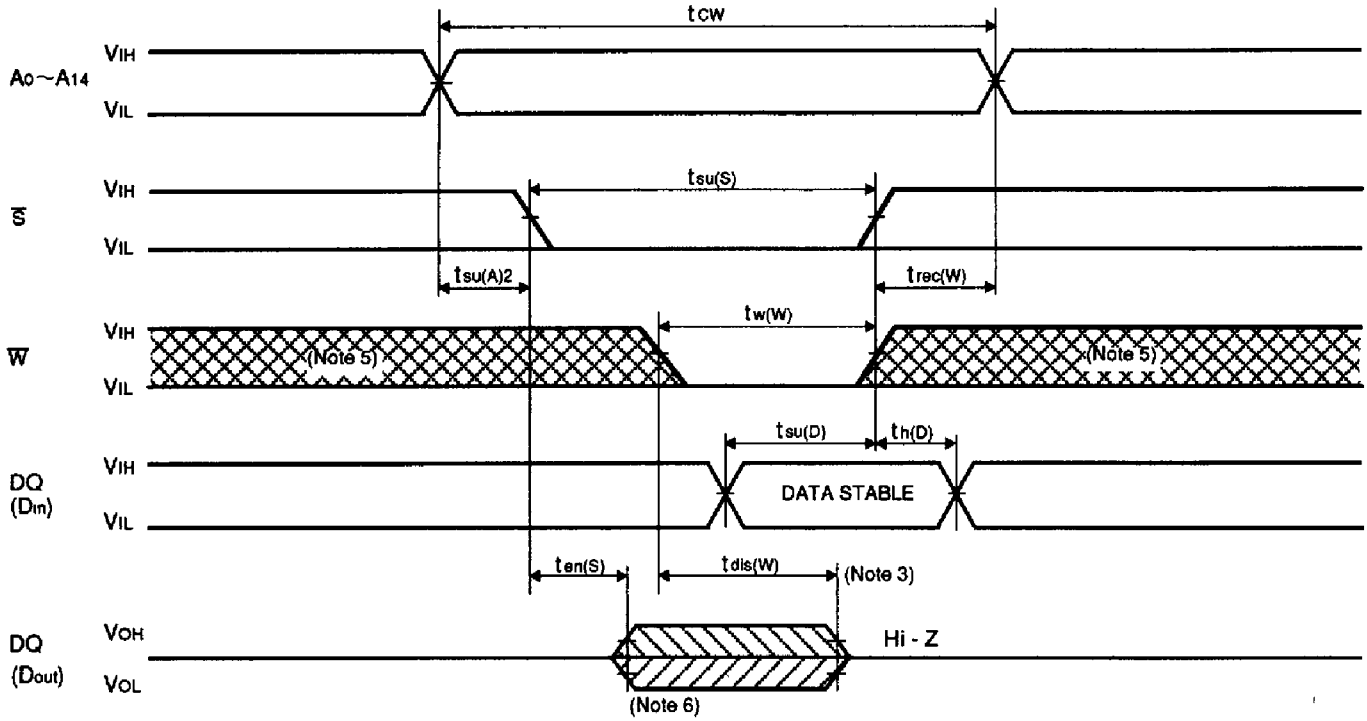
(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Note 5. Hatching indicates the state is don't care.

Write cycle 2 ($\overline{S}$ control mode)



Note 6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.
7. ten,tdis are periodically sampled and are not 100% tested.