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# OKI Semiconductor

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## MR53V1652J

## Preliminary

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1,048,576-Word X 16-Bit or 2,097,152-Word X 8-Bit

8Word X 16-Bit or 16Word X 8-Bit/Page Mode MASK ROM

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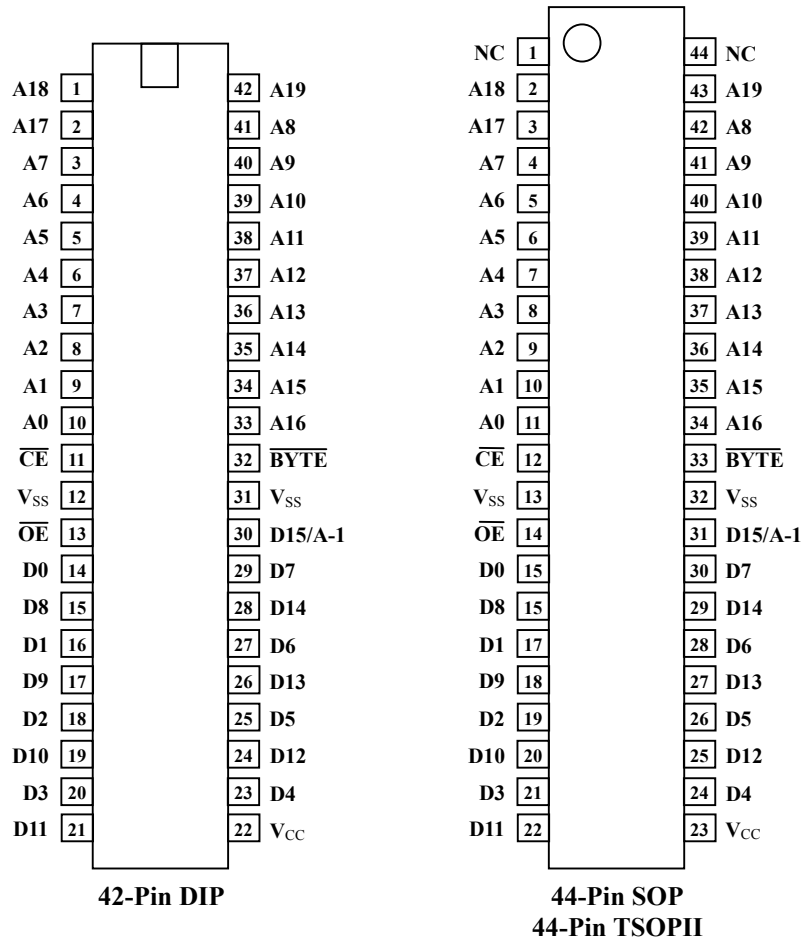
### DESCRIPTION

The MR53V1652J is a 16Mbit Read-Only Memory whose configuration can be electrically switched between 1,048,576 word x 16bit and 2,097,152 word x 8bit. The MR53V1652J operates asynchronously, external clocks are not required, making this device easy-to-use. The MR53V1652J is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS silicon gate technology and is offered in 42-pin DIP, 44-pin SOP or 44-pin TSOP packages.

### FEATURES

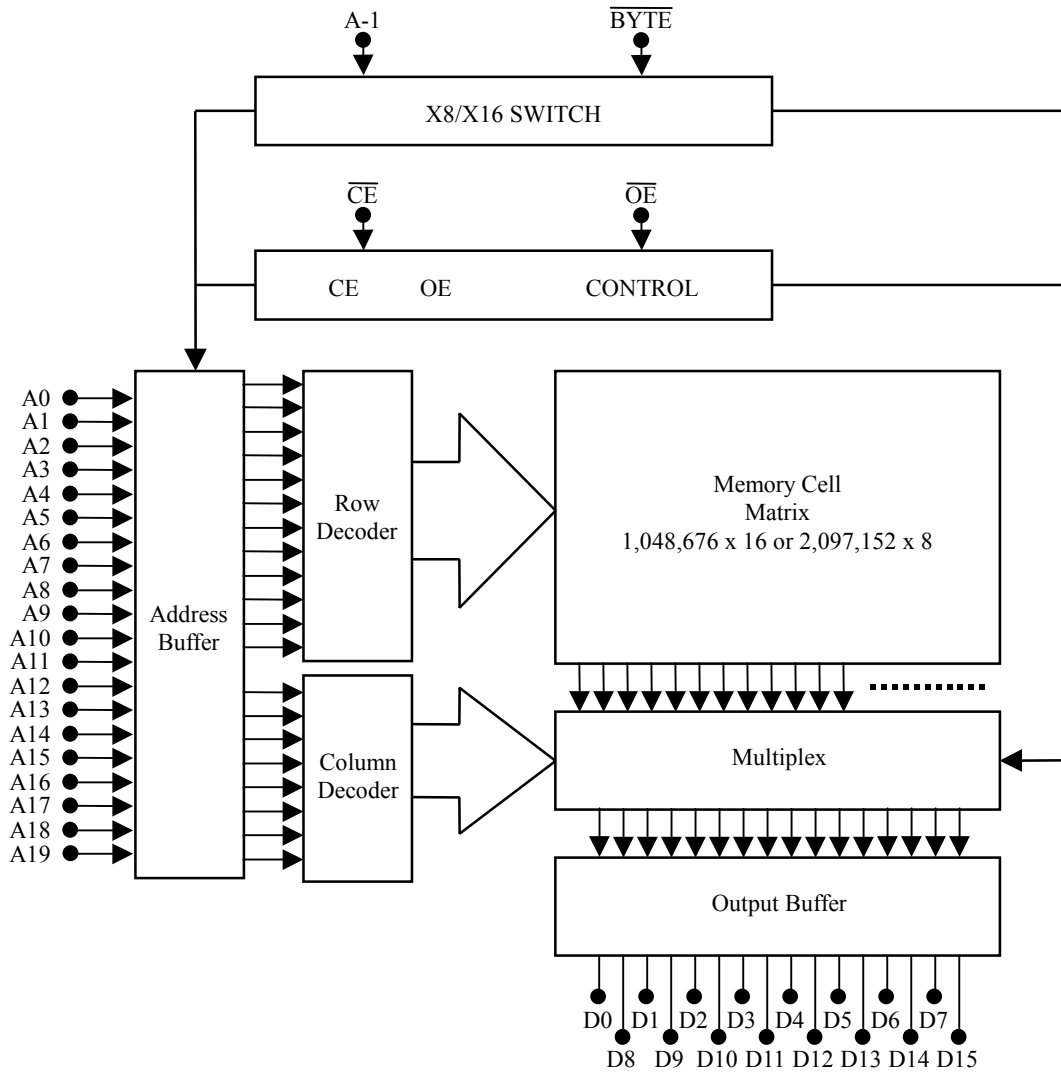
- 1,048,576 word x 16bit / 2,097,152 word x 8bit electrically switchable configuration
- 8word x 16-Bit or 16word x 8-bit / Page read mode
- Single +2.7V~3.6V power supply
- Normal access time            100ns
- Page access time                30ns
- V<sub>CC</sub> power supply current    80mA
- V<sub>CC</sub> standby current          10μA
- Input / Output TTL compatible
- Three-state output
- Packages
  - 42-pin plastic DIP    (DIP42-P-600-2.54)    MR53V1652J-XXRA
  - 44-pin plastic SOP    (SOP44-P-600-1.27-K)   MR53V1652J-XXMA
  - 44-pin plastic TSOP   (TSOP44-P-400-0.80-K) MR53V1652J-XXTP

PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0~A19	Address input
D0~D14	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{BYTE}$	Mode switch
V <sub>CC</sub>	Power supply voltage
V <sub>SS</sub>	GND
NC	Non connection

**BLOCK DIAGRAM**



**FUNCTION TABLE**

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	D0~D7	D8~D14	A-1/D15
STAND BY	H	X	X	Hi-Z	Hi-Z	L/H
OUTPUT DISABLE	L	H	H			
OUTPUT DISABLE	L	H	L			
READ(16-BIT)	L	L	H	$D_{OUT}$		
READ(8-BIT)	L	L	L	$D_{OUT}$	Hi-Z	L/H

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T <sub>OPR</sub>	-	0 ~ 70	°C
Storage temperature	T <sub>STG</sub>	-	-55 ~ 125	°C
Input voltage	V <sub>I</sub>	Relative to V <sub>SS</sub>	-0.5 ~ V <sub>CC</sub> +0.5	V
Output voltage	V <sub>O</sub>		-0.5 ~ V <sub>CC</sub> +0.5	V
Power supply voltage	V <sub>CC</sub>		-0.5 ~ 5	V
Power dissipation per package	P <sub>D</sub>	-	1.0	W

## RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 ~ 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>	V <sub>CC</sub> =2.7V ~ 3.6V	2.7	-	3.6	°C
Input "H" level	V <sub>IH</sub>		2.2	-	V <sub>CC</sub> +0.5	°C
Input "L" level	V <sub>IL</sub>		-0.5	-	0.8	V

Voltage is relative to V<sub>SS</sub>

## PIN Capacitance

(V<sub>CC</sub>=3.3V, Ta=25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input	C <sub>IN</sub>	V <sub>I</sub> =0V	-	-	12	pF
Output	C <sub>OUT</sub>	V <sub>O</sub> =0V	-	-	15	pF

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

(V<sub>CC</sub>=2.7V~3.6V, Ta=0~70°C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input leakage current	C <sub>IN</sub>	V <sub>I</sub> =0V~V <sub>CC</sub>	-	-	10	μA
Output leakage current	C <sub>OUT</sub>	V <sub>O</sub> =0V~V <sub>CC</sub>	-	-	10	μA
V <sub>CC</sub> power supply current (Standby)	I <sub>CCSC</sub>	$\overline{CE}=V_{CC}$	-	-	10	μA
	I <sub>CCST</sub>	$\overline{CE}=V_{IH}$	-	-	1	mA
V <sub>CC</sub> power supply current (Active)	I <sub>CCA</sub>	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc= 100ns	-	-	80	mA
Input "H" level	V <sub>IH</sub>	-	2.0	-	V <sub>CC</sub> +0.5	V
Input "L" level	V <sub>IL</sub>	-	-0.5	-	0.8	V
Output "H" level	V <sub>OH</sub>	I <sub>OH</sub> =-200 μA	V <sub>CC</sub> -0.4	-	-	V
Output "L" level	V <sub>OL</sub>	I <sub>OL</sub> =1mA	-	-	0.4	V

Voltage is relative to V<sub>SS</sub>

**AC Characteristics**

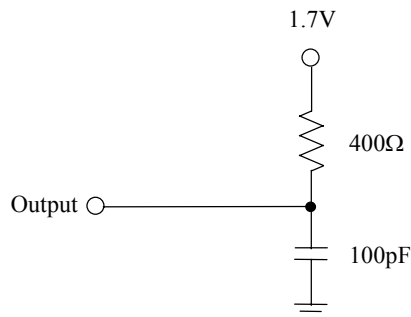
(V<sub>CC</sub>=2.7V~3.6V, Ta=0~70°C)

Parameter	Symbol	Condition	Min.	Min.	Unit
Address access cycle time	T <sub>C</sub>	-	100	-	ns
Address access time	T <sub>ACC</sub>	$\overline{CE}=\overline{OE}=V_{IL}$	-	100	ns
Page set up time	T <sub>PSET</sub>	NOTE.1	100	-	ns
Page access cycle time	T <sub>PC</sub>	-	30	-	ns
Page access time	T <sub>PAC</sub>	-	-	30	ns
$\overline{CE}$ access time	T <sub>CE</sub>	$\overline{OE}=V_{IL}$	-	100	ns
$\overline{OE}$ access time	T <sub>OE</sub>	$\overline{CE}=V_{IL}$	-	30	ns
Output disable time	T <sub>CHZ</sub>	$\overline{OE}=V_{IL}$	0	30	ns
	T <sub>OHZ</sub>	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T <sub>OH</sub>	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

NOTE.1 T<sub>PSET</sub> is defined as the end of either  $\overline{CE}$  falling edge or address transition in random access term until the first page address transition.

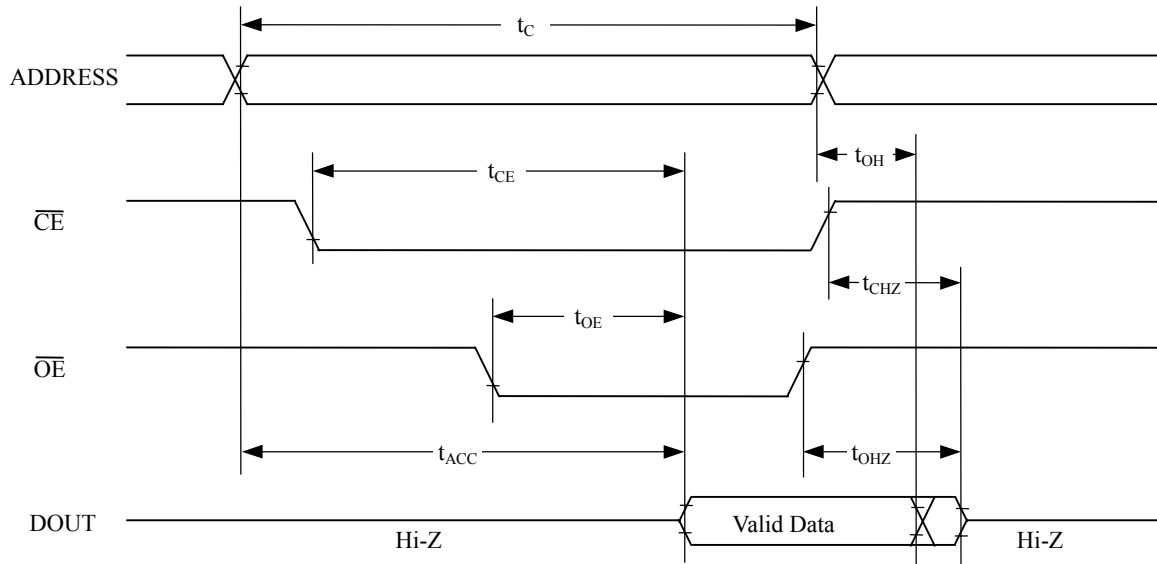
Measurement condition

- Input signal level                    0V/3V
- Input timing reference level        0.8V/2.0V
- Output load                            100pF
- Output timing reference level       0.8V/2.0V

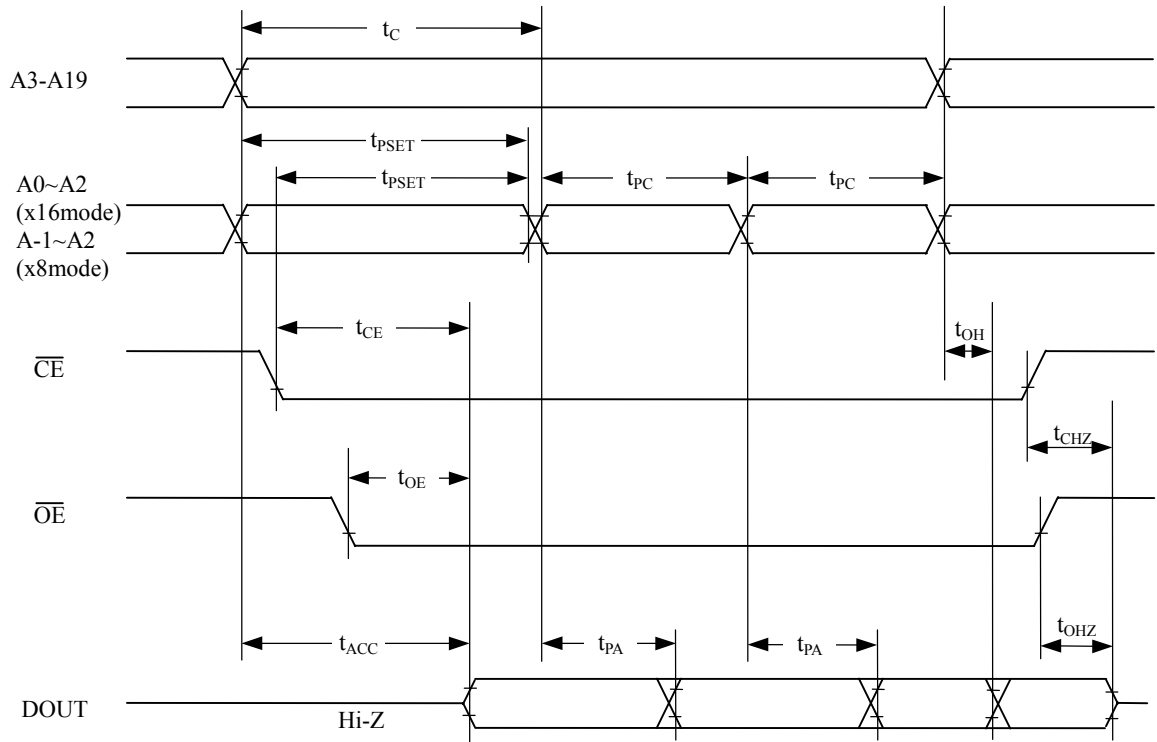


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



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