

1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x16 bit Extended Data Out CMOS DRAMs. Dxtended Data Out mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-45, -5, -6 or -7), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 1Mx16 Extended Data Out mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

FEATURES

• Part Identification

- KM416C1004B/B-L (5V, 4K Ref.)
- KM416C1204B/B-L (5V, 1K Ref.)
- KM416V1004B/B-L (3.3V, 4K Ref.)
- KM416V1204B/B-L (3.3V, 1K Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-45	-	-	660	935
-5	396	576	605	880
-6	360	540	550	825
-7	324	504	495	770

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

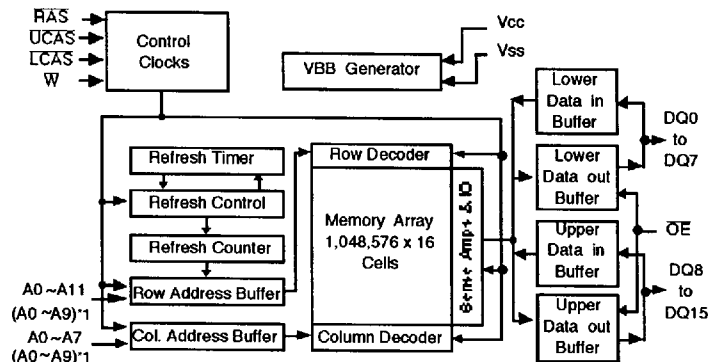
• Refresh cycles

Part NO	Vcc	Refresh cycle	Refresh period	
			Normal	L-ver
C1004B	5V	4K	64ms	128ms
V1004B	3.3V	4K	64ms	
C1204B	5V	1K	16ms	128ms
V1204B	3.3V	1K	16ms	

• Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-45	45ns	14ns	79ns	18ns	5V only
-5	50ns	15ns	84ns	20ns	5V/3.3V
-6	60ns	17ns	114ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V

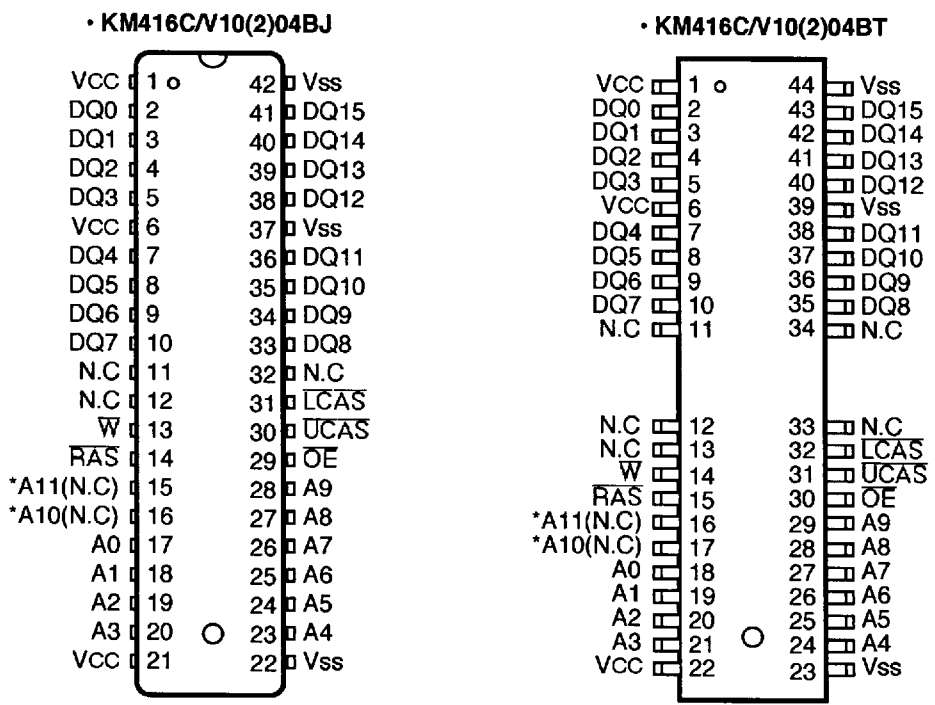
FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 1K Refresh

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PIN CONFIGURATION (Top Views)



* A10 and A11 are N.C for KM416C/V1204B (5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 -15	Data In/Out
V _{ss}	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
V _{cc}	Power (+5.0V) Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	2.4	-	V _{CC} +1 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.3V, all other pins not under test=0 volt.)	I _{I(L)}	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	- 5	5	μA
	Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{CC} +0.5V, all other pins not under test=0 volt.)	I _{I(L)}	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	- 5	5	μA
	Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1004B	KM416V1204B	KM416C1004B	KM416C1204B	
I _{CC1}	Don't care	-45	-	-	120	170	mA
		-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I _{CC2}	Normal L	Don't care	2	2	2	2	mA
			1	1	1	1	mA
I _{CC3}	Don't care	-45	-	-	120	170	mA
		-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I _{CC4}	Don't care	-45	-	-	130	130	mA
		-5	120	120	120	120	mA
		-6	110	110	110	110	mA
		-7	100	100	100	100	mA
I _{CC5}	Normal L	Don't care	1	1	1	1	mA
			200	200	200	200	μA
I _{CC6}	Don't care	-45	-	-	120	170	mA
		-5	110	160	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
I _{CC7}	L	Don't care	400	300	450	350	μA
I _{CC8}	L	Don't care	200	200	250	250	μA

I_{CC1}* : Operating Current (\overline{RAS} , \overline{UCAS} , \overline{LCAS} , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} -Only Refresh Current ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, \overline{RAS} , Address cycling @t_{RC}=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -before- \overline{RAS} Refresh Current (\overline{RAS} , \overline{UCAS} or \overline{LCAS} cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, \overline{UCAS} , \overline{LCAS} =0.2V,

Din = Don't care, T_{RC}= 31.25μs(4K/L-ver), 125μs(1K/L-ver), T_{RAS}=T_{RASmin}~300ns

I_{CC8} : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0 \sim A11 = V_{CC}-0.2V$ or 0.2V,

DQ0 ~ DQ15= V_{CC}-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, t_{HPC}.

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$ or 3.3V , $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DO}	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, See note 1,2)

Test condition (5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Test condition (3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.2/0.7\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	-45*1		-5		0		+7		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	79		84		104		124		ns	
Read-modify-write cycle time	tRWC	105		115		140		170		ns	
Access time from $\overline{\text{RAS}}$	tRAC		45		50		60		70	ns	3,4,9
Access time from $\overline{\text{CAS}}$	tCAC		14		15		17		20	ns	3,4
Access time from column address	tAA		23		25		30		35	ns	3,9
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	3	15	3	20	ns	5,12
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		30		40		50		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	45	10K	50	10K	60	10K	70	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		13		17		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	36		40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	7	10K	8	10K	10	10K	15	10K	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	19	31	20	35	20	43	20	50	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	14	22	15	25	15	30	15	35	ns	9
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	9		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	13
Column address hold time	tCAH	7		8		10		15		ns	13
Column address to $\overline{\text{RAS}}$ lead time	tRAL	23		25		30		35		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	8		10		10		15		ns	
Write command pulse width	tWP	8		10		10		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	10		13		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	7		8		10		15		ns	16

Note) *1 : 5V only

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, See note 1,2)

Test condition (5V device) : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{IH}/V_{IL}=2.4/0.8\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Test condition (3.3V device) : $V_{CC}=3.3\text{V} \pm 0.3\text{V}$, $V_{IH}/V_{IL}=2.2/0.7\text{V}$, $V_{OH}/V_{OL}=2.0/0.8\text{V}$

Parameter	Symbol	-45		-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8, 19
Data hold time	tDH	7		8		10		15		ns	8, 19
Refresh period (1K, Normal)	tREF		16		16		16		16	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
CAS to \bar{W} delay time	tCWD	28		32		36		44		ns	6, 15
RAS to \bar{W} delay time	tRWd	59		67		79		94		ns	6
Column address to \bar{W} delay time	tAWd	37		42		49		59		ns	6
CAS precharge to \bar{W} delay time	tCPWd	39		47		54		64		ns	6
CAS set-up time (CAS-before-RAS refresh)	tCSR	5		5		5		5		ns	17
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		15		ns	18
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time(CBR counter test cycle)	tCPT	20		20		20		25		ns	
Access time from CAS precharge	tCPA		25		28		35		40	ns	3
Hyper Page cycle time	tHPC	18		20		25		30		ns	10
Hyper Page read-modify-write cycle time	tHPRWC	39		47		56		71		ns	10
CAS precharge time (Hyper page cycle)	tCP	7		8		10		10		ns	14
RAS pulse width (Hyper page cycle)	tRASP	45	200K	50	200K	60	200K	70	200K	ns	
RAS hold time from CAS precharge	tRHCP	27		30		35		40		ns	
OE access time	tOEA		13		13		15		20	ns	3
OE to data delay	tOED	10		13		15		20		ns	
Output buffer turn off delay time from OE	tOEZ	3	13	3	13	3	15	3	20	ns	6
OE command hold time	tOEH	10		13		15		20		ns	
Output data hold time	tDOH	4		5		5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	13	3	13	3	15	3	20	ns	5, 12
Output buffer turn off delay from \bar{W}	tWEZ	3	13	3	13	3	15	3	20	ns	5
\bar{W} to data delay	tWED	15		15		15		20		ns	
OE to CAS hold time	tOCH	5		5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		5		ns	
OE precharge time	tOEP	5		5		5		5		ns	
\bar{W} pulth width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
RAS pulse width (C-B-R self refresh)	tRASS	100		100		100		100		us	11
RAS precharge time (C-B-R self refresh)	tRPS	79		90		110		130		ns	11
CAS hold time (C-B-R self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1 : 5V only

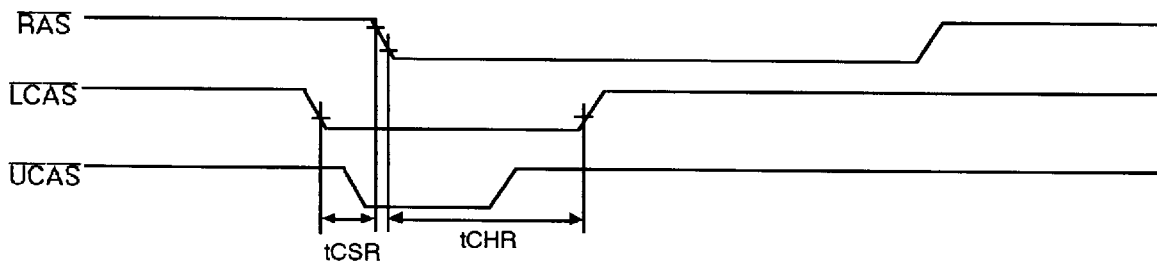
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH} and V_{IL} , and $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
6. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-modify-write cycles.
9. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

KM416C/V10(2)04B/B-L Truth Table

RAS	LCAS	UCAS	W	OE	DQ0 - DQ7	DQ8 - DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

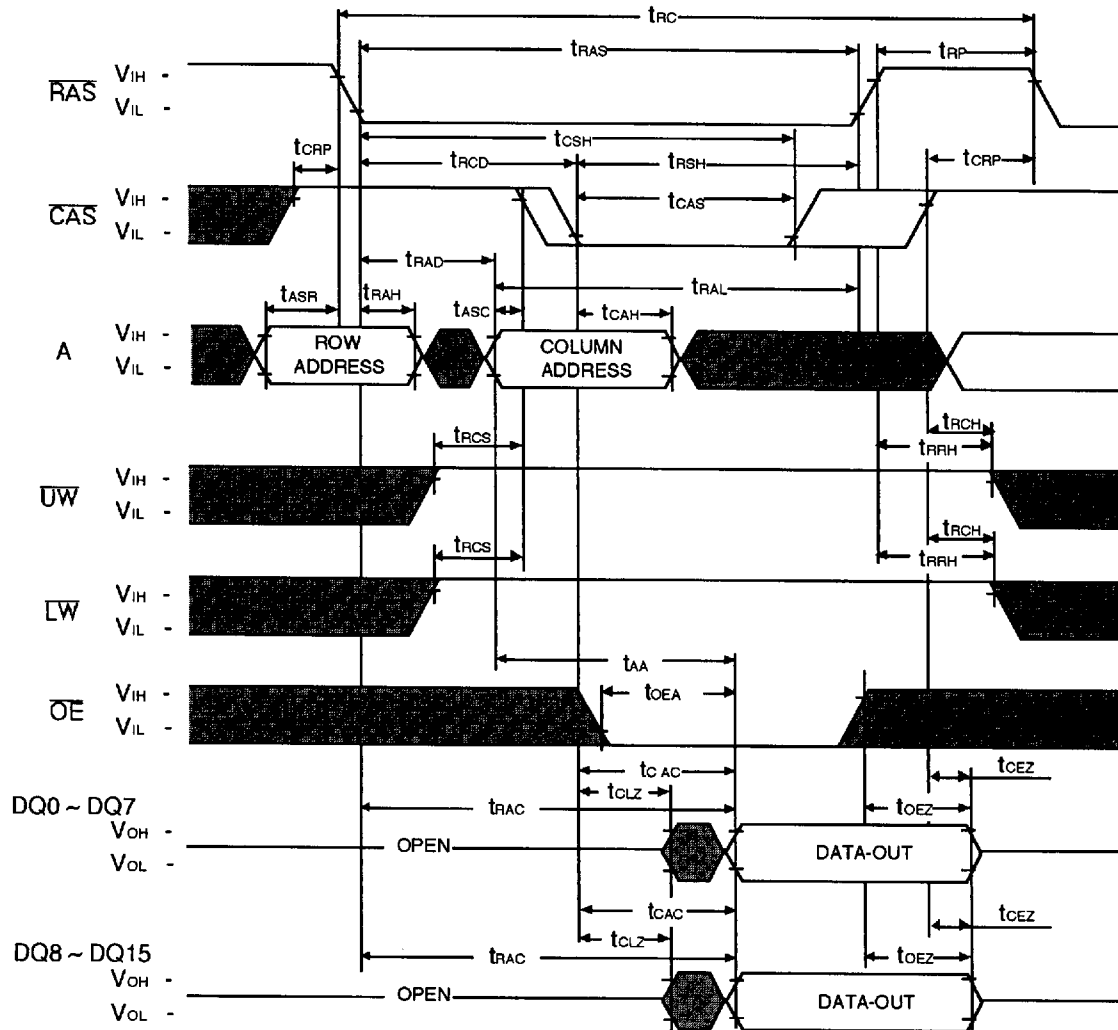
10. $t_{ASC} \geq 6$ ns, Assume $t_T = 2.0$ ns. If $t_{ASC} \leq 6$ ns, then $t_{HPC}(\min)$ and $t_{CAS}(\min)$ must be increased by the value of '6ns - t_{ASC} '.
11. 4096(4K Ref.)/1024(1K Ref.) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification(L-version).
12. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
13. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
14. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
15. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
17. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
18. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.



19. t_{DS} , t_{DH} is independently specified for lower byte $D_{IN}(0\sim7)$, upper byte $D_{IN}(8\sim15)$.

TIMING DIAGRAM
READ CYCLE

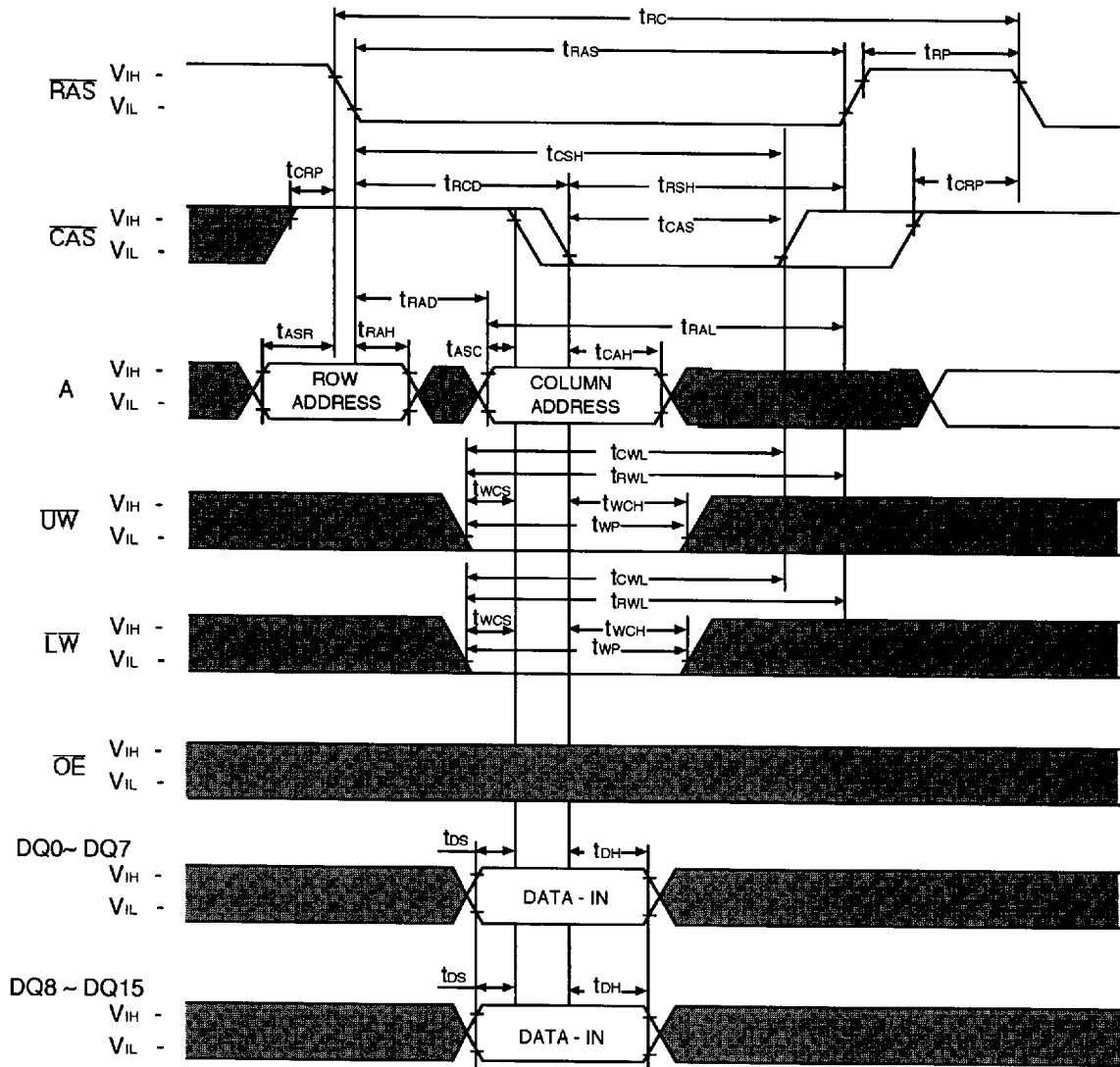
NOTE : D_{IN} = OPEN



■ Don't Care

WRITE CYCLE (EARLY WRITE)

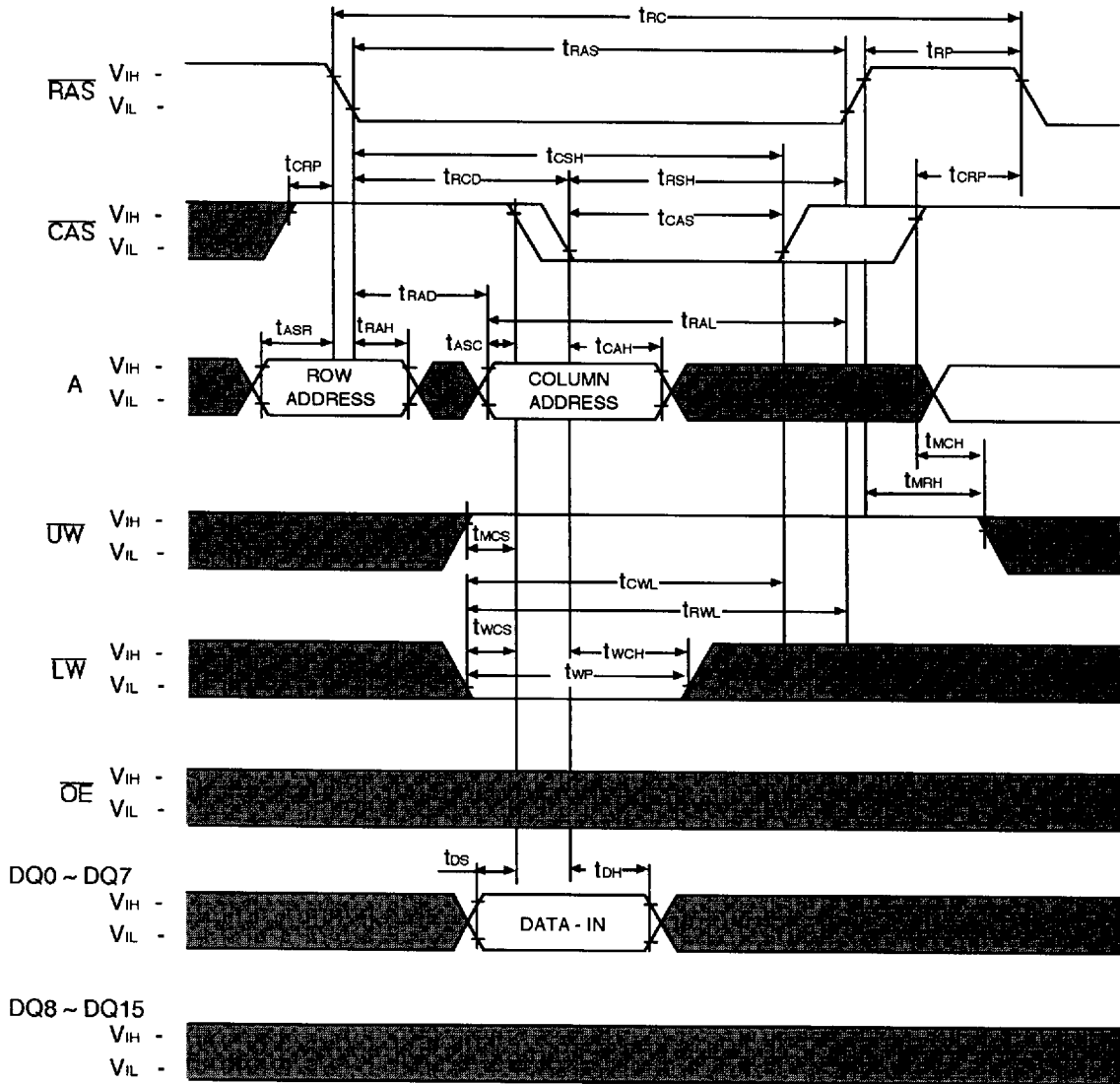
NOTE : D_{OUT} = OPEN



 Don't Care

LOWER BYTE WRITE CYCLE (EARLY WRITE)

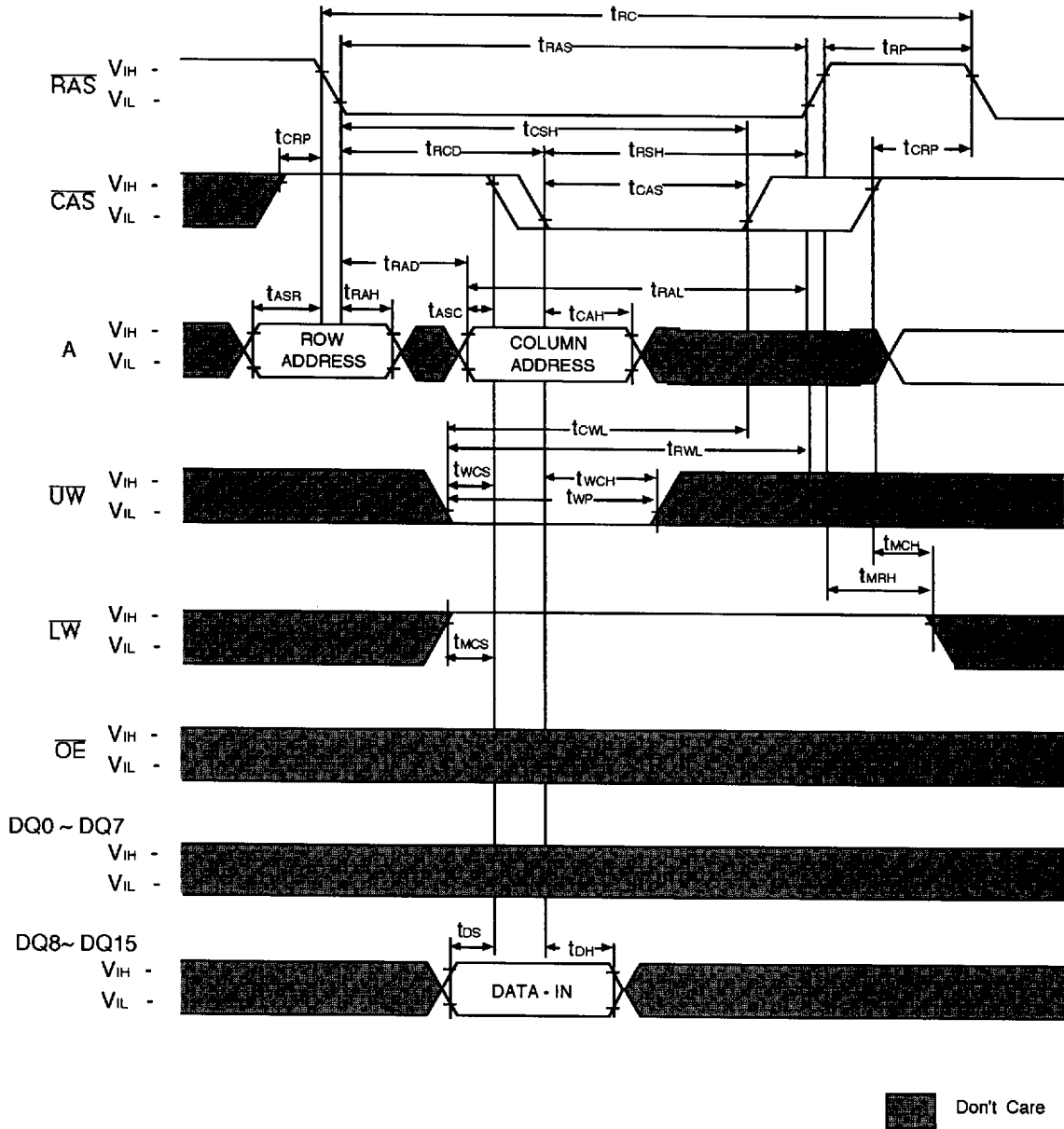
NOTE : D_{OUT} = OPEN



 Don't Care

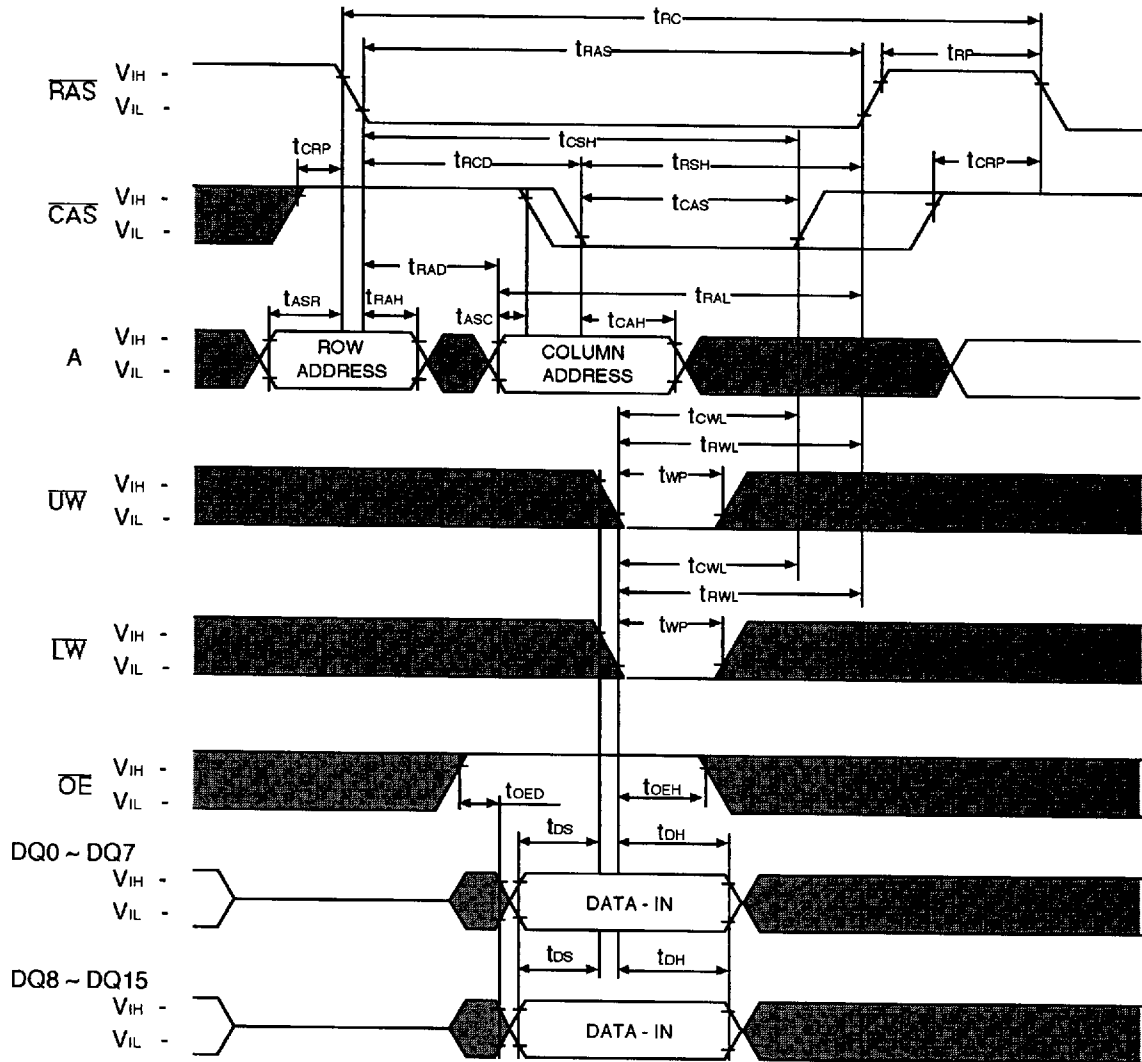
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



WRITE CYCLE (OE CONTROLLED WRITE)

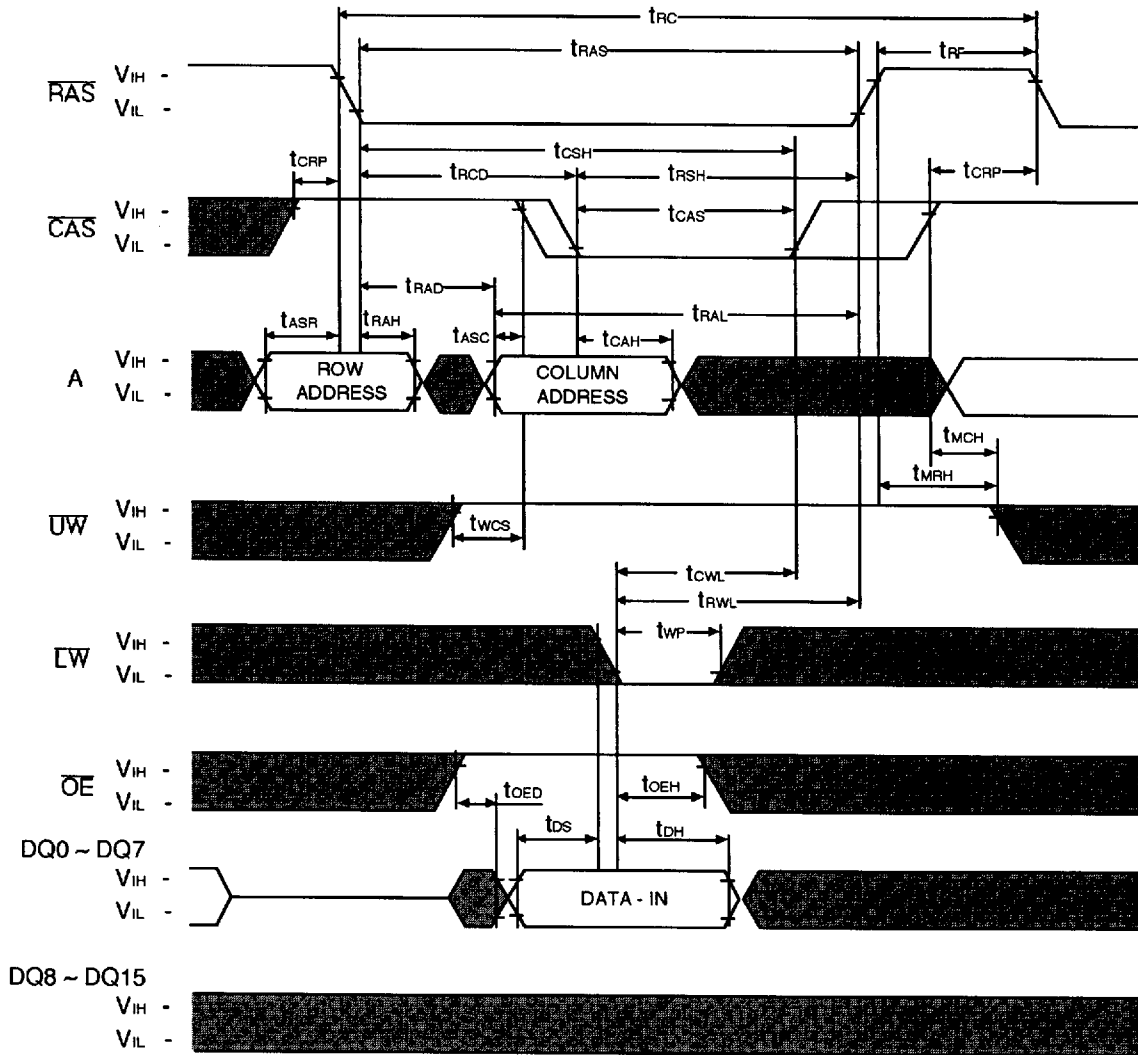
NOTE : D_{OUT} = OPEN



■ Don't Care

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

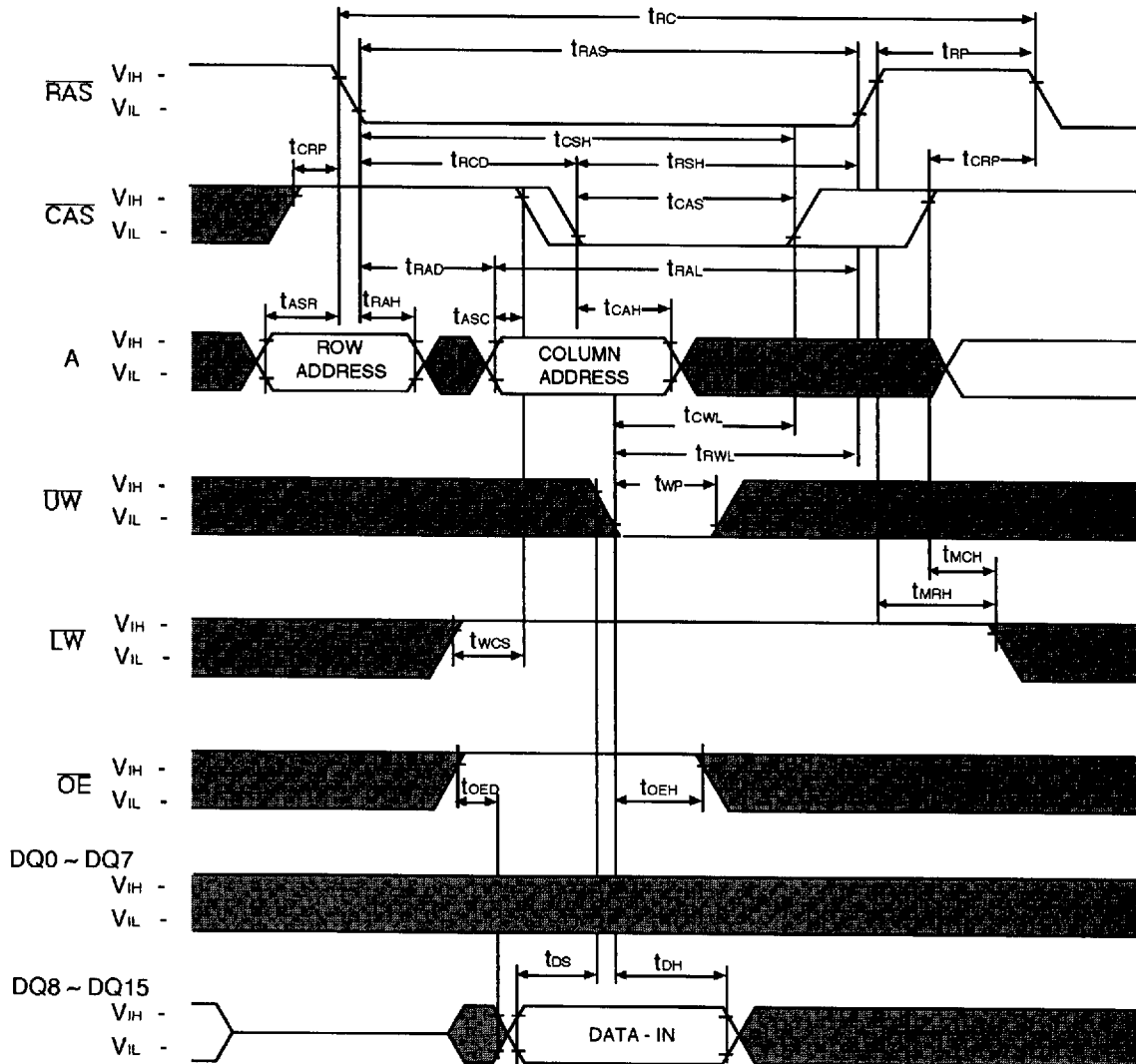
NOTE : D_{OUT} = OPEN



■ Don't Care

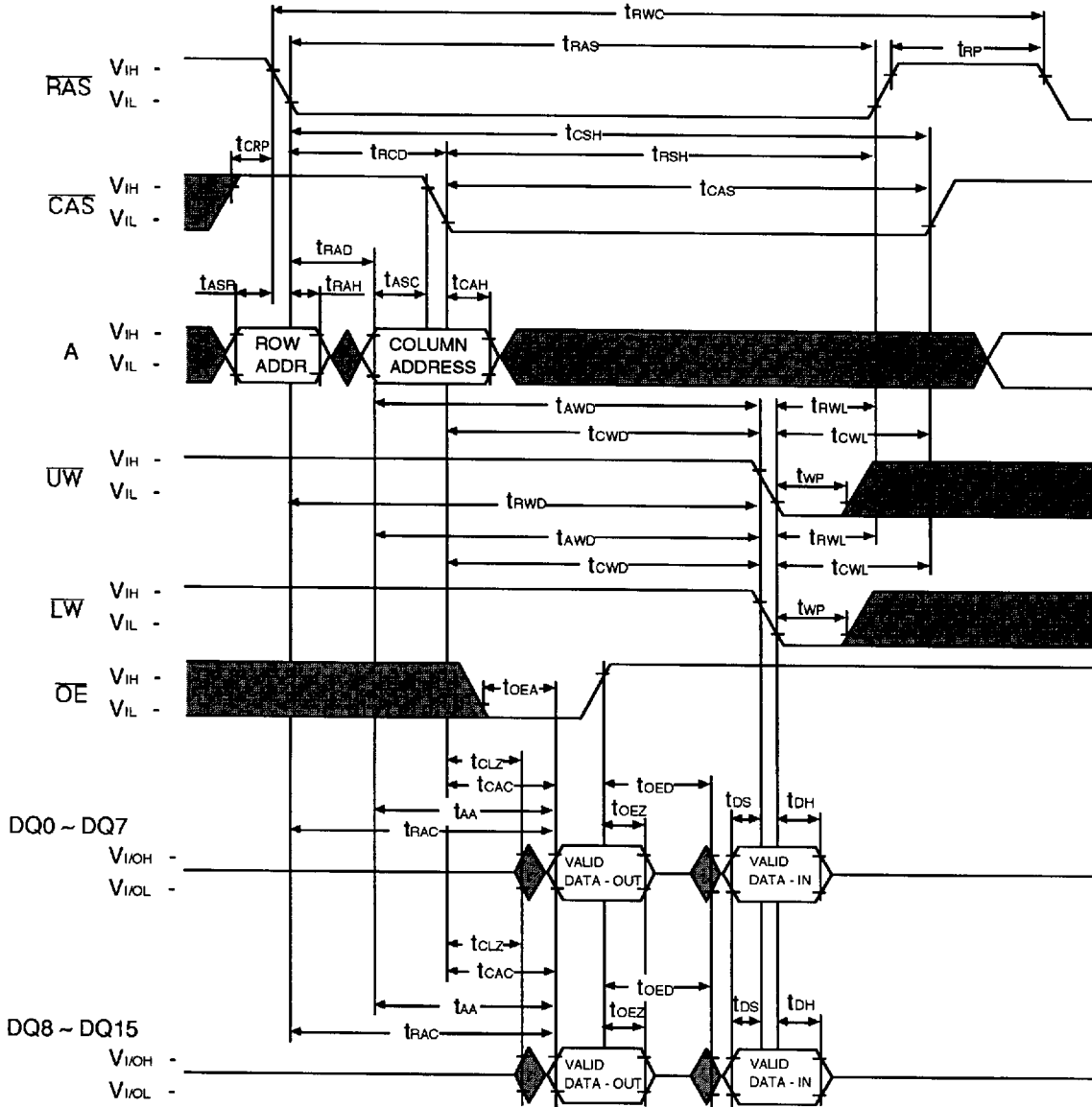
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



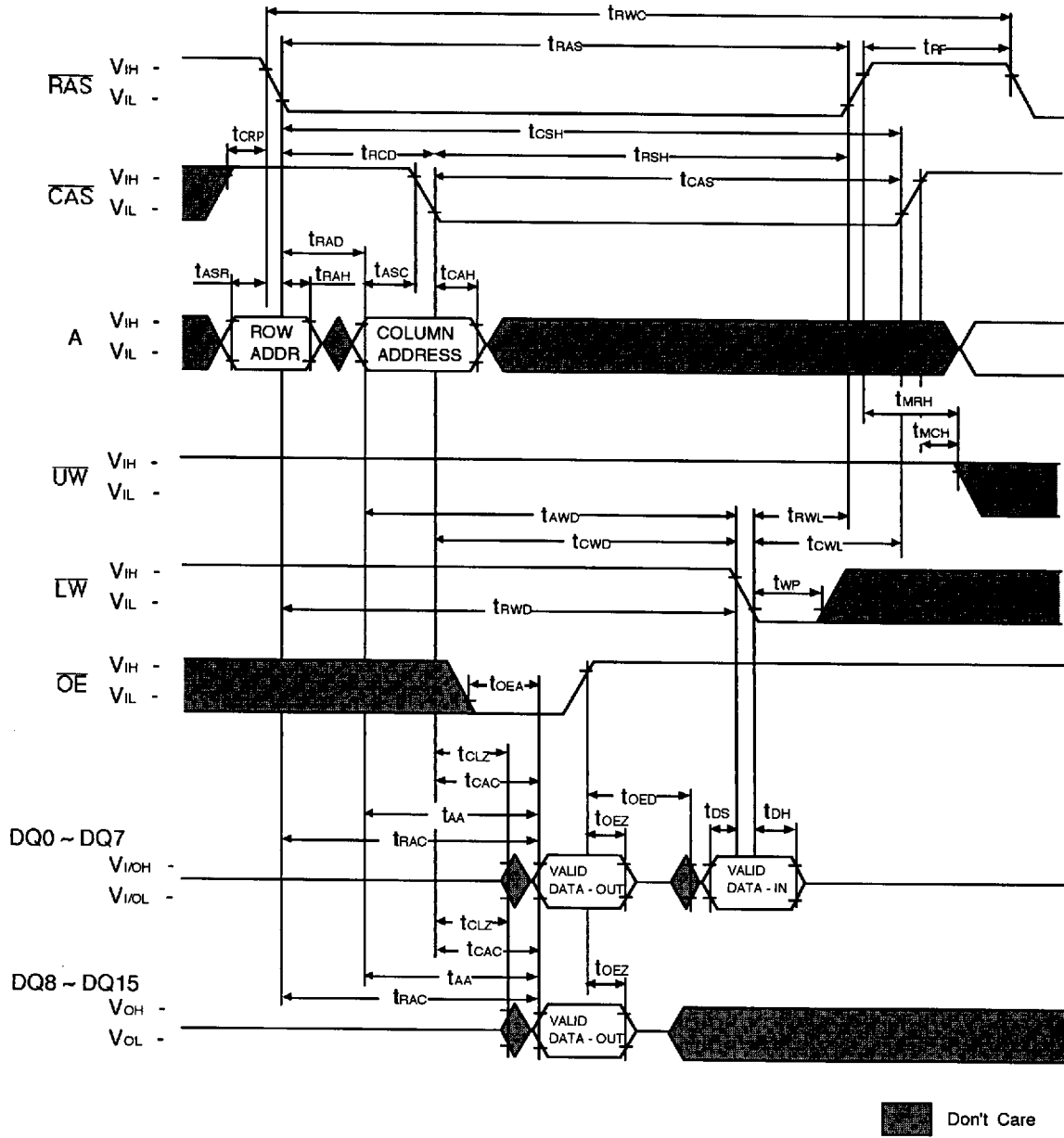
■ Don't Care

WORD READ - MODIFY - WRITE CYCLE

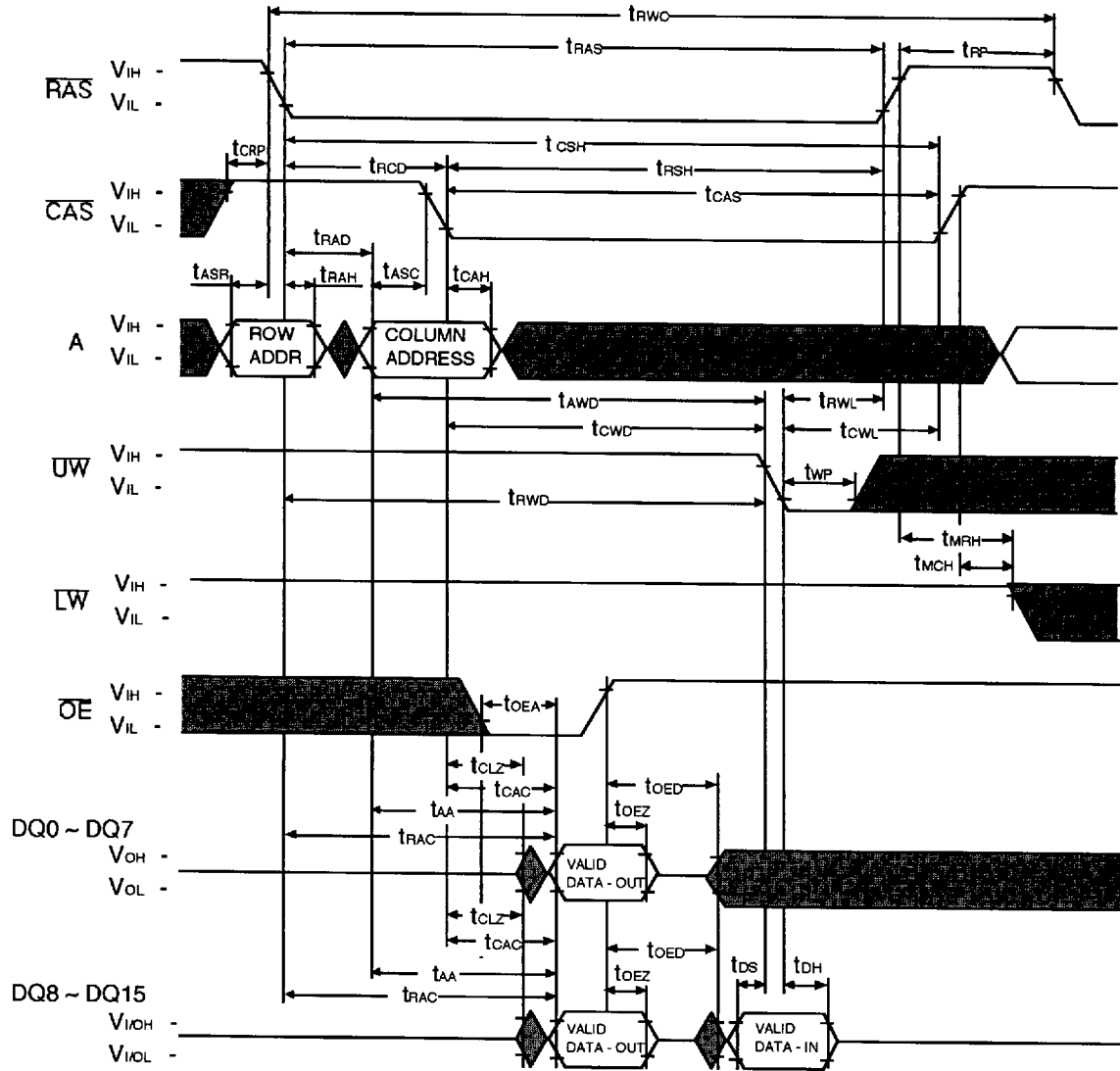


■ Don't Care

LOWER-BYTE READ - MODIFY - WRITE CYCLE

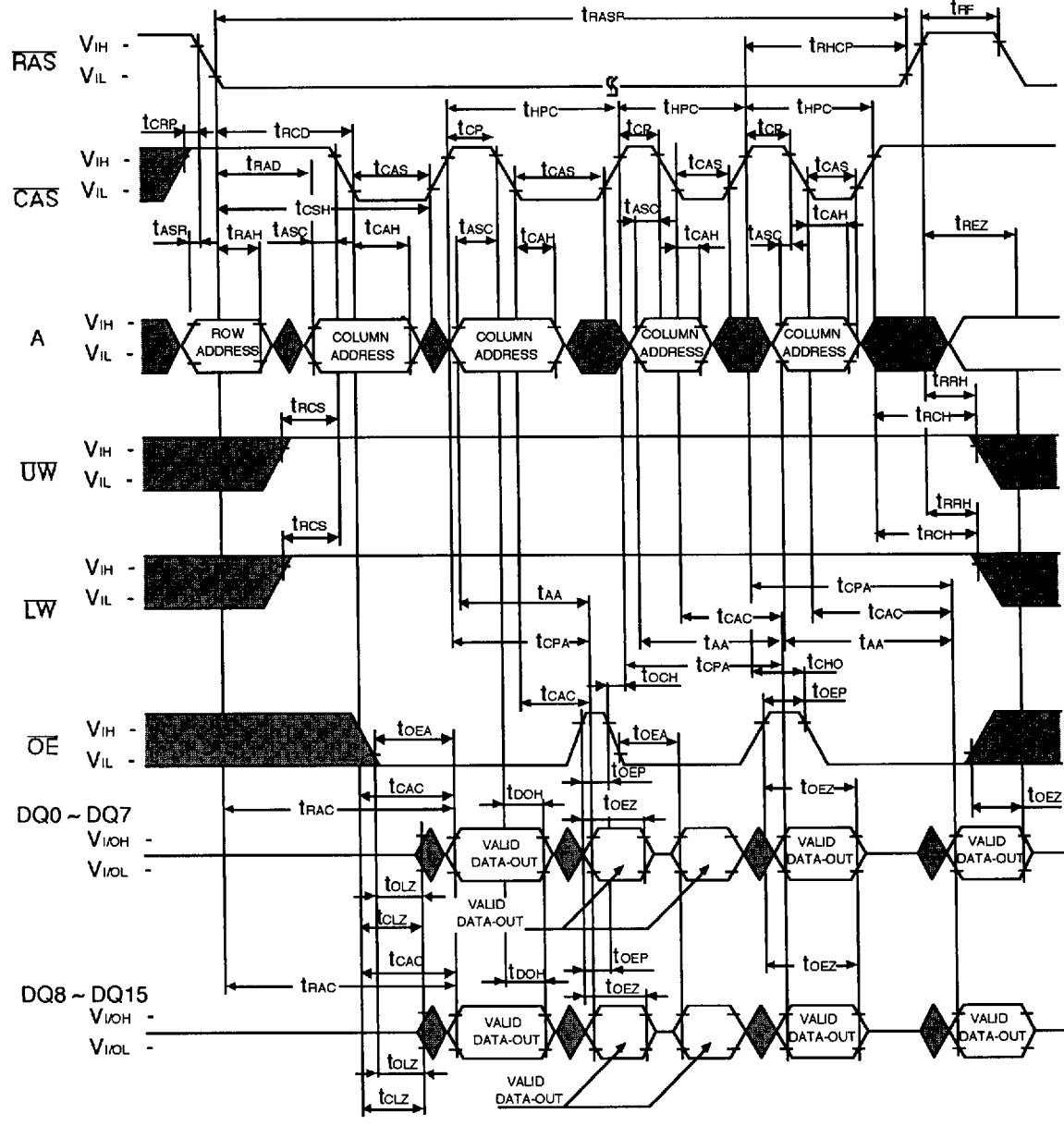


UPPER-BYTE READ - MODIFY - WRITE CYCLE



■ Don't Care

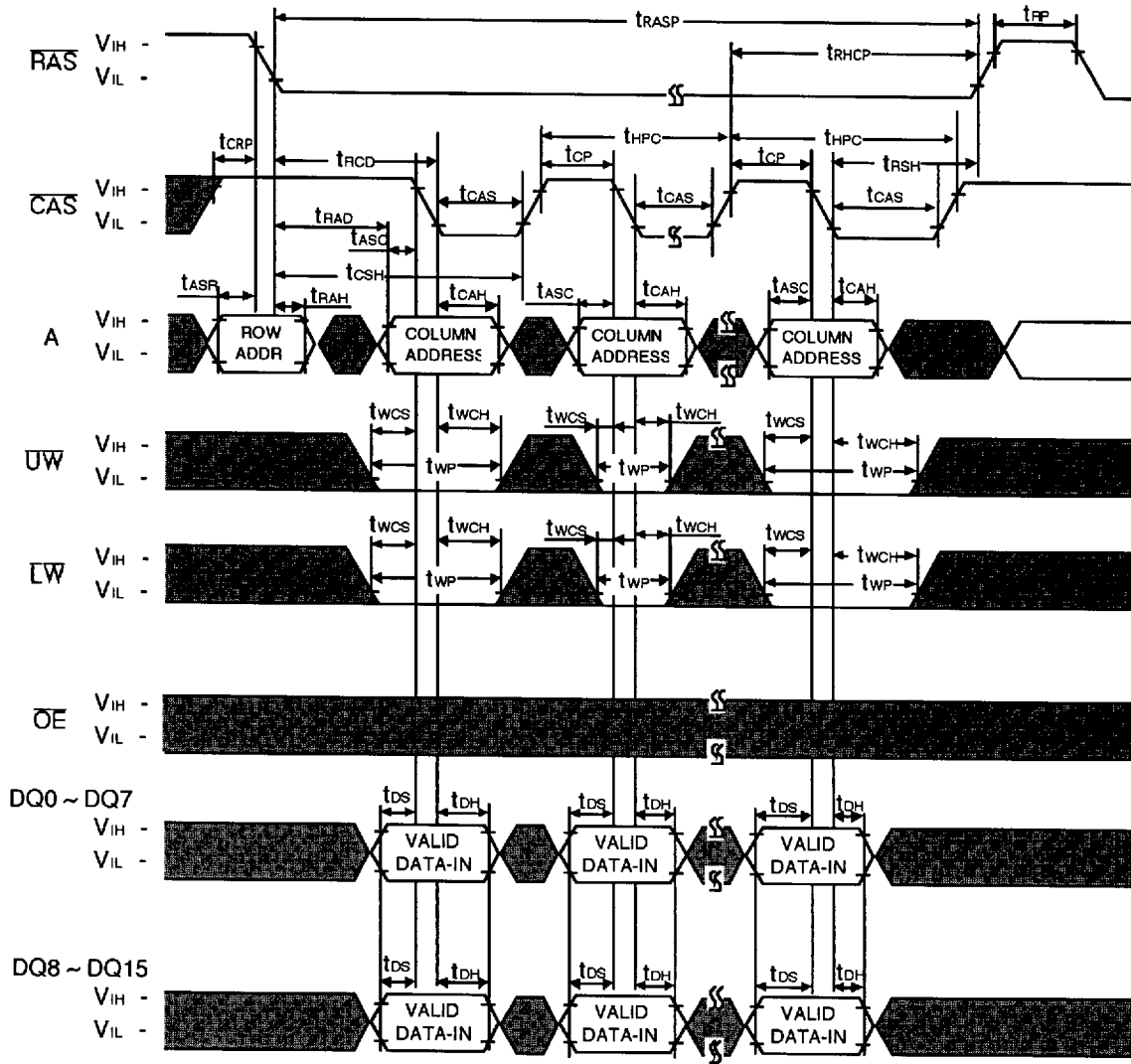
HYPER PAGE MODE WORD READ CYCLE



 Don't Care

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

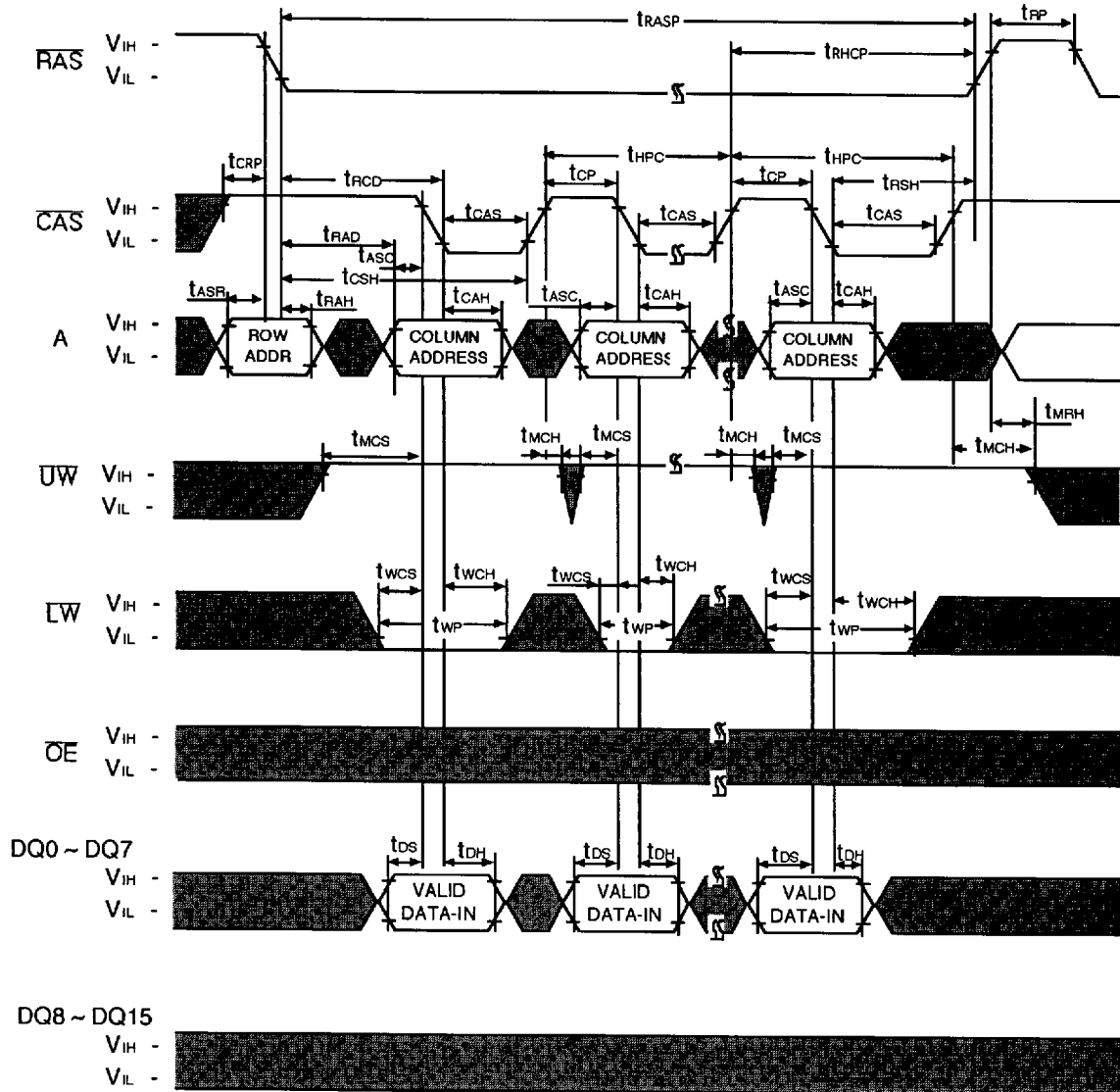
NOTE : Dout = Open



■ Don't Care

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

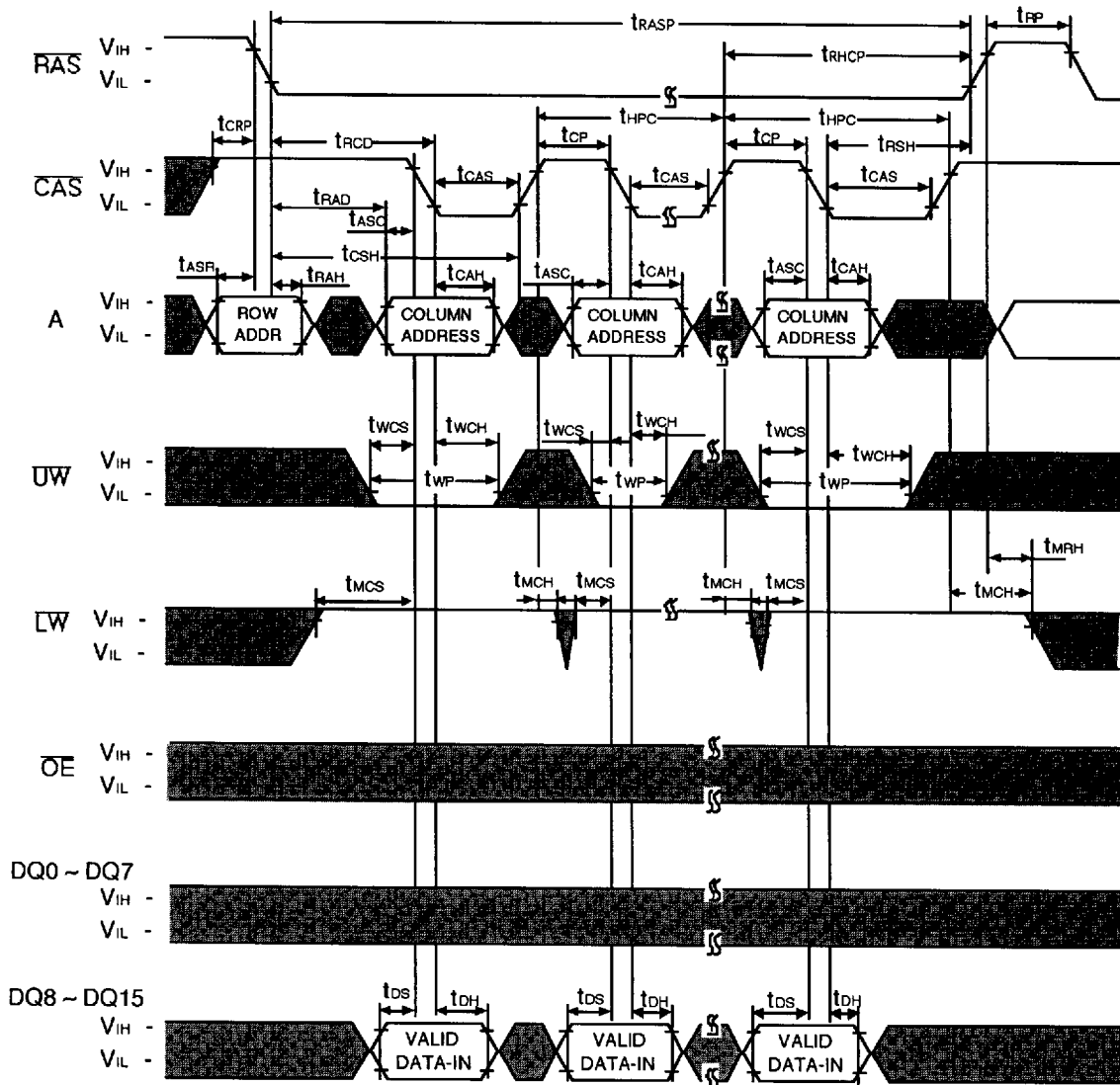
NOTE : DOUT = Open




■ Don't Care

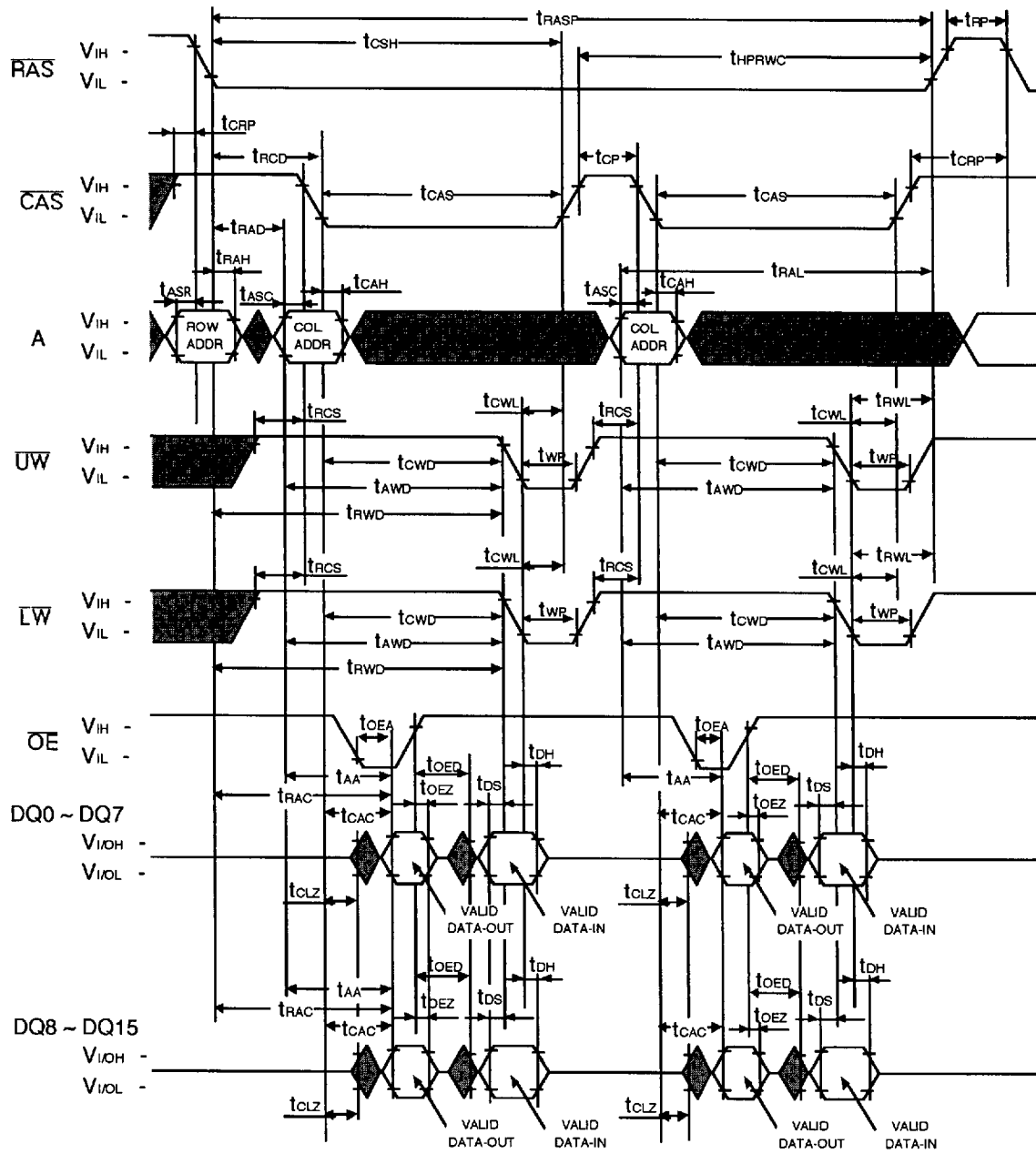
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = Open



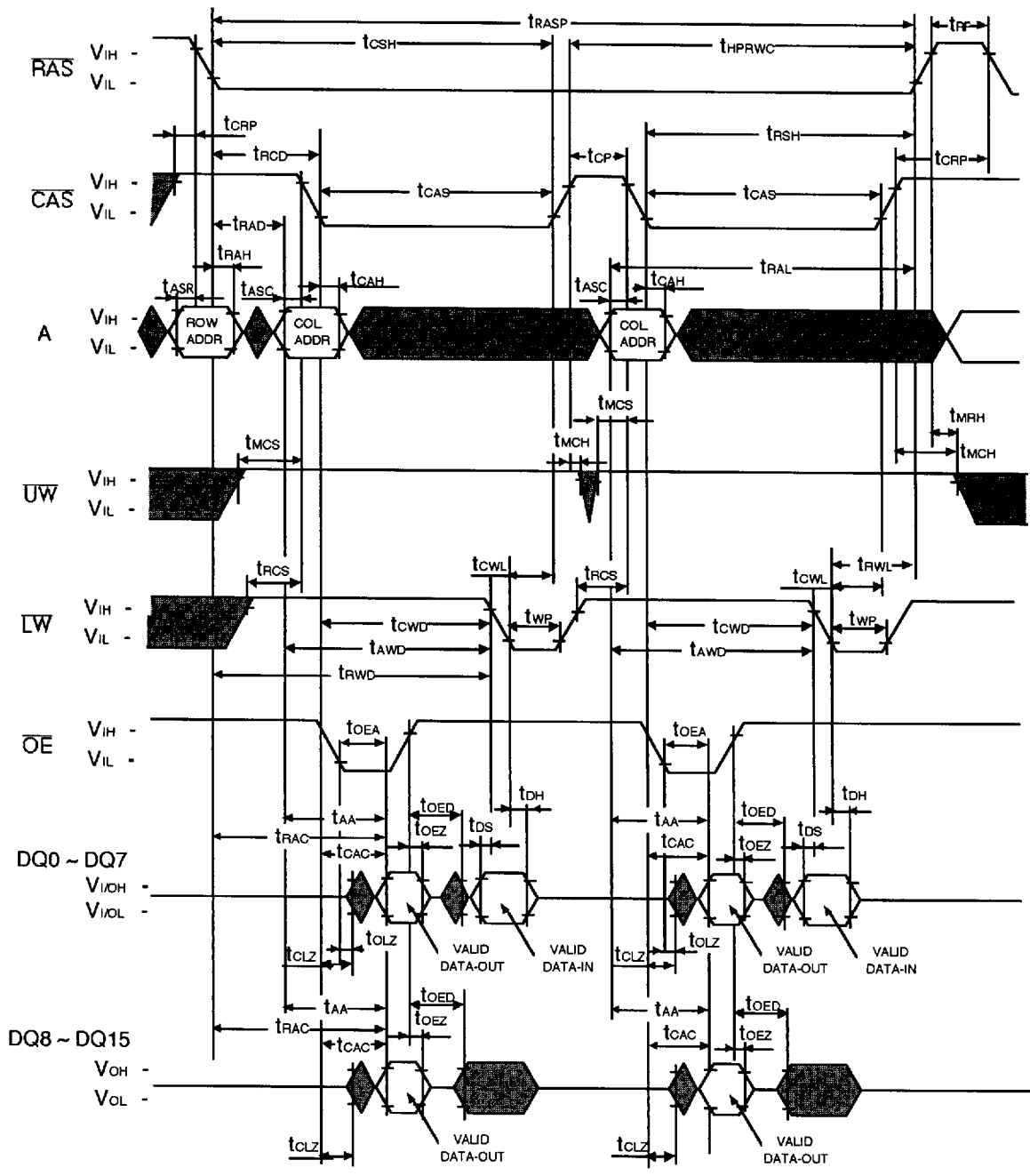
 Don't Care

HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



■ Don't Care

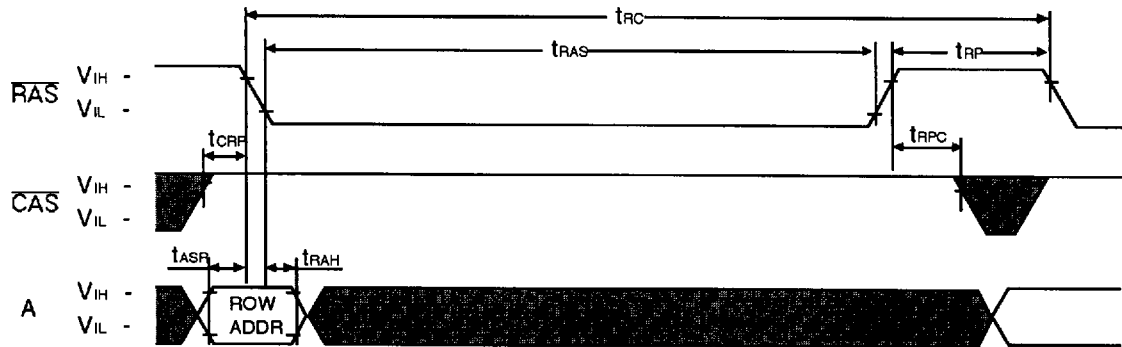
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



Don't Care

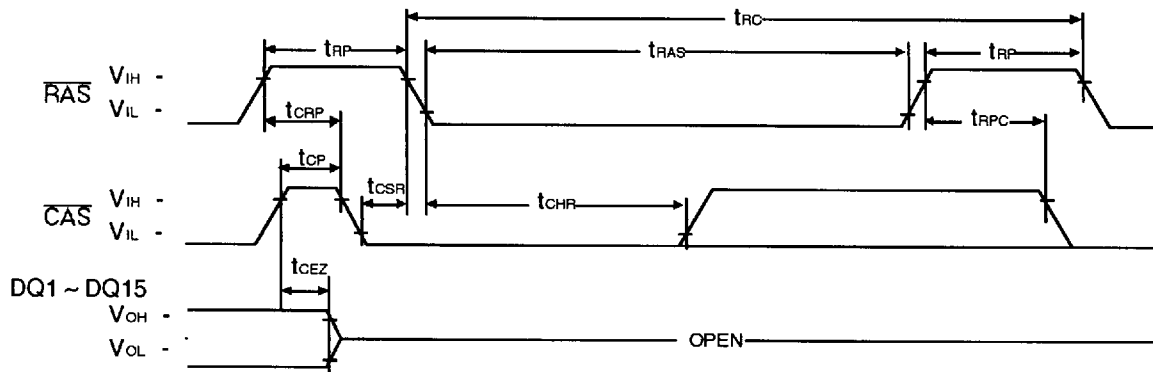
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



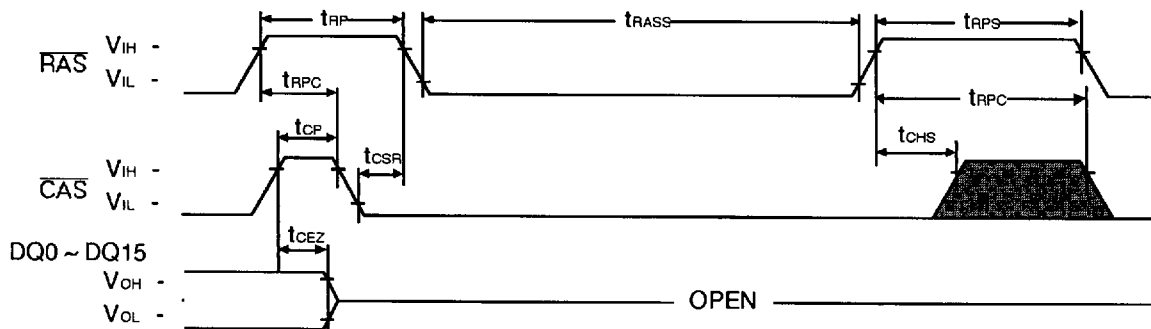
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care



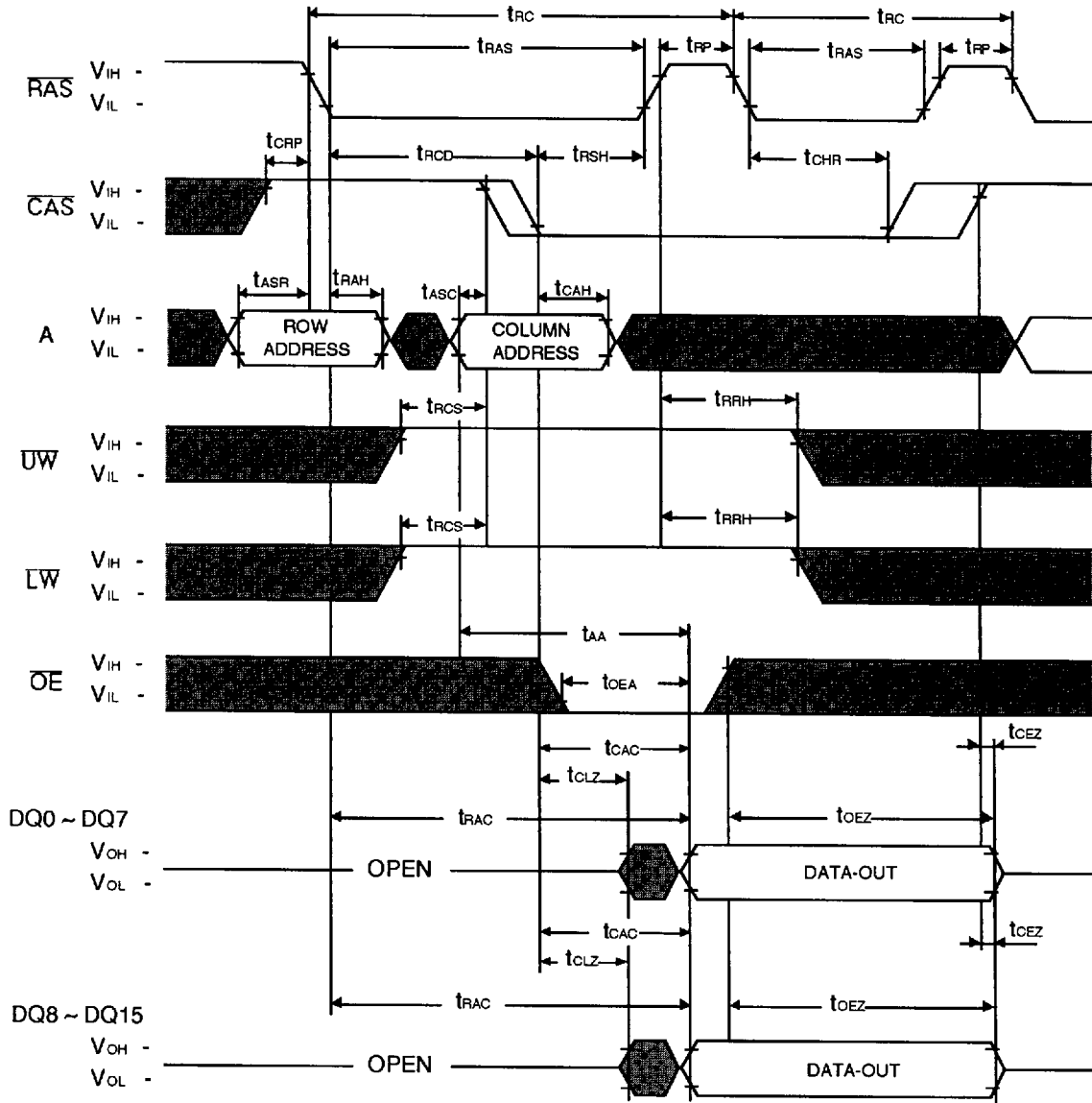
CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care



 Don't Care

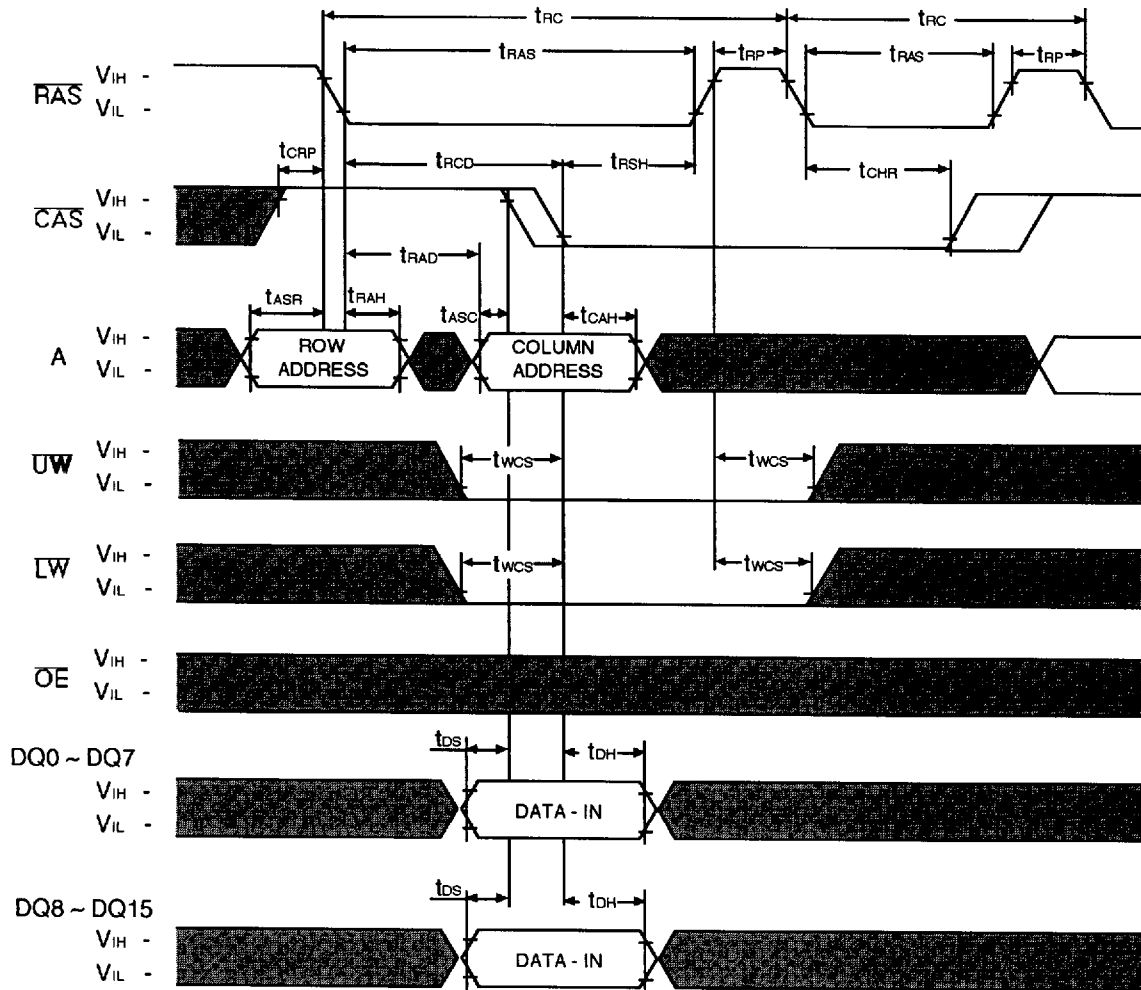
HIDDEN REFRESH CYCLE (READ)



■ Don't Care

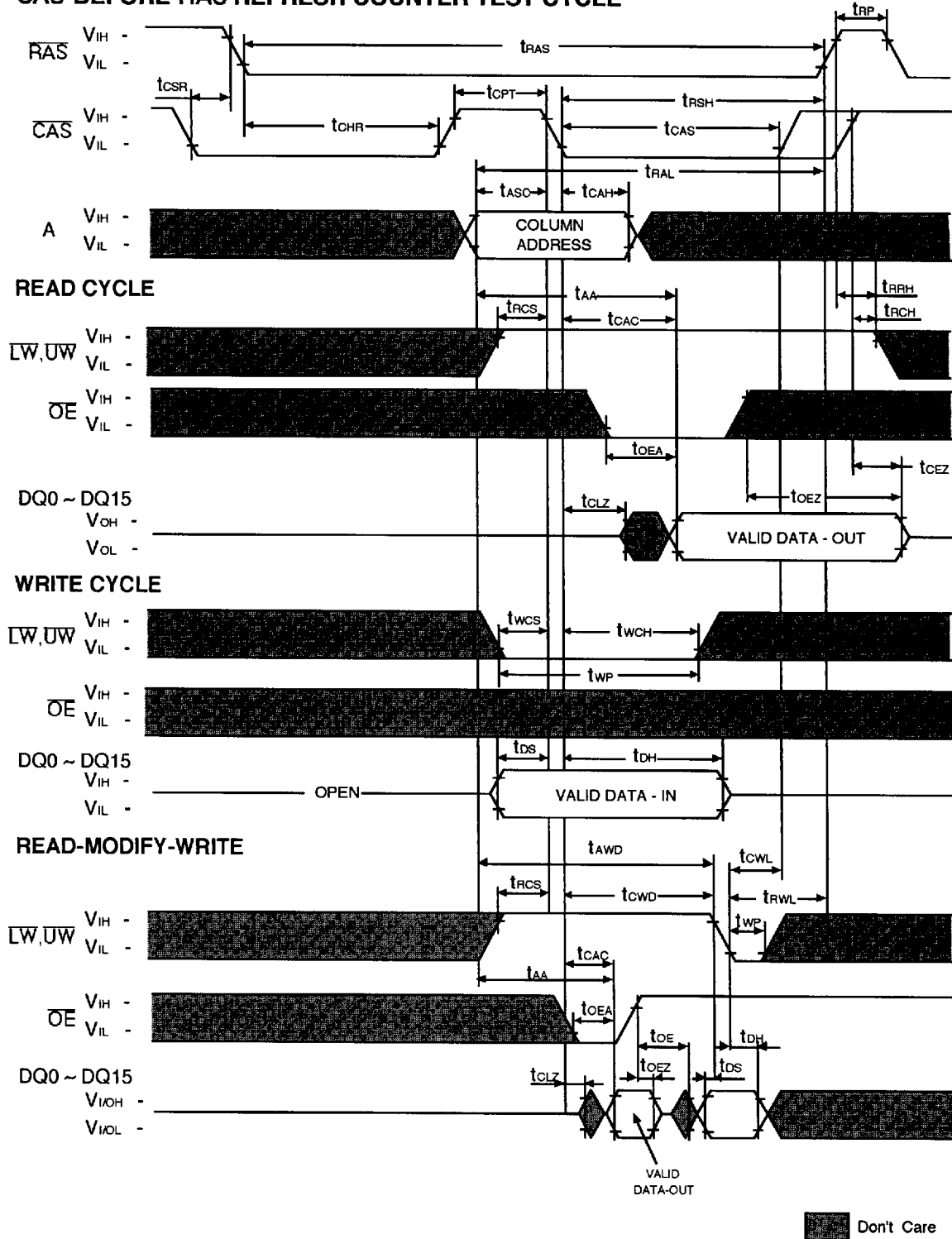
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{out} = OPEN



 Don't Care

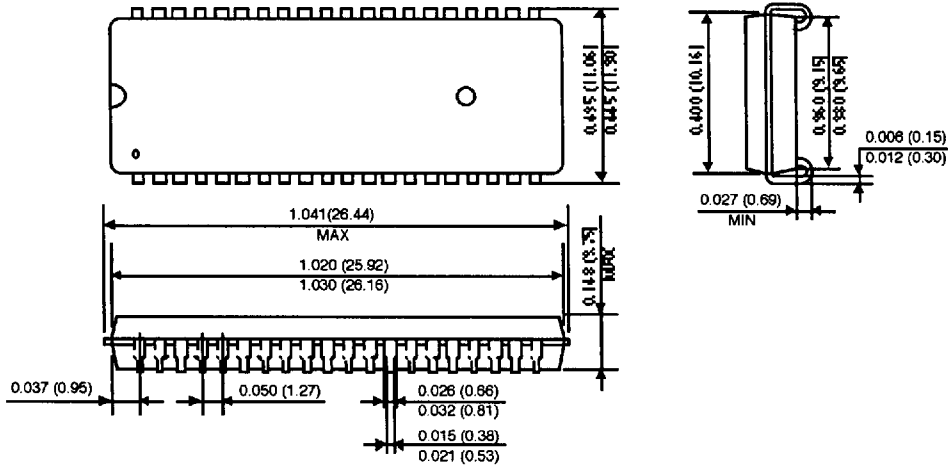
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PLASTIC SMALL OUT-LINE J-LEAD

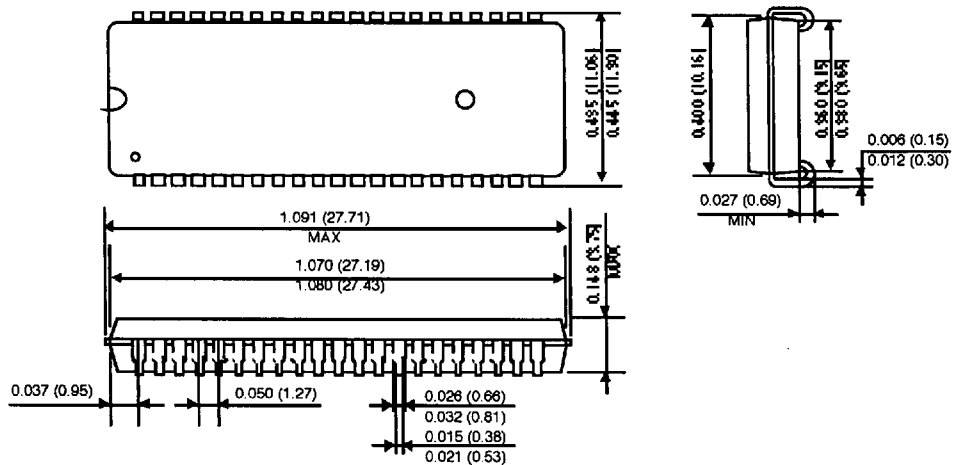
40SOJ 400 mil

Unit : Inches (millimeters)

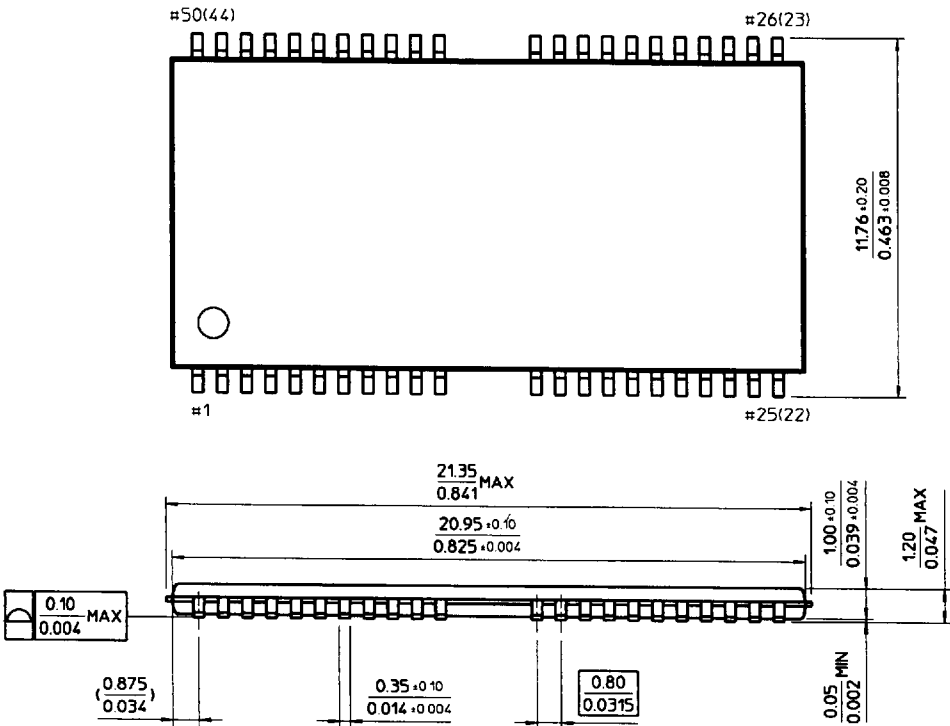


42 SOJ 400 mil

Unit : Inches (millimeters)



50(44)-TSOP2-400F



50(44)-TSOP2-400R

