Z86E08

CMOS Z8 8-BIT
MICROCONTROLLER

FEATURES

- 8-bit CMOS microcomputer, 18-pin DIP

- Low cost

- Low noise programmable

- ROM protect programmable

- 3.0 to 5.5 volt Vcc range

- Low power consumption -50 mW (typical)

- Brown-out protection

- Fast instruction pointer - 1 microsecond at 12 MHz

- Two standby modes - STOP and HALT

- 14 Input/Output lines

- All digital inputs, CMOS levels, Schmitt triggered.

- 2K bytes of one time PROM

- 144 bytes of RAM

- Two programmable 8-bit counter/timers each with a 6-bit programmable prescaler.

- 6 vectored, priority interrupts from 5 different sources.

- Clock speed 2, 8 and 12 MHz

- Watchdog Timer

- Power-On-Reset

- Two Comparators

- On-chip oscillator that accepts a crystal, ceramic resonator, LC, or external clock drive.

GENERAL DESCRIPTION

The Z86E08 Microcomputer (MCU) introduces a new level of sophistication to single-chip architecture. The Z86E08 is a member of the Z8 single-chip microcontroller family with 2K bytes of one-time PROM. The device is housed in an 18-pin DIP, and is manufactured in CMOS technology. The device offers easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

The Z86E08 is characterized by a flexible I/O scheme, an efficient register plus address space structure. Also, it has a number of ancillary features that are useful in many consumer, industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E08 fulfills this with 14-pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations; program memory and 124 bytes of general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86E08 offers two on-chip counter/timers with a large number of user selectable modes. Included are two on-board comparators that can process analog signals with a common reference voltage (Figures 1a and b).

Note: All Signals with a preceding front slash, "/", are active Low e.g.; B//W (WORD is active Low); /B/W (BYTE is active Low, only); /N//S (NORMAL and SYSTEM are both active Low).
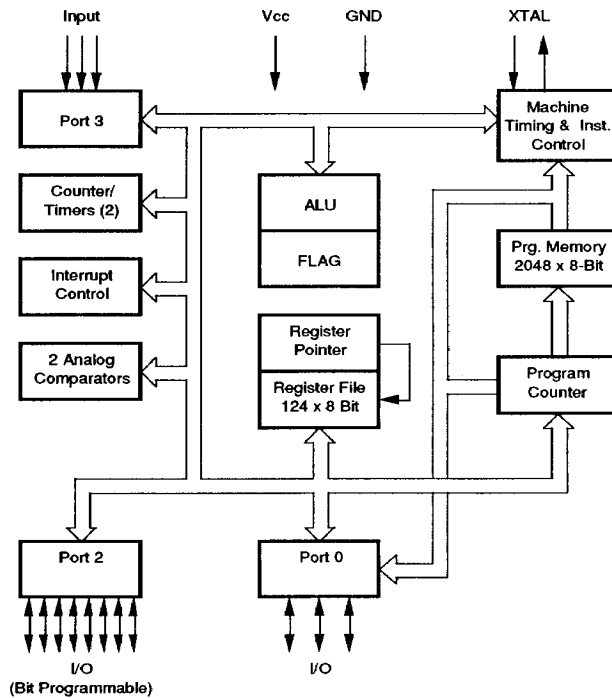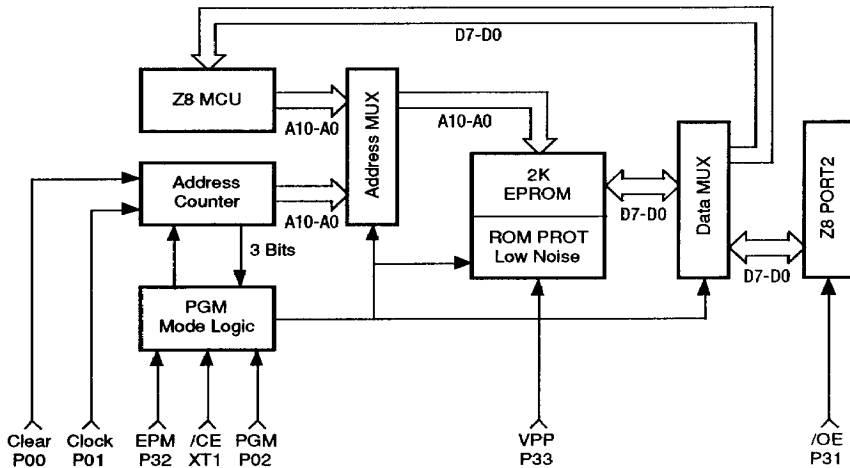
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Figure 1a. Functional Block Diagram

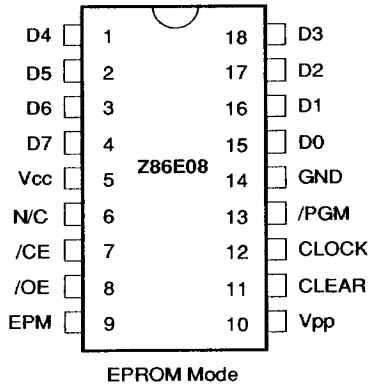**Figure 1b. EPROM Mode Block Diagram**

PIN IDENTIFICATION

EPROM Mode

Figure 2a. Pin Configuration

Normal Mode
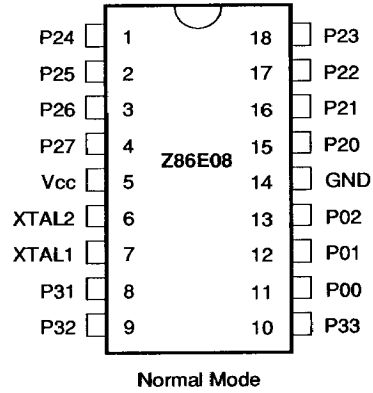
Figure 2b. Pin Configuration

Table 1a. Pin Identification

EPROM Mode			
Pin #	Symbol	Function	Direction
1-4	D4-7	Data 4,5,6,7	In/Output
5	V_{cc}	Power Supply	Input
6	N/C	No connection	
7	/CE	Chip Enable	Input
8	/OE	Output Enable	Input
9	EPM	EPROM Prog Mode	Input
10	Vpp	Prog Voltage	Input
11	Clear	Clear Clock	Input
12	Clock	Address	Input
13	/PGM	Prog Mode	Input
14	GND	Ground, V_{ss}	Input
15-18	D0-3	Data 0,1,2,3	In/Output

Table 1b. Pin Identification

Z86C08 Mode			
Pin #	Symbol	Function	Direction
1-4	P24-7	Port 2 pin 4,5,6,7	In/Output
5	V_{cc}	Power Supply	Input
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3 pin 1	Input
9	P32	Port 3 pin 2	Input
10	P33	Port 3 pin 3	Input
11-13	P00-2	Port 0 pin 0,1,2	Input/Output
14	GND	Ground, V_{ss}	Input
15-18	P20-3	Port 2 pin 0,1,2,3	In/Output

PIN FUNCTIONS

OTP Programming Mode

D7-D0. *Data Bus.* The data can be read from, or written to the EPROM through this data bus.

V$_{cc}$. *Power Supply.* It is 5V during the EPROM Read Mode and 6V during the other modes.

/CE. *Chip Enable. Active Low.* This pin is active during EPROM Read Mode, Program Mode, and Program Verify Mode.

/OE. *Output Enable. Active Low.* This pin drives the Data Bus direction. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM. *EPROM Program Mode.* This pin controls the different EPROM Program Modes by applying different voltages.

V$_{PP}$. *Program Voltage.* This pin supplies the program voltage.

Clear. *Clear, Active High.* This pin clears the internal address counter at the High Level.

Clock. *Address Clock.* This Pin is a serial address input. The internal address counter increases by one with one clock signal.

/PGM. *Program Mode. Active Low.* Low Level at this pin programs the data to the EPROM through the Data Bus.

4

XTAL1, XTAL2. *Crystal In, Crystal Out (time-based input and output, respectively).* These pins connect a parallel-resonant crystal, LC, or an external single-phase clock (12 MHz max) to the on-chip clock oscillator and buffer.

Port 0 P00-P02. Port 0 is a 3-bit bi-directional, CMOS compatible I/O port. These 3 I/O lines can be globally configured under software control to be an input or output (Figure 3).
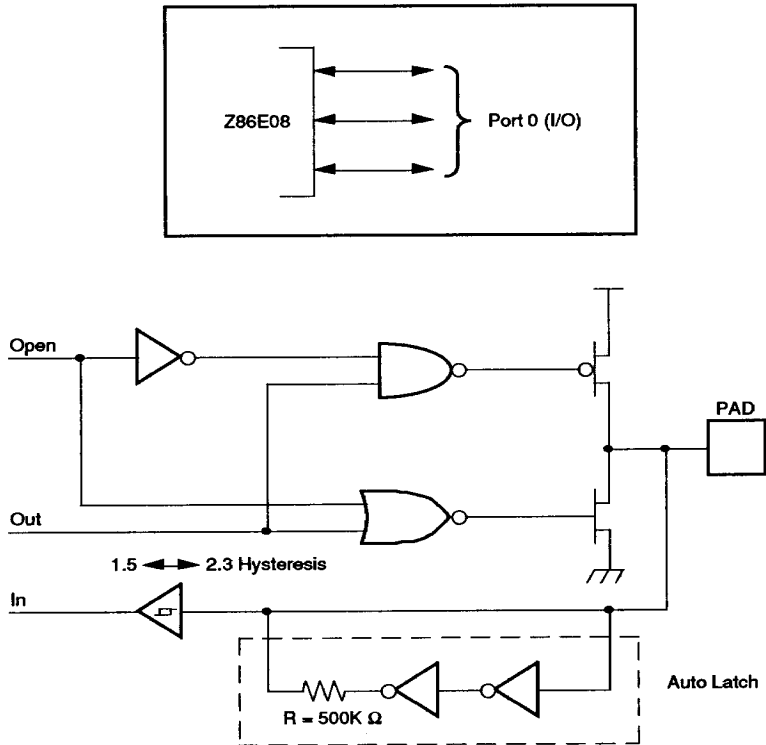
Figure 3. Port 0 Configuration

Port 2 P20-P27. Port 2 is an 8-bit, bit programmable, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 4).
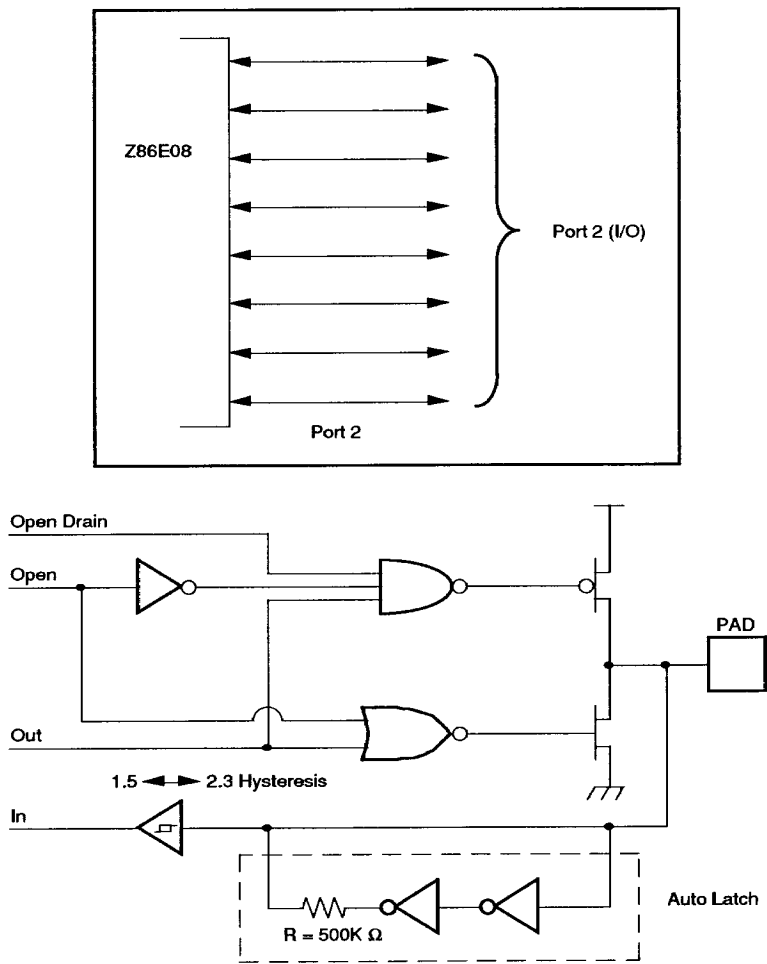
Figure 4. Port 2 Configuration

Port 3 P31-P33. Port 3 is a 3-bit, CMOS compatible port with three fixed input (P30-P32) lines. These three input lines can be configured under software control as digital inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal (Tin) (Figure 5).

IRQ 0,1,2 = Falling Edge Detection
IRQ3   = Rising Edge Detection
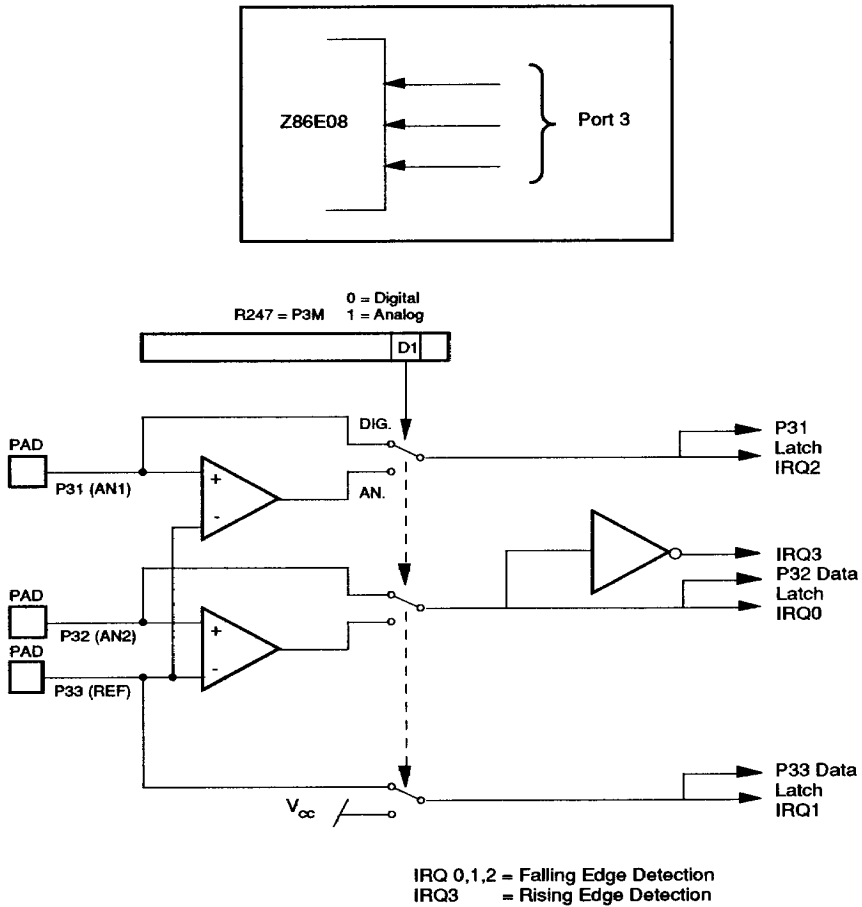
Figure 5. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3 P31, and P32 for interface flexibility. The comparators reference voltage P3REF is common to both comparators.

Typical applications for the on-board comparators are: Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input function serving as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP Mode. The common voltage range is 0-4V; the power supply and common mode rejection ratios are 90dB and 60dB, respectively.

Interrupts are generated on either edge of comparator 2's output, or on the falling edge of comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or Tin through P31. Alternatively, the comparators may be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

SPECIAL FUNCTIONS

The Z8 MCU incorporates special functions to enhance the Z8's application in industrial, scientific research and advanced technologies applications.

Reset. RESET is accomplished through Power On or a watch dog timer RESET. Upon Power Up, the power-on reset circuit waits for 50 msec plus 18 crystal clocks and then starts program execution at address %000C(HEX). Reference a table of the Z86E08 control registers' Reset values (Figure 6).
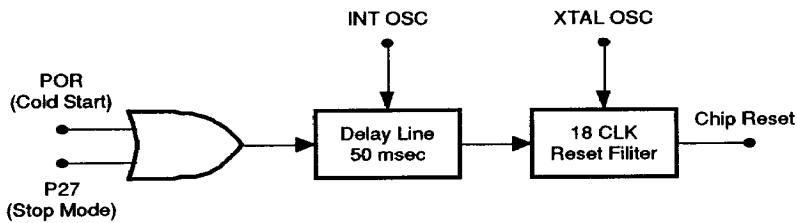

Figure 6. Internal Reset Configuration

Power-On Reset *(POR)*. A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows Vcc and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by on one of three conditions:

■ Power bad to power good status
■ STOP Mode recovery
■ WDT time out

Watch Dog Timer Reset. The WDT is a retriggerable one-shot timer that will reset the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and will be retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator.

Table 1. Z86E08 Control Registers

Addr.	Reg.	Reset Condition								Comments
		D7	D6	D5	D4	D3	D2	D1	D0	
F1	TMR	0	0	0	0	0	0	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F4	T0	U	U	U	U	U	U	U	U	
F5	PRE0	U	U	U	U	U	U	U	0	
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset.
F7*	P3M	U	U	U	U	U	U	0	0	
F8*	P01M	U	U	U	0	U	U	0	1	
F9	IPR	U	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection.
PB	IMR	0	U	U	U	U	U	U	U	
PC	FLAGS	U	U	U	U	U	U	U	U	
FD	RP	0	0	0	0	0	0	0	0	
FF	SPL	U	U	U	U	U	U	U	U	

* Not reset after a low on P27 to get out of STOP Mode

Program Memory. The Z86E08 addresses up to 2K bytes of internal program memory (Figure 7). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-2048 is on-chip one-time programmable PROM.
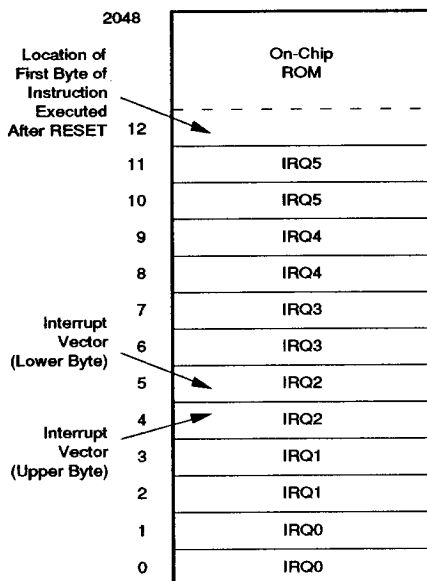
Figure 7. Program Memory Map

Register File. The Register File consists of three I/O port registers, 124 general purpose registers, and 14 control and status registers (R0-R3, R4-R127 and R241-R255, respectively (Figure 8). General purpose registers occupy the %04 to %7F address space. I/O ports are mapped as per the existing CMOS Z8. The Mode and Configuration Registers should be as in the Z86C08. The Z86E08 instruc-tions can access registers directly or indirectly via an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 9) addresses the starting location of the active working-register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	General Purpose Register	GPR
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	HMH
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	T0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
127	Not Implemented	
	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	P1
0	Port 0	P0

Figure 8. Register File

r_7 r_6 r_5 r_4 r_3 r_2 r_1 r_0 R253

The upper nibble of the register file address provided by the register pointer specifies the active working-register group

R127

The lower nibble of the register file address provided by the instruction points to the specified register

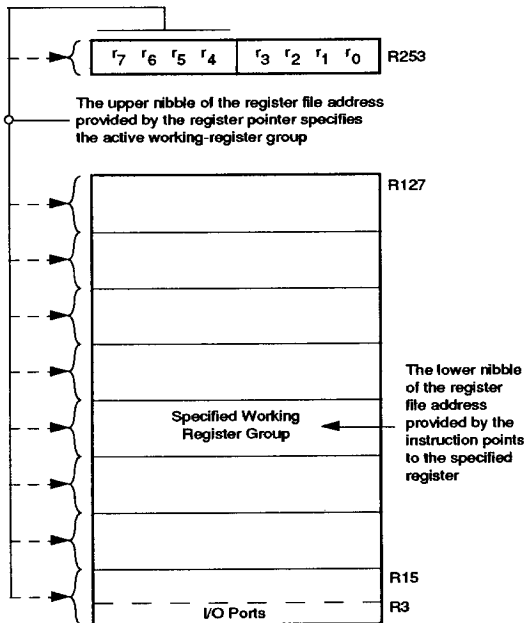Specified Working Register Group

R15

I/O Ports   R3

Figure 9. Register Pointer

Stack Pointer. The Z86E08 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 124 general-purpose registers.

GPR. *(R254.)* This register is a general-purpose register.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however the T0 can be driven by the internal clock source only (Figure 10).

The 6-bit prescalers divides the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ4 (T0) or IRQ5 (T1) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that is retriggerable or not retriggerable, or used as a gate input for the internal clock.
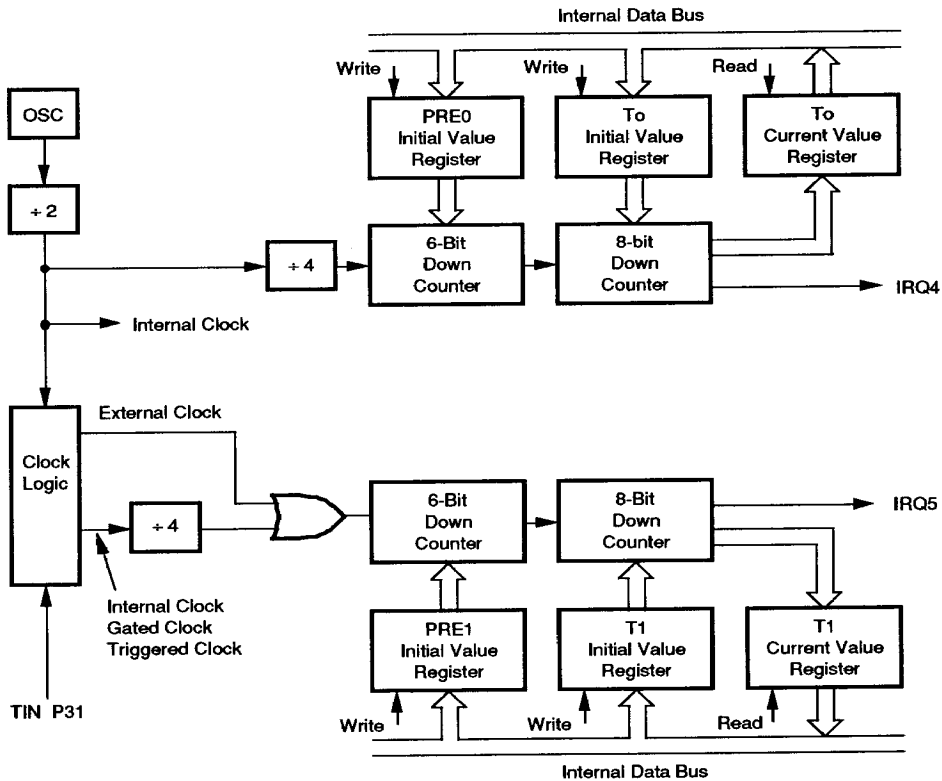
Figure 10. Counter/Timers Block Diagram

11

Interrupts. The Z86E08 has six interrupts from five different sources. These interrupts are maskable and prioritized (Figure 11). The five sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33(REF), and two counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 2).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86E08 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Table 2. Interrupt Types, Sources, and Vectors

| Source	Name	Vector Location	Comments
AN2(P32)	IRQ0	0,1	External (F)Edge
REF(P33)	IRQ1	2,3	External (F)Edge
AN1(P31)	IRQ2	4,5	External (F)Edge
AN2(P32)	IRQ3	6,7	External (R)Edge
T0	IRQ4	8,9	Internal ---
T1	IRQ5	10,11	Internal ---

F=Falling edge triggered
R=Rising edge triggered
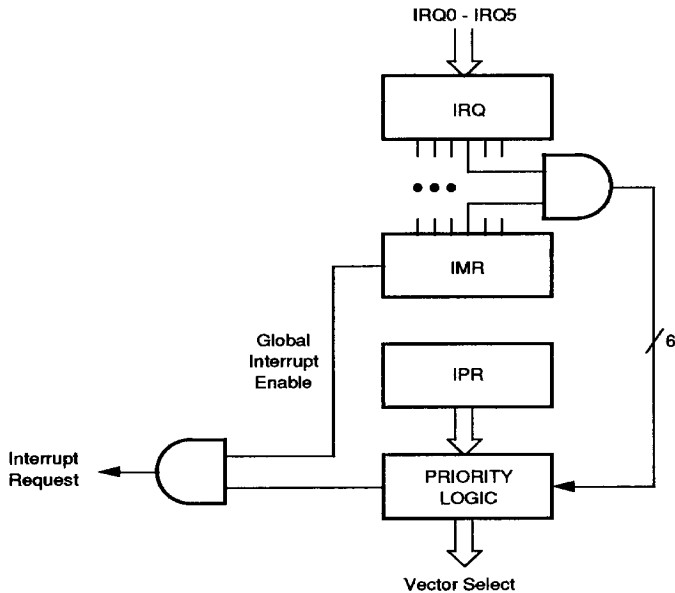
Figure 11. Interrupt Block Diagram

Clock. The Z86E08 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source. The crystal should be AT cut, 12 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal is connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is between 10 pf to 250 pf which depends on the crystal manufacturer, ceramic resonator and PCB layout) from each pin to ground (Figure 12).

Ceramic Resonator   LC Clock   External Clock
or Crystal
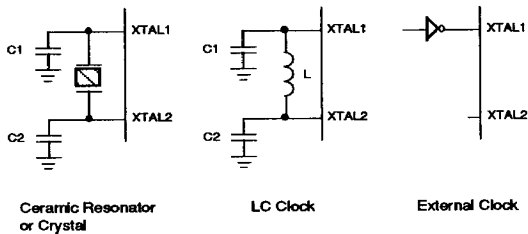
Figure 12. Oscillator Configuration

HALT Mode. Turns off the internal CPU clock but not the crystal oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. The program execution begins at location %000C (HEX). The Icc in HALT state is Icc (run mode) divided by 10.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA. The STOP Mode is released by a RESET via a STOP Mode Recovery, P27. Program execution under both conditions begins at location %000C (HEX). However, when P27 is used to release the STOP Mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP Mode, use the following instruction:

```
OR  P2M, #%80
NOP
STOP
```

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction. i.e.:

FF	NOP;	clear the pipeline
6F	STOP;	enter STOP mode
		or
FF	NOP;	clear the pipeline
7F	HALT;	enter HALT mode

Watch Dog Timer *(WDT).* The Watch Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed once the WDT is enabled within every 15 msec; otherwise the Z86E08 resets itself.

WDT=5F (HEX)

Opcode WDT *(5F%).* The first time opcode %5F is executed, the WDT is enabled and subsequent execution clears the WDT counter. This has to be done at least every 15 msec. Otherwise, the WDT will time out and generate a reset. The generated reset is the same as a power on reset of 50 msec +18 XTAL clock cycles.

Opcode WDH *(%4F).* When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT function running during HALT Mode. A WDH instruction executed without executing WDT (%5F) has no effect.

Brown-Out Protection (V_{BO}). The brown out trip voltage (V_{BO}) is less than 3 volts and above 1.4 volts under the following conditions.
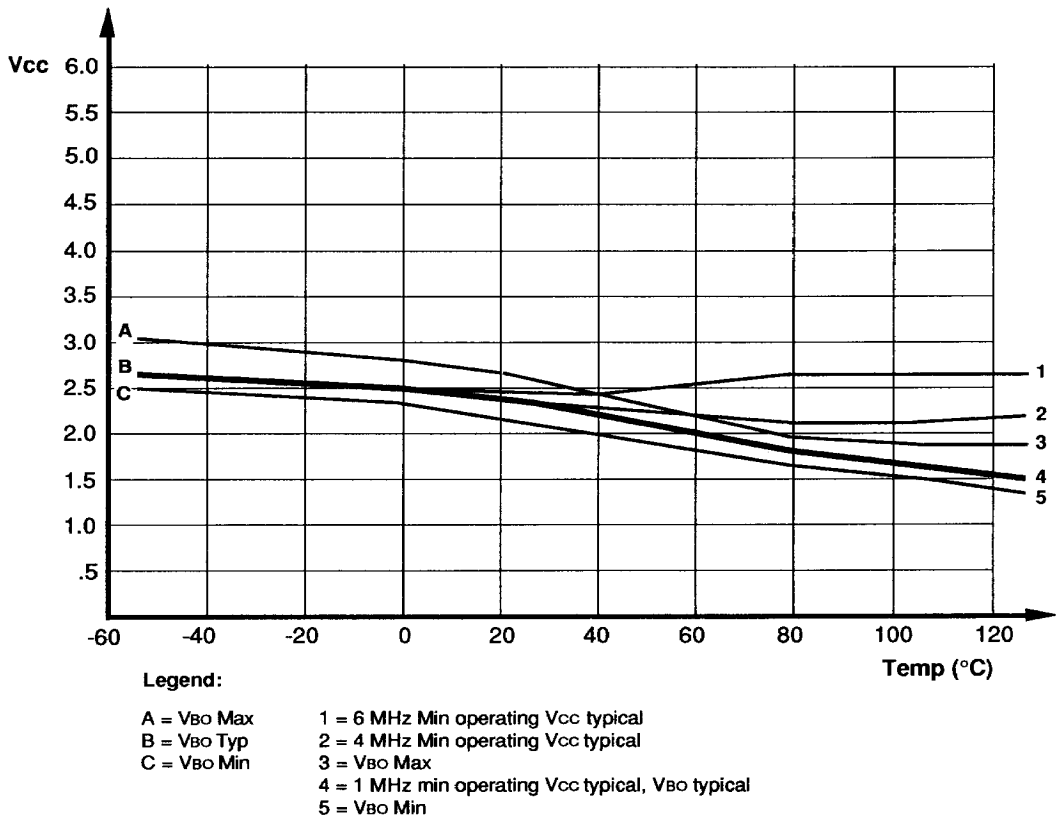
Maximum (V_{BO}) Conditions

Case 1   TA= -40°C, +105°C, Internal Clock Frequency (equal or less than 1 MHz)

Case 2   TA= -40°C, +85°C, Internal Clock Frequency (equal or less than 2 MHz)

Note: The internal clock frequency is one half the external clock frequency.

The device functions normally at, or above, 3.0V under all conditions. Below 3.0V, the device functions normally until the Brown Out Protection trip point (V_{BO}) is reached for the temperatures and operating frequencies shown above.

The device is guaranteed to function normally at supply voltages above the brown-out trip point. The actual brown out trip point is a function of temperature and process parameters (Figure 13).

Legend:

A = VBO Max   1 = 6 MHz Min operating Vcc typical
B = VBO Typ   2 = 4 MHz Min operating Vcc typical
C = VBO Min   3 = VBO Max
                     4 = 1 MHz min operating Vcc typical, VBO typical
                     5 = VBO Min

Note: All frequencies are internal frequency.

Figure 13. V_{cc} Vs Temperature

At, and below the brown-out trip point, the device is kept in reset. This implies that the device is always either in a normal function mode or in reset mode.

2 MHz (Typical)

Temp	-40	0	25	70	105°C
V_{BO}	2.25	2.4	2.21	1.7	1.6

Low EMI Emission

The 86E08 can be programmed to operate in a low EMI emission mode by means of an EPROM programmable bit option. Use of this feature results in:

- Less than 1 mA consumed during HALT mode.

- All pre-drivers slew rates reduced to 10 ns typical.

- Internal SLCK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.

- Output drivers have resistances of 200 ohms (typical).

- Oscillator divide-by-two circuitry eliminated.

ROM Protect. ROM Protect is fully protecting the ROM code in the Z86E08 to be read by the programmer or other machines. When ROM protect is selected, the Z86Z08 will disable the instructions of "LDC" and "LDCI" (Z86E08 and Z86C08 do not support the instructions of "LDE" and "LDEI").

User Modes. Table 3 shows the programming voltage of each mode of Z86E08.

Table 3. OTP Programming Table

User Modes	V_{PP} (P33)	EPM (P32)	/CE (XTAL1)	/OE (P31)	/PGM (P02)	ADDR	DATA (Port2)	V_{CC}
EPROM Read	X	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	Data Out	5.0V
Program	V_{PP}	X	V_{IL}	V_{IH}	V_{IL}	Addr	Data In	6.0V
Program Verify	V_{PP}	X	V_{IL}	V_{IL}	V_{IH}	Addr	Data Out	6.0V
EPROM Protect	V_{PP}	V_H	V_H	V_{IH}	V_{IL}	X	X	6.0V
Low Noise	V_{PP}	V_{IH}	V_H	V_{IH}	V_{IL}	X	X	6.0V

Notes:
$V_{PP} = 12.5V \pm 0.5V$
$V_H = 12.5V \pm 0.5V$
X = TTL Level (irrelevant)
$V_{IH} = 5.0V$
$V_{IL} = 0V$

Serial Address Input. The address of Z86E08 is serial input from pin P01 (Clock). Each clock signal increases the address by one and the "high" level of pin P00 (Clear) will reset the address to zero. Figure 14 shows the set-up time of the serial address ihnput.

Programming Waveform. Figures 15, 16 and 17 show the programming waveforms of each mode. Table 4 shows the timing of programming waveforms.

Programming Algorithm. Figure 18 shows the flow chart of Z86E08 programming algorithm.

Table 4. Timing of Programming Waveform

Parameters	Name	Min	Max
1	Address Setup Time	2 μsec	
2	Data Setup Time	2 μsec	
3	VPP Setup Time	2 μsec	
4	V_{CC} Setup Time	2 μsec	
5	Chip Enable SetupTime	2 μsec	
6	Program Pulse Width	0.95 msec	1.05 msec

Table 4. Timing of Programming Waveform (Continued)

Parameters	Name	Min.	Max
7	Data Hold Time	2 μsec	
8	OE Setup Time	2 μsec	
9	Data Access Time		200 nsec
10	Data Output Float Time		100 nsec
11	Overprogram Pulse Width	2.85 msec	78.75 msec
12	EPM Setup Time	2 μsec	
13	OE Setup Time	2 μsec	
14	Address to OE Setup Time	2 μsec	
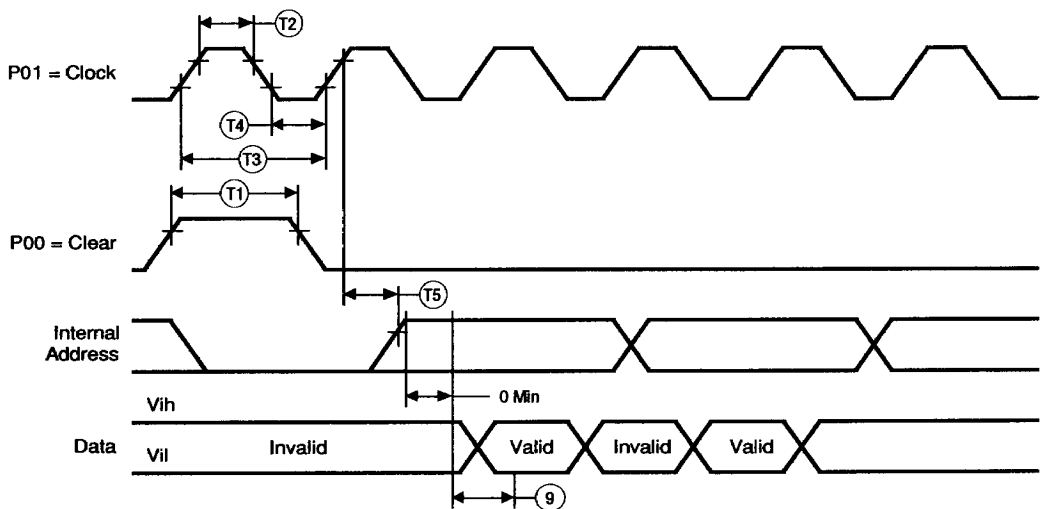
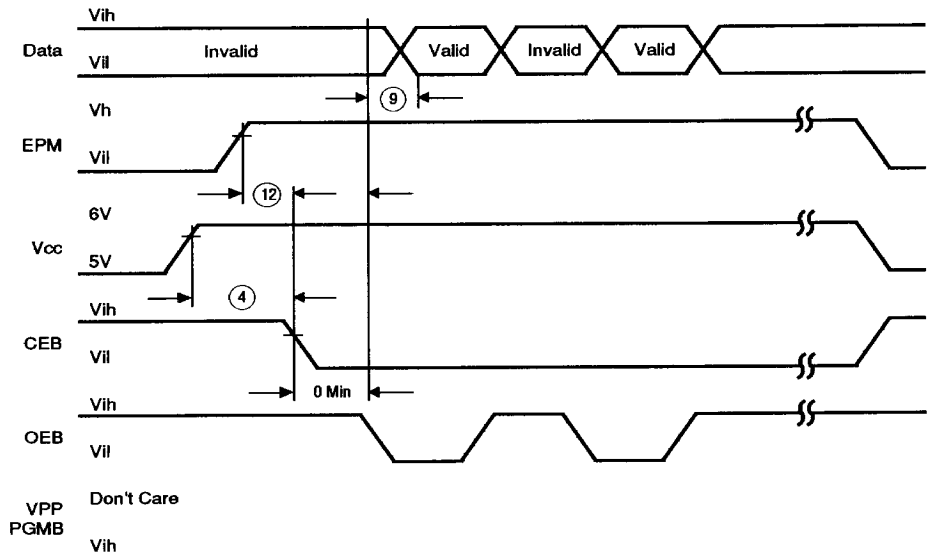| Legend:	
T1 Reset Clock Width	30 ns Min
T2 Input Clock High	30 ns Min
T3 Input Clock Period	70 ns Min
T4 Input Clock Low	30 ns Min
T5 Clock to Address Counter Out Delay	15 ns Max

Figure 14. Z86E08 Serial Address Waveform

16

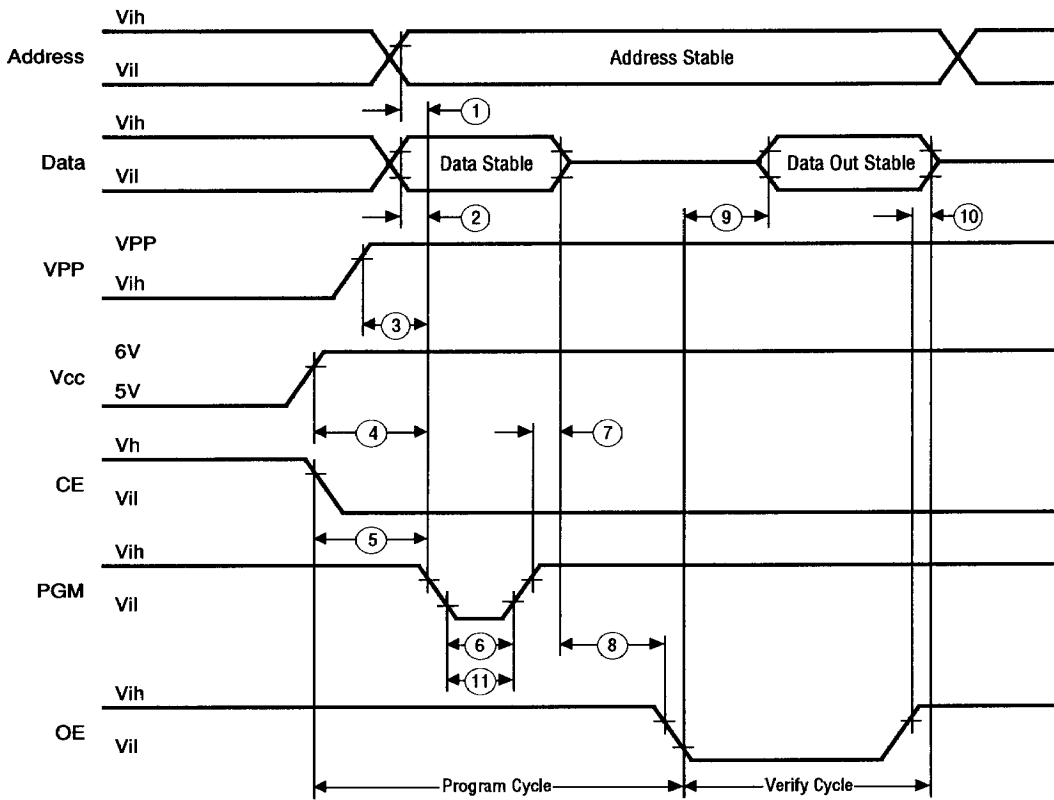**Figure 15. Z86E08 Programming Waveform** (User Mode 1)

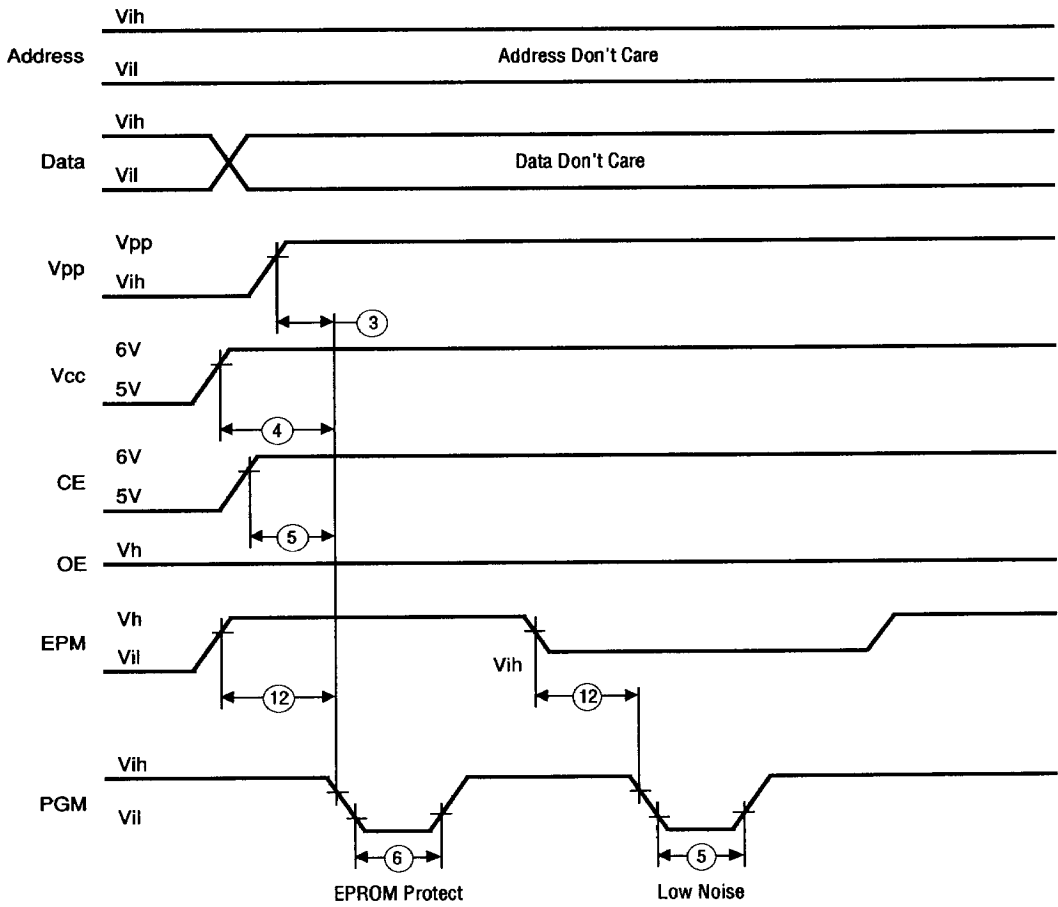**Figure 16. Z86E08 Programming Waveform** (User Modes 2,3)

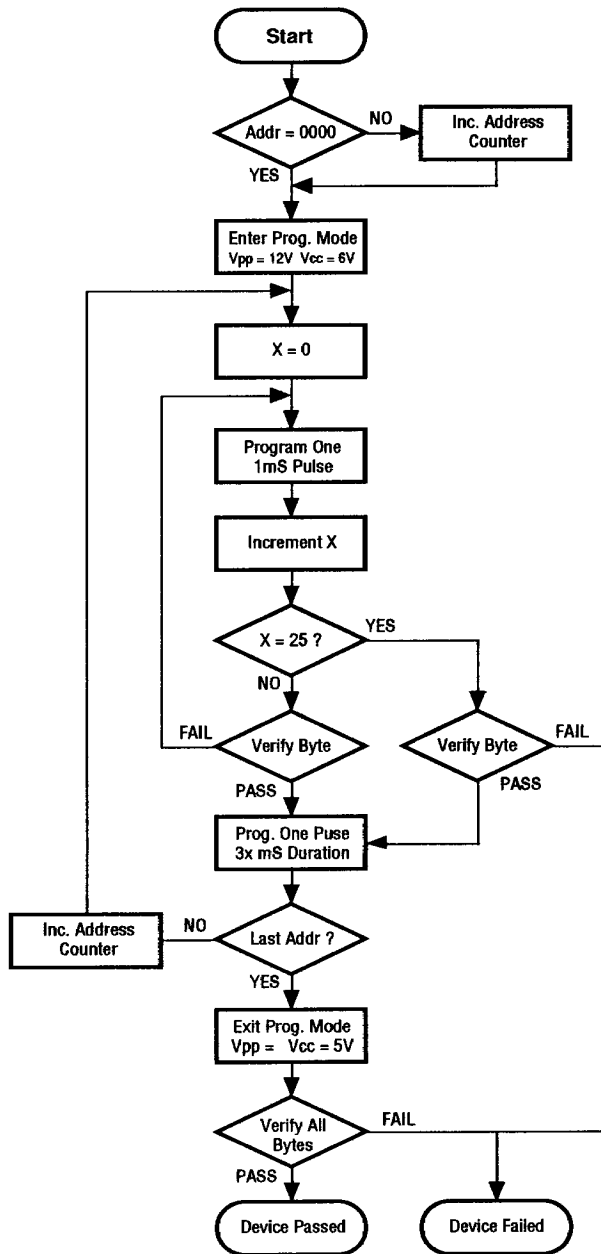**Figure 17. Z86E08 Programming Waveform** (User Modes 4,5)

Start

Addr = 0000

NO → Inc. Address Counter

YES

Enter Prog. Mode
Vpp = 12V Vcc = 6V

X = 0

Program One
1mS Pulse

Increment X

X = 25 ?

YES

NO

Verify Byte — FAIL

Verify Byte — FAIL

PASS

PASS

Prog. One Puse
3x mS Duration

Inc. Address Counter — NO — Last Addr ?

YES

Exit Prog. Mode
Vpp =   Vcc = 5V

Verify All Bytes — FAIL

PASS

Device Passed

Device Failed

Figure 18. Z86E08 Programming Algorithm

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 19).
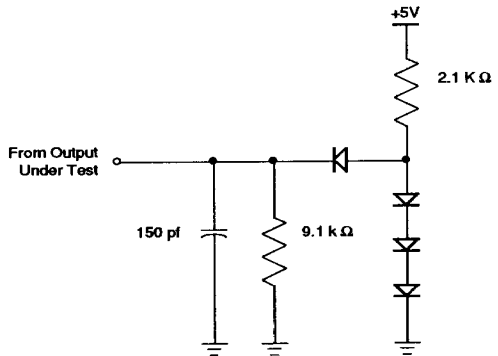

Figure 19. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{cc}	Supply Voltage*	-0.3	+7	V
TSTG	Storage Temp	-65	+150	C
TA	Oper Ambient Temp	†	†	C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND.

Parameter	Max
Input Capacitance	10 pf
Output Capacitance	20 pf
I/O Capacitance	25 pf

V_{cc} SPECIFICATION

Low V_{cc}	3.3V ± 0.3V
High V_{cc}	5.0V ± 0.5V

21

DC ELECTRICAL CHARACTERISTICS
Z86E08

Symbol	Parameter	V_{cc}	$T_A = 0°C$ to 70°C		$T_A = -40°C$ to 105°C		Typical @ 25°C	Units	Conditions
			Min	Max	Min	Max			
	Max Input Voltage	3.0V		12		12		V	$V_{IN} = 250\ \mu A$
		5.5V		12		12		V	$V_{IN} = 250\ \mu A$
V_{CH}	Clock Input High Voltage	3.0V	$0.7\ V_{cc}$	$V_{cc}+0.3$	$0.7\ V_{cc}$	$V_{cc}+0.3$	1.7	V	Driven by External Clock Generator
		5.5V	$0.7\ V_{cc}$	$V_{cc}+0.3$	$0.7\ V_{cc}$	$V_{cc}+0.3$	2.75	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	3.0V	$V_{ss}-0.3$	$0.2\ V_{cc}$	$V_{ss}-0.3$	$0.2\ V_{cc}$	0.8	V	Driven by External Clock Generator
		5.5V	$V_{ss}-0.3$	$0.2\ V_{cc}$	$V_{ss}-0.3$	$0.2\ V_{cc}$	1.5	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	3.0V	$0.7\ V_{cc}$	$V_{cc}+0.3$	$0.7\ V_{cc}$	$V_{cc}+0.3$	1.8	V	
		5.5V	$0.7\ V_{cc}$	$V_{cc}+0.3$	$0.7\ V_{cc}$	$V_{cc}+0.3$	2.8	V	
V_{IL}	Input Low Voltage	3.0V	$V_{ss}-0.3$	$0.2\ V_{cc}$	$V_{ss}-0.3$	$0.2\ V_{cc}$	0.8	V	
		5.5V	$V_{ss}-0.3$	$0.2\ V_{cc}$	$V_{ss}-0.3$	$0.2\ V_{cc}$	1.5	V	
V_{OH}	Output High Voltge	3.0V	$V_{cc}-0.4$		$V_{cc}-0.4$		3.0	V	$I_{OH} = -2.0\ mA$
		5.5V	$V_{cc}-0.4$		$V_{cc}-0.4$		4.8	V	$I_{OH} = -2.0\ mA$
$V_{OL}1$	Output Low Voltage	3.0V		0.8		0.8	0.2	V	$I_{OL} = +4.0\ mA$
		5.5V		0.4		0.4	0.1	V	$I_{OL} = +4.0\ mA$
$V_{OL}2$	Output Low Voltage	3.0V		TBD		TBD	1.0	V	$I_{OL} = +12\ mA$, 3 Pin Max
		5.5V		0.8		0.8	0.3	V	$I_{OL} = +12\ mA$, 3 Pin Max
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV	
		5.5V		25		25	10	mV	
V_{BO}	V_{cc} Brown Out Voltage		1.55	2.7	1.45	2.95	2.1	V	@ 2 MHz Max, Ext. CLK Freq
I_{IL}	Input Leakage (Input Bias Current of Comparator)	3.0V	-1.0	1.0	-1.0	1.0		μA	$V_{IN} = 0V, V_{cc}$
		5.5V	-1.0	1.0	-1.0	1.0		μA	$V_{IN} = 0V, V_{cc}$
I_{OL}	Output Leakage	3.0V	-1.0	1.0	-1.0	1.0		μA	$V_{IN} = 0V, V_{cc}$
		5.5V	-1.0	1.0	-1.0	1.0		μA	$V_{IN} = 0V, V_{cc}$

Symbol	Parameter	V_{cc}	$T_A = 0°C$ to 70°C		$T_A = -40°C$ to 105°C		Typical @ 25°C	Units	Conditions
			Min	Max	Min	Max			
I_{cc}	Supply Current (Standard Mode)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		7.0		7.0	3.0	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8.0		8.0	3.0	mA	All Output and I/O Pins Floating @ 8 MHz
		5.5V		11.0		11.0	6.0	mA	All Output and I/O Pins Floating @ 8 MHz
		3.0V		10		10	3.6	mA	All Output and I/O Pins Floating @ 12 MHz
		5.5V		15		15	9.0	mA	All Output and I/O Pins Floating @ 12 MHz
$I_{cc}1$	Standby Current (Standard Mode)	3.0V		2.5		2.5	0.7	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 2 MHz
		5.5V		4.0		5.0	2.5	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 2 MHz
		3.0V		4.0		4.0	1.0	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 8 MHz
		5.5V		5.0		5.0	3.0	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 8 MHz
		3.0V		4.5		4.5	1.5	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 12 MHz
		5.5V		7.0		7.0	4.0	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 12 MHz
I_{cc}	Supply Current (Low Noise Mode)	3.0V		3.5		3.5	1.5	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		7.0		7.0	3.0	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		5.8		5.8	3.0	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		9		9	6.0	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		8		8	3.6	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		11		11	9.0	mA	All Output and I/O Pins Floating @ 4 MHz

DC ELECTRICAL CHARACTERISTICS (Continued)
Z86E08

Symbol	Parameter	V_{cc}	$T_A = 0°C$ to 70°C Min	$T_A = 0°C$ to 70°C Max	$T_A = -40°C$ to 105°C Min	$T_A = -40°C$ to 105°C Max	Typical @ 25°C	Units	Conditions
$I_{cc}1$	Standby Current (Low Noise Mode)	3.0V		0.8		2.5	0.8	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 1 MHz
		5.5V		1		1	1	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 1 MHz
		3.0V		0.8		0.8	0.8	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 2 MHz
		5.5V		1		1	1	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 2 MHz
		3.0V		TBD		TBD	TBD	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 4 MHz
		5.5V		2.0		2.0	TBD	mA	HALT Mode $V_{IN} = 0V$, V_{cc} @ 4 MHz
$I_{cc}2$	Standby Current	3.0V		10		20	1.0	µA	STOP Mode $V_{IN} = 0V$, V_{cc} WDT is not Running
		5.5V		10		20	1.0	µA	STOP Mode $V_{IN} = 0V$, V_{cc} WDT is not Running
I_{ALL}	Auto Latch Low Current	3.0V		5.0		7.0	3.0	µA	$0V < V_{IN} < V_{cc}$
		5.5V		15		20	11	µA	$0V < V_{IN} < V_{cc}$
I_{ALH}	Auto Latch High Current	3.0V		-2.5		-4.0	-1.5	µA	$0V < V_{IN} < V_{cc}$
		5.5V		-7.0		-9.0	-5.0	µA	$0V < V_{IN} < V_{cc}$

Notes:

[1] $I_{cc}1$

	Type	Max	Unit	Freq
Clock Driven on Crystal	3.0	5.0	mA	8 MHz
or XTAL Resonator	0.3	50	mA	8 MHz

[2] $V_{ss} = 0V = GND$

[3] For 2.75V operating the device operates down to V_{BO}. The min operational V_{cc} is determined on the value of the voltage V_{BO} at the ambient temperature. The V_{BO} increases as the temperature decreases.
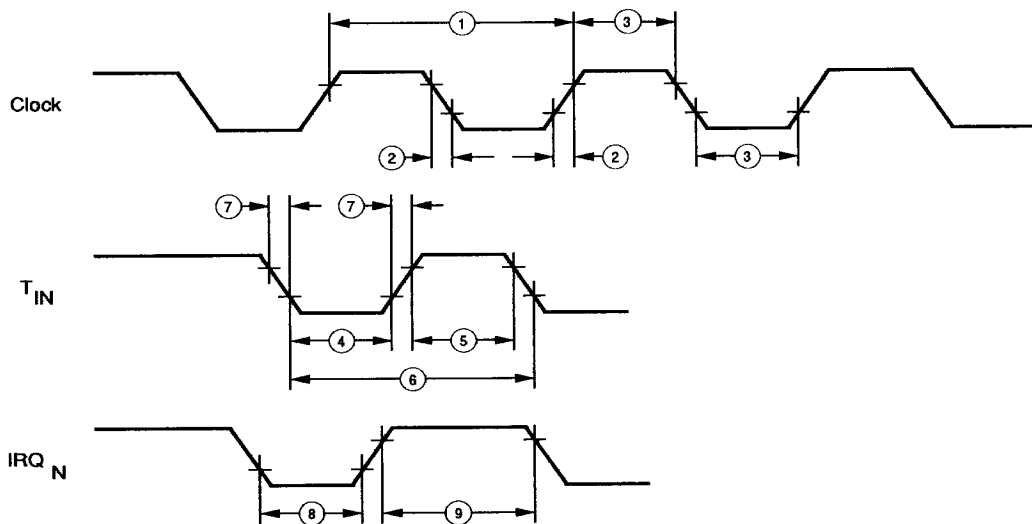
AC ELECTRICAL CHARACTERISTICS

Figure 20. Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS
Z86E08 (Low Noise Mode)

No	Symbol	Parameter	V_{cc}	$T_A = 0°C$ TO 70°C				$T_A = -40°C$ TO 105°C				Units	Notes
				1 MHz		4 MHz		1 MHz		4 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.3V	500		125	100,000	500	100,000	125	100,000	ns	[1]
			5.0V	500		125	100,000	500	100,000	125	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.3V		25		25		25		25	ns	[1]
			5.0V		25		25		25			ns	
3	TwC	Input Clock Width	3.3V	225		37		225		37		ns	[1]
			5.0V	225		37		225		37		ns	[1]
4	TwTinL	Timer Input Low Width	3.3V	100		100		100		100		ns	[1]
			5.0V	70		70		70		70		ns	[1]

25

AC ELECTRICAL CHARACTERISTICS (Continued)
Z86E08 (Low Noise Mode)

No	Symbol	Parameter	V_{cc}	$T_A = 0°C$ TO 70°C				$T_A = -40°C$ TO 105°C				Units	Notes
				1 MHz		4 MHz		1 MHz		4 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
5	TwTinH	Timer Input High Width	3.3V	1.5TpC		1.5TpC		1.5TpC		1.5TpC			[1]
			5.0V	1.5TpC		1.5TpC		1.5TpC		1.5TpC			[1]
6	TpTin	Timer Input Period	3.3V	4TpC		4TpC		4TpC		4TpC			[1]
			5.0V	4TpC		4TpC		4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.3V		100		100		100		100	ns	[1]
			5.0V		100		100		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.3V	100		100		100		100		ns	[1,2]
			5.0V	70		70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.3V	1.5TpC		1.5TpC		1.5TpC		1.5TpC			[1]
			5.0V	1.5TpC		1.5TpC		1.5TpC		1.5TpC			[1,2]
10	Twdt	Watchdog Timer Delay Time	3.3V		25		25		25		25	ms	[1]
			5.0V		15		15		15		15	ms	[1]

Notes:

[1] Timing Reference uses 0.9 V_{cc} for a logic "1" and 0.1 V_{cc} for a logic "0".
[2] Interrupt request via Port 3 (P31-P33)

AC ELECTRICAL CHARACTERISTICS
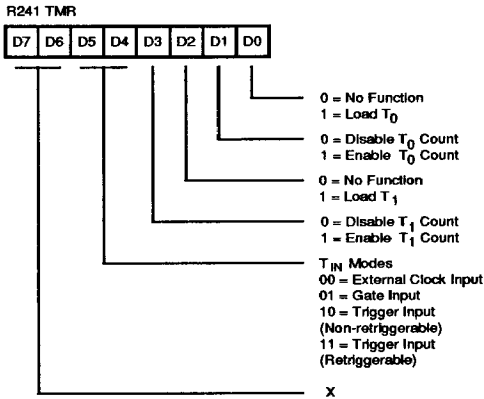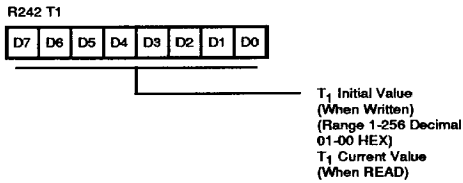Z86E08 (Standard Mode, Standard Temperature)

No	Symbol	Parameter	V_{cc}	$T_A = 0°C$ TO $70°C$						Units	Notes
				2 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	500		125	100,000	83	100,000	ns	[1]
			5.5V	500		125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25		15	ns	[1]
			5.5V		25		25		15	ns	
3	TwC	Input Clock Width	3.0V	225		37		26		ns	[1]
			5.5V	225		37		26		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		ns	[1]
			5.5V	70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC		3TpC			[1]
			5.5V	3TpC		3TpC		3TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100	ns	[1]
			5.5V		100		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		ns	[1,2]
			5.5V	70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC		3TpC			[1]
			5.5V	3TpC		3TpC		3TpC			[1,2]
10	Twdt	Watchdog Timer Delay Time	3.0V		25		25		25	ms	[1]
			5.5V		15		15		15	ms	[1]

Notes:

[1] Timing Reference uses 0.9 V_{cc} for a logic "1" and 0.1 V_{cc} for a logic "0".
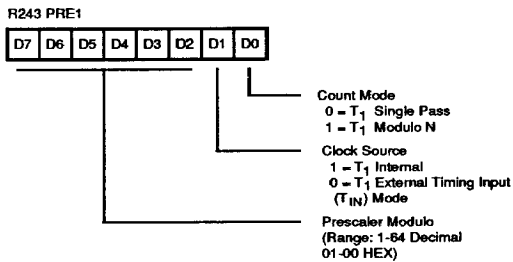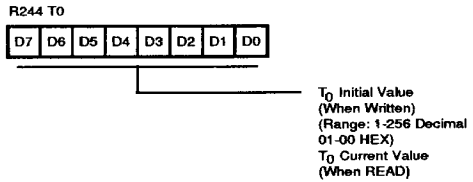[2] Interrupt request via Port 3 (P31-P33)

AC ELECTRICAL CHARACTERISTICS (CONTINUED)
Z86E08 (Standard Mode, Extended Temperature)

No	Symbol	Parameter	V_{cc}	T_A = 40°C TO 105°C						Units	Notes
				2 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	500	100,000	125	100,000	83	100,000	ns	[1]
			5.5V	500	100,000	125	100,000	83	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25		15	ns	[1]
			5.5V		25				15	ns	
3	TwC	Input Clock Width	3.0V	225		37		26			[1]
			5.5V	225		37		26		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		ns	[1]
			5.5V	70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC		3TpC			[1]
			5.5V	3TpC		3TpC		3TpC			[1]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC			[1]
			5.5V	8TpC		8TpC		8TpC			[1}
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100		100	ns	[1}
			5.5V		100		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		100		ns	[1,2]
			5.5V	70		70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC		3TpC			[1]
			5.5V	3TpC		3TpC		3TpC			[1,2]
10	Twdt	Watchdog Timer Delay Time	3.0V		25		25		25	ms	[1]
			5.5V		15		15		15	ms	[1]

Notes:

[1] Timing Reference uses 0.9 V_{cc} for a logic "1" and 0.1 V_{cc} for a logic "0".
[2] Interrupt request via Port 3 (P31-P33)

Z8 CONTROL REGISTER DIAGRAMS

R241 TMR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

0 = No Function
1 = Load T_0

0 = Disable T_0 Count
1 = Enable T_0 Count

0 = No Function
1 = Load T_1

0 = Disable T_1 Count
1 = Enable T_1 Count

T_{IN} Modes
00 = External Clock Input
01 = Gate Input
10 = Trigger Input
(Non-retriggerable)
11 = Trigger Input
(Retriggerable)

x

Figure 21. Timer Mode Register
($F1_H$: Read/Write)

R242 T1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

T_1 Initial Value
(When Written)
(Range 1-256 Decimal
01-00 HEX)
T_1 Current Value
(When READ)

Figure 22. Counter Timer 1 Register
($F2_H$: Read/Write)

R243 PRE1

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Count Mode
0 = T_1 Single Pass
1 = T_1 Modulo N

Clock Source
1 = T_1 Internal
0 = T_1 External Timing Input
(T_{IN}) Mode

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)

Figure 23. Prescaler 1 Register
($F3_H$: Write Only)

R244 T0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

T_0 Initial Value
(When Written)
(Range: 1-256 Decimal
01-00 HEX)
T_0 Current Value
(When READ)

Figrue 24. Counter/Timer 0 Register
($F4_H$: Read/Write)

R245 PRE0

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Count Mode
0 = T_0 Single Pass
1 = T_0 Modulo N

x

Prescaler Modulo
(Range: 1-64 Decimal
01-00 HEX)
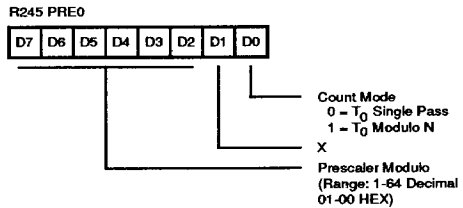
Figure 25. Prescaler 0 Register
($F5_H$: Write Only)

R246 P2M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

$P2_7$ - $P2_0$ I/O Definition
0 Defines Bit as OUTPUT
1 Defines Bit as INPUT
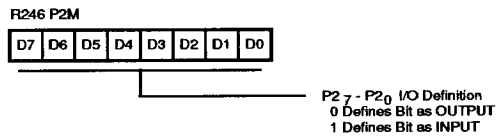
Figure 26. Port 2 Mode Register
($F6_H$: Write Only)

R247 P3M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

0 Port 2 Pull-Ups Open Drain
1 Port 2 Pull-Ups Active

Port 3 Inputs
0 Digital
1 Analog

x
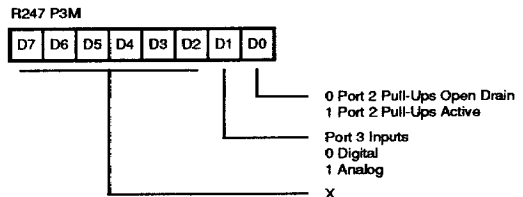
Figure 27. Port 3 Mode Register
($F7_H$: Write Only)

29

Z8 CONTROL REGISTER DIAGRAMS (Continued)

R248 P01M

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

$P0_3 - P0_0$ Mode
00 = Output
01 = Input

X

Must be 0

X
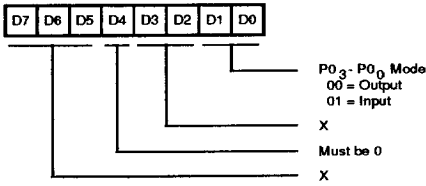
Figure 28. Port 0 and 1 Mode Register
($F8_H$: Write Only)

R249 IPR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Interrupt Group Priority
Reserved = 000
C > A > B = 001
A > B > C = 010
A > C > B = 011
B > C > A = 100
C > B > A = 101
B > A > C = 110
Reserved = 111

IRQ1, IRQ4 Priority (Group C)
0 = IRQ1 > IRQ4
1 = IRQ4 > IRQ1

IRQ0, IRQ2 Priority (Group B)
0 = IRQ2 > IRQ0
1 = IRQ0 > IRQ2

IRQ3, IRQ5 Priority (Group A)
0 = IRQ5 > IRQ3
1 = IRQ3 > IRQ5

0

Figure 29. Interrupt Priority Register
($F9_H$: Write Only)

R250 IRQ

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = P32 Input
IRQ4 = T0
IRQ5 = T1

Reserved

Figure 30. Interrupt Request Register
(FA_H: Read/Write)

R251 IMR

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

1 Enables IRQ0-IRQ5
(D_0 = IRQ0)

Reserved

1 Enables Interrupts

Figure 31. Interrupt Mask Register
(FB_H: Read/Write)

R252 Flags

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

User Flag F1
User Flag F2
Half Carry Flag
Decimal Adjust Flag
Overflow Flag
Sign Flag
Zero Flag
Carry Flag

Figure 32. Flag Register
(FC_H: Read/Write)

R253 RP

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Don't Care
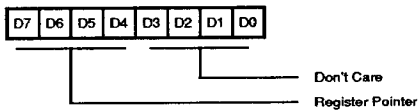
Register Pointer

Figure 33. Register Pointer
(FD_H: Read/Write)

R255 SPL

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Stack Pointer Lower
Byte ($SP_7 - SP_0$)
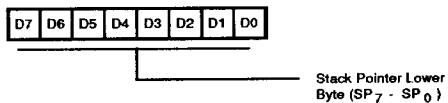
Figure 34. Stack Pointer
(FF_H: Read/Write)

30

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
–	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True	

INSTRUCTION FORMATS

One-Byte Instructions
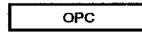
```
[      OPC      ]        CCF, DI, EI, IRET, NOP,
                        RCF, RET, SCF

[ dst |  OPC    ]
```

One-Byte Instructions

Two-Byte Instructions
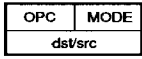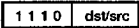
```
[ OPC | MODE ]                        CLR, CPL, DA, DEC,
[  dst/src   ]  OR [ 1 1 1 0 | dst/src ]  DECW, INC, INCW,
                                      POP, PUSH, RL, RLC,
                                      RR, RRC, SRA, SWAP

[    OPC     ]                        JP, CALL (Indirect)
[    dst     ]  OR [ 1 1 1 0 |  dst   ]

[    OPC     ]                        SRP
[   VALUE    ]

[ OPC | MODE ]                        ADC, ADD, AND, CP,
[ dst  | src ]                        OR, SBC, SUB, TCM,
                                      TM, XOR

[ MODE | OPC ]                        LD, LDE, LDEI,
[ dst/src | src/dst ]                 LDC, LDCI

[ dst/src | OPC ]                     LD
[    src/dst     ]  OR [ 1 1 1 0 | src ]

[ dst  | OPC ]                        LD
[   VALUE    ]

[ dst/CC | OPC ]                      DJNZ, JR
[     RA       ]

[    FFH     ]                        STOP/HALT
[ 6FH | 7FH  ]
```
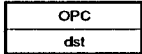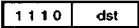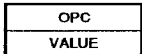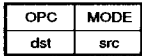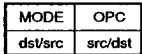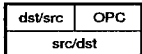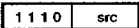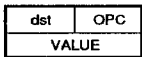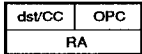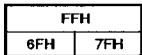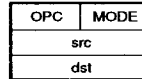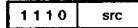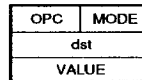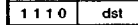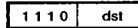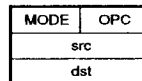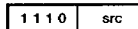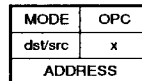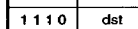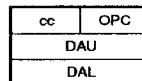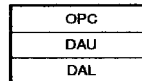
Two-Byte Instructions

Three-Byte Instructions

```
[ OPC | MODE ]                        ADC, ADD, AND, CP,
[    src     ]  OR [ 1 1 1 0 | src ]  LD, OR, SBC, SUB,
[    dst     ]  OR [ 1 1 1 0 | dst ]  TCM, TM, XOR

[ OPC | MODE ]                        ADC, ADD, AND, CP,
[    dst     ]  OR [ 1 1 1 0 | dst ]  LD, OR, SBC, SUB,
[   VALUE    ]                        TCM, TM, XOR

[ MODE | OPC ]                        LD
[    src     ]  OR [ 1 1 1 0 | src ]
[    dst     ]  OR [ 1 1 1 0 | dst ]

[ MODE | OPC ]                        LD
[ dst/src | x ]
[  ADDRESS   ]

[  cc  | OPC ]                        JP
[    DAU     ]
[    DAL     ]

[    OPC     ]                        CALL
[    DAU     ]
[    DAL     ]
```

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:
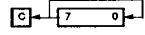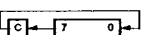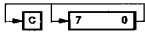
dst (7)

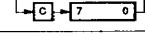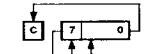refers to bit 7 of the destination operand.

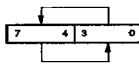| Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst, src dst←dst + src +C	†	1[ ]	* * * * 0 *
ADD dst, src dst←dst + src	†	0[ ]	* * * * 0 *
AND dst, src dst←dst AND src	†	5[ ]	- * * 0 - -
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR	D6 D4	- - - - - -
CCF C←NOT C		EF	* - - - - -
CLR dst dst←0	R IR	B0 B1	- - - - - -
COM dst dst←NOT dst	R IR	60 61	- * * 0 - -
CP dst, src dst - src	†	A[ ]	* * * * - -
DA dst dst←DA dst	R IR	40 41	* * * X - -
DEC dst dst←dst - 1	R IR	00 01	- * * * - -
DECW dst dst←dst - 1	RR IR	80 81	- * * * - -
DI IMR(7)←0		8F	- - - - - -
DJNZ r, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA	rA r = 0 - F	- - - - - -
EI IMR(7)←1		9F	- - - - - -
HALT		7F	- - - - - -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
INC dst dst←dst + 1	r R IR	rE r = 0 - F 20 21	- * * * - -
INCW dst dst←dst + 1	RR IR	A0 A1	- * * * - -
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1		BF	* * * * * *
JP cc, dst if cc is true PC←dst	DA IRR	cD c = 0 - F 30	- - - - - -
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA	cB c = 0 - F	- - - - - -
LD dst, src dst←src	r Im r R R r r X X r r Ir Ir r R R R IR R IM IR IM IR R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst, src	r Irr	C2	- - - - - -
LDCI dst,src r←r + 1;rr←rr + 1	Ir Irr	C3	- - - - - -
NOP		FF	- - - - - -
OR dst, src dst←dst OR src	†	4[ ]	- * * 0 - -

34

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
POP dst dst←@SP; SP←SP + 1	R IR	50 51	- - - - - -
PUSH src SP←SP - 1; @SP←src	R IR	70 71	- - - - - -
RCF C←0		CF	0 - - - - -
RET PC←@SP; SP←SP + 2		AF	- - - - - -
RL dst 	R IR	90 91	* * * * - -
RLC dst 	R IR	10 11	* * * * - -
RR dst 	R IR	E0 E1	* * * * - -
RRC dst 	R IR	C0 C1	* * * * - -
SBC dst, src dst←dst←src←C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst 	R IR	D0 D1	* * * 0 - -
SRP src RP←src	Im	31	- - - - - -
STOP		6F	- - - - - -

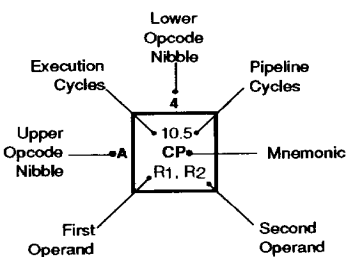| Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
SUB dst, src dst←dst←src	†	2[ ]	* * * * 1 *
SWAP dst 	R IR	F0 F1	X * * X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
XOR dst, src dst←dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst src		Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

35

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex) ↓ / Lower Nibble (Hex) →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1,r2	6.5 ADD r1,Ir2	10.5 ADD R2,R1	10.5 ADD IR2,R1	10.5 ADD R1,IM	10.5 ADD IR1,IM	6.5 LD r1,R2	6.5 LD r2,R1	12/10.5 DJNZ r1,RA	12/10.0 JR cc,RA	6.5 LD r1,IM	12.10.0 JP cc,DA	6.5 INC r1	
1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1,r2	6.5 ADC r1,Ir2	10.5 ADC R2,R1	10.5 ADC IR2,R1	10.5 ADC R1,IM	10.5 ADC IR1,IM								
2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1,r2	6.5 SUB r1,Ir2	10.5 SUB R2,R1	10.5 SUB IR2,R1	10.5 SUB R1,IM	10.5 SUB IR1,IM								
3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1,r2	6.5 SBC r1,Ir2	10.5 SBC R2,R1	10.5 SBC IR2,R1	10.5 SBC R1,IM	10.5 SBC IR1,IM								
4	8.5 DA R1	8.5 DA IR1	6.5 OR r1,r2	6.5 OR r1,Ir2	10.5 OR R2,R1	10.5 OR IR2,R1	10.5 OR R1,IM	10.5 OR IR1,IM								4.0 WDH
5	10.5 POP R1	10.5 POP IR1	6.5 AND r1,r2	6.5 AND r1,Ir2	10.5 AND R2,R1	10.5 AND IR2,R1	10.5 AND R1,IM	10.5 AND IR1,IM								5.0 WDT
6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1,r2	6.5 TCM r1,Ir2	10.5 TCM R2,R1	10.5 TCM IR2,R1	10.5 TCM R1,IM	10.5 TCM IR1,IM								6.0 STOP
7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1,r2	6.5 TM r1,Ir2	10.5 TM R2,R1	10.5 TM IR2,R1	10.5 TM R1,IM	10.5 TM IR1,IM								7.0 HALT
8	10.5 DECW RR1	10.5 DECW IR1														6.1 DI
9	6.5 RL R1	6.5 RL IR1														6.1 EI
A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1,r2	6.5 CP r1,Ir2	10.5 CP R2,R1	10.5 CP IR2,R1	10.5 CP R1,IM	10.5 CP IR1,IM								14.0 RET
B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1,r2	6.5 XOR r1,Ir2	10.5 XOR R2,R1	10.5 XOR IR2,R1	10.5 XOR R1,IM	10.5 XOR IR1,IM								16.0 IRET
C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1,Irr2	18.0 LDCI Ir1,Irr2				10.5 LD r1,x,R2								6.5 RCF
D	6.5 SRA R1	6.5 SRA IR1			20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1								6.5 SCF
E	6.5 RR R1	6.5 RR IR1		6.5 LD r1,IR2	10.5 LD R2,R1	10.5 LD IR2,R1	10.5 LD R1,IM	10.5 LD IR1,IM								6.5 CCF
F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1,r2	10.5 LD R2,IR1											6.0 NOP

Bytes per Instruction: 2 (columns 0–3), 3 (columns 4–7), 2 (columns 8–B), 3 (columns C–E), 1 (column F)

Execution Cycles — Lower Opcode Nibble — Pipeline Cycles
Upper Opcode Nibble — A — 10.5 CP — Mnemonic
R1, R2
First Operand — Second Operand

Legend:
R = 8-bit address
r = 4-bit address
R or r = Dst address
R 1 or r 2 = Src address
   1   2
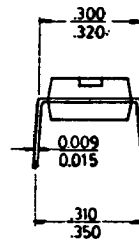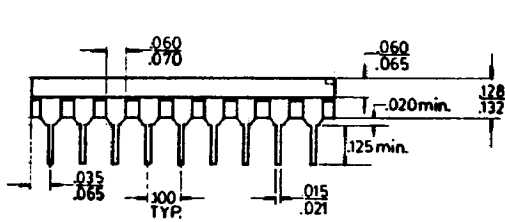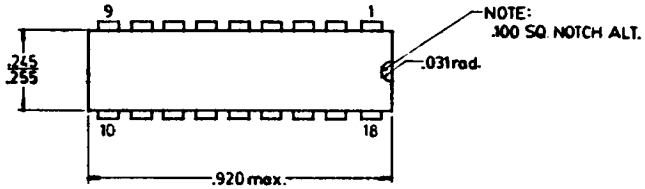**Sequence:**
Opcode, First Operand,
Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a
  3-byte instruction

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PACKAGE INFORMATION

18-Pin Plastic Package

ORDERING INFORMATION

Z86E08

2 MHz	8 MHz	12 MHz
Z86E0802PSC	Z86E0808PSC	Z86E0812PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package
P = Plastic DIP
V = Plastic Chip Carrier
C = Ceramic DIP
L = Ceramic LCC

Longer Lead Time
F = Plastic Quad Flat Pack

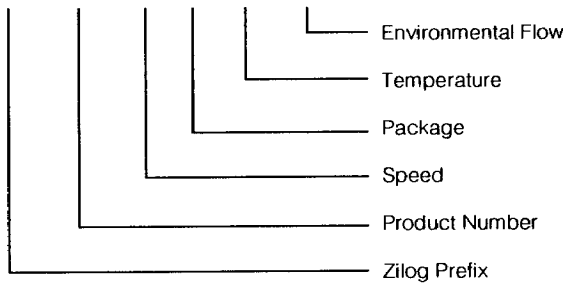**Temperature**
E = -40°C to +100°C
S = 0°C to + 70°C

Speed
04 = 4 MHz

Environmental
C = Plastic Standard

Example:

Z   86E08   04   P   S   C   is an 86E08 4 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

└──────────── Environmental Flow

└──────────── Temperature

└──────────── Package

└──────────── Speed

└──────────── Product Number

└──────────── Zilog Prefix

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