Am79C401

Integrated Data Protocol Controller (IDPC)

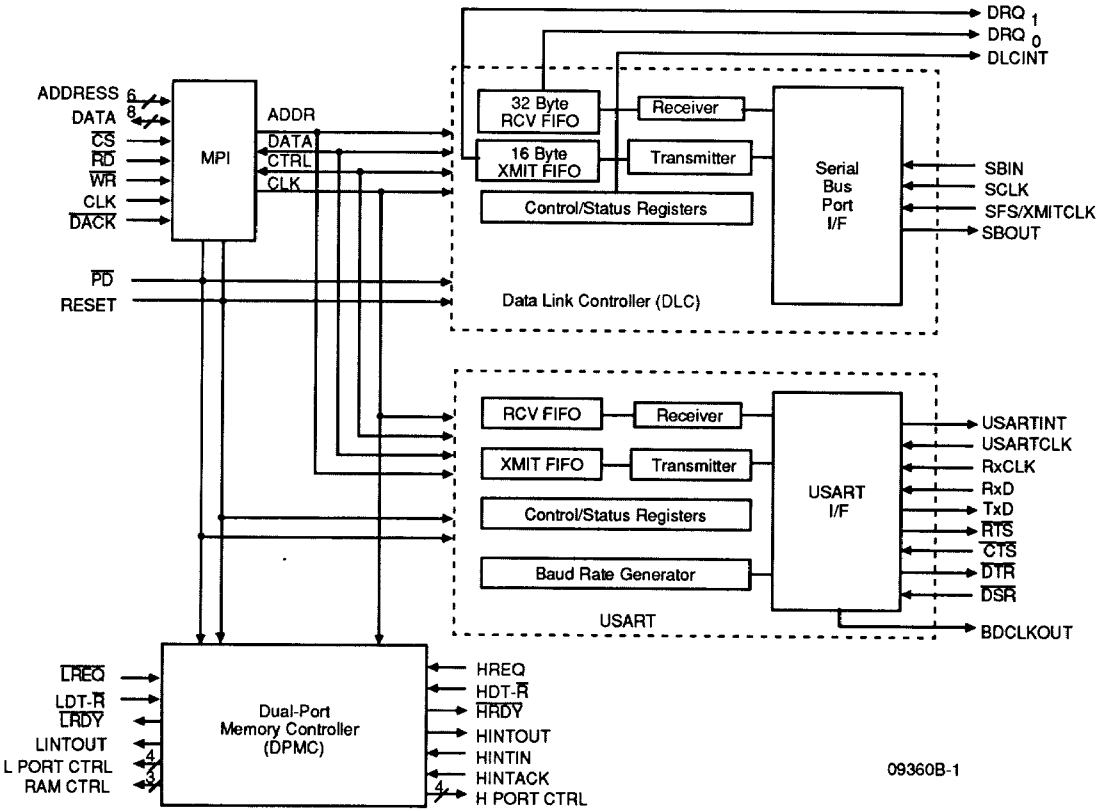
Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

Data Link Controller

- Full-featured bit-oriented communication controller supporting HDLC, SDLC, LAPB, LAPD, and DMI
- Data transfer rate: 2.048 Mb/s
- 32-byte receive FIFO and 16-byte transmit FIFO with programmable thresholds and DMA handshakes
- Multiple (four plus broadcast) address recognition modes
- Multiplexed serial interface with up to 31 8-bit channels or non-multiplexed serial interface
- Local and Remote Loopback Modes
- Transparent (Protocol-Free) Mode
- 56 kb/s Mode

BLOCK DIAGRAM



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DISTINCTIVE CHARACTERISTICS (continued)

USART

- Superset of Industry-Standard 8250 UART features
- Four-byte transmit/receive FIFOs
- Special character recognition (up to 128 programmable)
- Synchronous mode provides a transparent serial data path
- Local Loopback mode

Dual-Port Memory Controller

- Memory bus arbitrator provides dual-port access to standard low-cost static RAM
- Programmable inter-processor interrupts support RAM-based inter-processor mailboxes

Microprocessor Interface

- 8-bit non-multiplexed data bus
- Operates with 12.5 MHz 80188 processor with zero wait states

General Features

- Compatible with Am79C30A DSC and Am79C32A IDC
- CMOS technology, single +5 V supply
- Power-down mode
- 68-pin PLCC

GENERAL DESCRIPTION

The Am79C401 Integrated Data Protocol Controller (IDPC) and companion software product, the Am79LLD401 IDPC Low-Level Driver (LLD), provide the essential building blocks for construction of a variety of communications systems. When combined with ROM, RAM, a microprocessor, and the physical layer transceiver, a complete ISDN, X.25, SNA, or similar system can be constructed. The IDPC is design-compatible with existing AMD communication components such as the Am79C30A Digital Subscriber Controller (DSC) and Am79C32A ISDN Data Controller (IDC) and off-the-shelf microprocessors such as the 80188.

The IDPC contains hardware and software support features for use in a single-processor environment (such as a terminal adapter for an ISDN network) or a multiprocessor application (such as a communication interface for a PC or integrated voice/data work station application). For multi-processor applications, the IDPC controls access to an external "shared" static RAM by arbitrating simultaneous shared memory requests and supports an interprocessor interrupt scheme.

A companion software product, the Am79LLD401 IDPC LLD, provides isolation of the various hardware functions from the higher levels of packet protocol software. The LLD can be used with any bit-oriented protocol, including AmLink™, which is AMD's LAPD/LAPB implementation. Additionally, AMD's AmLink3™ package offers a complete implementation of the X.25 Packet Layer (Layer 3) protocol.

For ISDN D-channel applications, a similar function is provided by the Am79C30A DSC and Am79LLD30A LLD software.

The interfaces presented by the Am79LLD30A DSC LLD and the Am79LLD401 IDPC LLD use the same primitives so that both the D-channel and the B-channel can use the same layer-2 software. Both LLDs provide a hardware-independent interface to upper-layer protocols such as AmLink LAPD.

Functionally, the IDPC consists of four sections: a Data Link Controller (DLC), a Universal Synchronous/Asynchronous Receiver/Transmitter (USART), a Dual-Port Memory Controller (DPMC), and a Microprocessor Interface (MPI).

Data Link Controller (DLC)

The DLC shown in the Block Diagram is a high-speed, bit-oriented protocol processor that supports either multiplexed or non-multiplexed data rates up to 2.048 Mb/s.

The DLC provides full-duplex (simultaneous transmit and receive) data transfer between the chip's Serial Bus Port (SBP) and internal parallel bus. Through the use of a 32-byte receive FIFO, a 16-byte transmit FIFO, and two external DMA channels, the DLC provides efficient movement of data to and from external memory and the SBP (network interface).

The DLC supports data transfers via DMA, interrupts, or polled I/O. The use of the FIFO buffers minimizes interrupt latency and frequency of interrupts.

The DLC has several programmable modes of operation which include:

- Non-multiplexed mode
- Multiplexed mode
- Local/Remote Test modes
- Transparent (Protocol-Free) Mode
- 56 kb/s Mode

Non-multiplexed Mode

In non-multiplexed mode, the DLC functions as a conventional serial communications controller capable of supporting full-duplex data transfers at rates up to 2.048 Mb/s. This mode is useful in non-ISDN applications such as Local Area Networks, personal computer networks, Host-to-Host or terminal-to-Host applications.

Multiplexed Mode

In multiplexed mode, the DLC's SBP interfaces cleanly with the SBP on the Am79C30A DSC or the Am79C32A IDC, and provides access to 31 64 kb/s time slots.

Local/Remote Loopback Test Modes

The DLC can be placed in either local or remote loopback mode under software control. In local loopback, the transmitter output is tied back to the receiver input. In remote loopback, the receiver input from the network is transmitted back to the network for system test purposes.

Transparent Mode

In Transparent Mode, the DLC receives and transmits data without performing any HDLC protocol processing, creating a clear path between the SBP and the transmit and receive FIFOs. This mode can be used in either multiplexed or non-multiplexed modes.

56 kb/s Mode

In 56 kb/s Mode, the DLC transmits and receives data at a 56 kb/s data rate. In this mode, the DLC sends data within an 8-bit time slot period, and always pulls the SBOUT pin High during the transmit time period of the eighth bit. Similarly, during data reception, the DLC shifts in 7 bits during the programmed time slot, but always waits until eight bits have been accumulated before transferring the data to the receive FIFO.

Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The IDPC contains a USART for exchanging data between RS232 type terminals and the ISDN network in applications where there is no host processor. The USART provides a superset of 8250 UART features and supports both synchronous and asynchronous serial communications. The USART is capable of full-duplex operation at speeds up to 64 kb/s.

The USART supports the following functions:

- Programmable synchronous/asynchronous modes
- Software reset
- Line break recognition and generation
- Special character recognition
- Selectable stop bits (1-, 1.5-, or 2-stop bits)
- Modem control handshake lines ($\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, and $\overline{DTR}$)
- Local loopback and "stick parity" test features

The USART receiver can detect up to 128 user-identified special characters. As each character is received, it is tested. If it is identified as a special character, a maskable interrupt can be generated.

The USART includes an internal Baud Rate Generator (BRG) that provides a clock for the transmitter and receiver sections (and to the external pin BDCLKOUT). The Baud Rate Generator's data rate is programmed by loading two "divisor latches" under software control.

Dual-Port Memory Controller (DPMC)

The DPMC provides access control and an inter-processor interrupt mechanism that permits two processors to share static RAM memory without the expense of dual-port RAM. These features are necessary in developing network interface applications for PCs and Integrated Voice/Data Workstations (IVDWs).

In a typical multi-processor application, a local processor (such as the 80188) exchanges data with the host processor in the PC or IVDW using shared memory. The DPMC performs RAM access arbitration between the local and host processors, allowing the static RAM to appear as a dual-port memory to each processor.

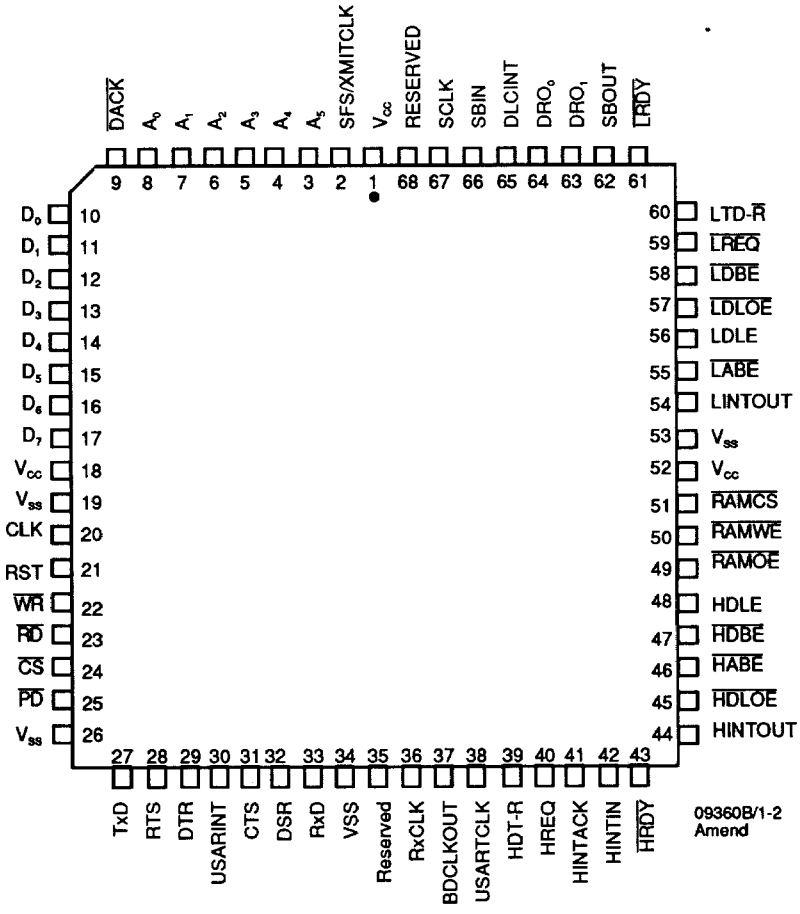
The local processor can access any device on the IDPC local bus. The host processor can only access the RAM on the IDPC local bus. Any contention between the local processor and the host processor is arbitrated by the DPMC on the IDPC. Both processors communicate via memory-resident data buffers and mailboxes. An interprocessor interrupt scheme notifies the other processor when one of the processors has written data to a buffer or a command to a mailbox.

Microprocessor Interface (MPI)

The MPI consists of an 8-bit non-multiplexed data bus that allows the IDPC to function with a 12.5-MHz 80188 processor (or other similar microprocessor) with zero wait-states.

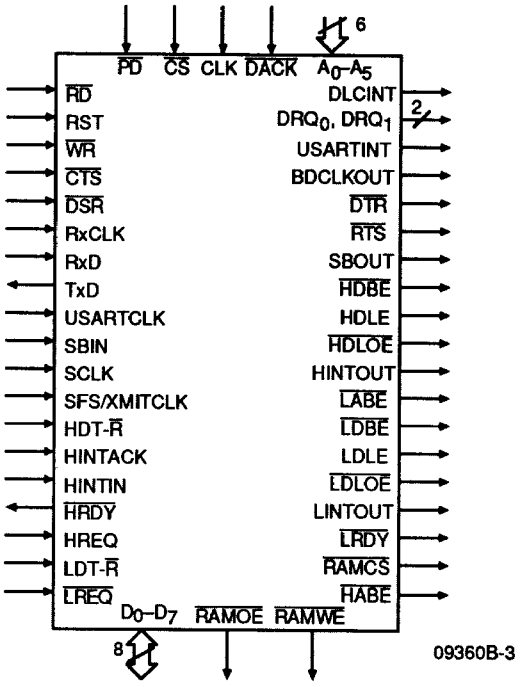
CONNECTION DIAGRAM
Top View

PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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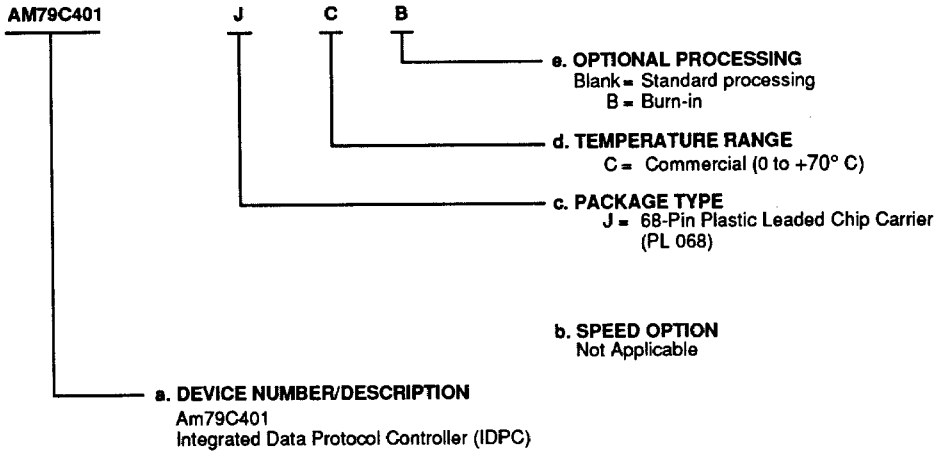
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C401	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

The interface pins of the 68-pin IDPC chip can be classified into six major groups:

Processor Bus Interface	(25 pins)
USART Interface	(9 pins)
Serial Bus Port Interface	(4 pins)
Bus Arbitration Control	(21 pins)
Power/Ground	(7 pins)
No Connects (Reserved)	(2 pins)

Unless otherwise specified, all input pins are TTL compatible.

Processor Bus Interface

A_5–A_0 Address Lines (Input)

These six address lines are generated by the external processor to select internal registers of the IDPC, and are valid only when $\overline{CS}$ is active Low.

$\overline{DACK}$ DMA Acknowledge (Input; Active Low)

The $\overline{DACK}$ signal is an indication that the DMA Controller is executing a DMA cycle to the DLC transmit FIFO. This indication occurs early in the DMA cycle, allowing the transmit FIFO to deactivate the DRQ_1 signal when the last data transfer takes place (before an unwanted DMA cycle is initiated). An equivalent signal is not required for the DLC receive FIFO operation.

CLK Master Clock (Input)

The Master Clock is an input that provides synchronization and timing for internal IDPC logic functions. CLK is normally the same clock used by the CPU.

$\overline{CS}$ Chip Select (Input; Active Low)

$\overline{CS}$ is an input that indicates the IDPC has been selected for a read or write cycle.

D7–D0 Data Lines (Input/Output; Three State)

D7–D0 are bidirectional data lines used to transfer data between the local processor and the IDPC. The direction of the data transfer is controlled by the $\overline{RD}$ and $\overline{WR}$ control lines. When $\overline{CS}$ is inactive High, the data lines remain in a high-impedance state.

DLCINT DLC Interrupt (Output; Active High)

DLCINT goes active High when the IDPC's DLC sets a status bit and the associated interrupt enable bit is set, and remains active until all pending DLC interrupts are cleared.

DRQ_0 Receive DMA Request (Output; Active High)

DRQ_0 is an output signal used by the DLC's receive FIFO to begin a DMA cycle for received data.

DRQ_0 goes active High under the following conditions:

1) when number of bytes transferred into the receive FIFO equals the number specified in the DLC FIFO Threshold Register, or
2) when an "end of packet" byte is loaded into the receive FIFO.

DRQ_0 is deactivated Low under the following conditions:

1) Reset
2) when the receive FIFO becomes empty, or
3) when the last byte of a packet is transferred from the receive FIFO to external memory.

DRQ_1 Transmit DMA Request (Output; Active High)

DRQ_1 is an output signal used by the DLC's transmit FIFO to request the start of a DMA cycle for the transmit data.

DRQ_1 goes active High when ALL of the following conditions are met:

1) the transmit byte count is not equal to zero,
2) last byte of the packet has not been loaded into the transmit FIFO, and
3) number of bytes in the FIFO is equal to or less than the value programmed in the transmit FIFO Threshold.

DRQ_1 is deactivated Low under the following conditions:

1) Reset,
2) when the transmit FIFO is full, or
3) when the last byte of the packet is loaded into the transmit FIFO.

$\overline{PD}$ Power Down (Input; Active Low)

This signal disables all internal clocks and places all three-state signals in a high-impedance state. $\overline{HRDY}$ and $\overline{LRDY}$ are disabled and all interrupt outputs are deactivated. Status and data will be lost but programming is retained. $\overline{PD}$ should be held active for a period of 8 MCLK cycles.

$\overline{RD}$ Read (Input; Active Low)

This input is used by the IDPC to indicate when data from the IDPC is being requested.

$\overline{RD}$ is qualified internally with an active Low $\overline{CS}$.

RST Reset (Input; Active High)

This input forces all functions to terminate and places the IDPC in a default state. $\overline{HRDY}$ and $\overline{LRDY}$ are disabled and all three-state outputs are placed in a high-impedance state. RST should be held active for a period of 8 MCLK cycles.

USARTINT USART Interrupt (Output; Active High)

USARTINT goes active High when the IDPC's USART sets a status bit and the associated interrupt enable bit is

active, and remains active until all pending USART interrupts are cleared.

$\overline{WR}$ Write (Input; Active Low)

$\overline{WR}$ is used by the IDPC to latch incoming data (D_7–D_0) during a write cycle.

$\overline{WR}$ is qualified internally with an active Low $\overline{CS}$.

USART Interface

BDCLKOUT Baud Rate Generator Clock Out (Output)

This signal is the output of the USART's Baud Rate Generator, and can be used as a common clocking source for a modem or other similar device.

$\overline{CTS}$ Clear To Send (Input; Active Low)

Activity on $\overline{CTS}$ generates a maskable interrupt, but does not directly control the USART's transmitter.

$\overline{DSR}$ Data Set Ready (Input; Active Low)

Activity on $\overline{DSR}$ generates a maskable interrupt, but does not directly control the USART's transmitter or receiver.

$\overline{DTR}$ Data Terminal Ready (Output; Active Low)

$\overline{DTR}$ is user-controlled and does not directly control the USART's transmitter or receiver.

$\overline{RTS}$ Request To Send (Output; Active Low)

$\overline{RTS}$ is user-controlled and does not directly control the USART's transmitter.

RxCLK Receive Clock (Input)

RxCLK is an input to the USART and is used in synchronous and asynchronous operation. In asynchronous mode, the RxCLK should be 16 times the data rate. In synchronous mode, RxCLK is synchronized to the incoming data, and the rising edge is used to latch data on the RxD pin. The maximum data rate supported is 64 kb/s.

RxD Receive Data (Input; Active High)

RxD is an input to the USART. Data on this pin is clocked into the IDPC on the rising edge of the selected clock source.

TxD Transmit Data (Output; Active High)

TxD is an output of the USART. Data is clocked out of the IDPC on the falling edge of the selected clock source.

USARTCLK USART Clock (Input)

This pin is the clock input for the USART's Baud Rate Generator. The frequency of this clock source must be an integer multiple of the desired baud rate (output of the Baud Rate Generator is the same as the data rate for synchronous operation and 16 times the data rate for asynchronous operation). If the Baud Rate Generator is programmed to divide by one, USARTCLK operates as a direct input to the USART. When the IDPC is used in conjunction with the Am79C30 (DSC), the 12.288-MHz clock output can be used as the USART clock source. The maximum data rate supported is 64 kb/s.

Serial Bus Port Interface

SBIN Serial Data In (Input)

SBIN is the serial data input to the IDPC's DLC. Data is clocked into the DLC, LSB (bit 0) first, on the rising edge of SCLK. The maximum data rate supported is $^1/_5$ of clock supplied via the CLK pin. This data rate, however, should not exceed 2.048 Mb/s.

In applications where an Am79C30A (DSC) is used, SBIN can be tied to the SBOUT pin of the DSC directly.

SBOUT Serial Data Out (Output; Open Drain)

SBOUT is the serial data output of the IDPC's DLC. Data is clocked out, LSB (bit 0) first, on the falling edge of either SCLK or SFS/XMITCLK. SBOUT data rate may range from 0 to 2.048 Mb/s. In applications where an Am79C30A (DSC) is used, SBOUT of the IPDC is tied to SBIN of the DSC with a pullup resistor.

SCLK Serial Clock In (Input)

SCLK is used as the clocking source for the DLC.

In multiplexed mode, SCLK supplies both the transmit and receive clocks synchronized to SFS/XMITCLK. In non-multiplexed mode, SCLK is used as the receive clock and is not synchronized to SFS/XMITCLK. The rising edge of SCLK is used to latch data on SBIN and the falling edge is used to shift data out on SBOUT in multiplexed mode. The maximum data rate supported is 1/5 of clock supplied via the CLK pin. This data rate, however, should not exceed 2.048 Mb/s.

SFS/XMITCLK Serial Frame Sync/Transmit Clock (Input)

This input clock signal has two different functions depending on the mode of operation selected by bits 4–0 in the DLC SBP Control Register. In multiplexed mode, this input pin functions as SFS, the synchronization pulse used to indicate the first of up to 31 independent 8-bit time slots on SBIN and SBOUT.

In non-multiplexed mode, SFS/XMITCLK is used by the DLC as the input for an independent transmit clock. SFS/XMITCLK is used by the DLC to shift data out onto SBOUT, LSB (bit 0) first, on the falling edge. This clock operates from 0 to 2.048 MHz.

Bus Arbitration Control

$\overline{HDBE}$ Host Data Bus Enable (Output; Active Low)

$\overline{HDBE}$ is an active Low output used to enable the data bus lines from the host processor to the shared RAM data bus. $\overline{HDBE}$ is driven active as a result of HDT-$\overline{R}$

being sampled High (write cycle) and remains High until the end of the memory cycle.

$\overline{\text{HABE}}$ Host Address Bus Enable (Output; Active Low)

$\overline{\text{HABE}}$ is driven active Low by the IDPC as a result of receiving an HREQ from the host processor and is used to enable the address lines from the host processor and remains active until the end of the memory cycle.

HDLE Host Data Latch Enable (Output; Active High)

This active High output is used to latch data from shared RAM to the host processor. HDLE is driven High as a result of HDT-$\overline{\text{R}}$ being sampled Low. HDLE returns Low at the end of the memory cycle.

$\overline{\text{HDLOE}}$ Host Data Latch Output Enable (Output; Active Low)

This active Low output is used by the host processor to enable the output of the data bus latches to the host processor. $\overline{\text{HDLOE}}$ is driven Low when HDT-$\overline{\text{R}}$ is sampled Low. It is deactivated when HREQ goes inactive Low.

HDT-$\overline{\text{R}}$ Host Data Transmit-Receive (Input)

HDT-$\overline{\text{R}}$ indicates whether a read or write cycle takes place to shared memory from the host processor. When HDT-$\overline{\text{R}}$ is sampled High, it indicates that a shared RAM write cycle is in progress. As a result, $\overline{\text{RAMWE}}$ and $\overline{\text{HDBE}}$ are driven active Low .

When HDT-$\overline{\text{R}}$ is sampled Low, a shared RAM read cycle occurs and $\overline{\text{RAMOE}}$ and $\overline{\text{HDLOE}}$ are driven active Low, and HDLE is driven active High .

HINTACK Host Interrupt Acknowledge (Input; Active High)

HINTACK is generated by the host processor in response to a Host Interrupt Out signal (HINTOUT) from the IDPC. HINTACK is used to clear bit 0 of the Semaphore Register, and deactivate the HINTOUT signal Low.

HINTIN Host Interrupt In (Input; Active High)

This signal is used by the host processor to generate an interrupt to the local processor via the LINTOUT pin. When the host processor pulses this pin High, bit 1 of the Semaphore Register is set to '1' and LINTOUT is driven active High.

HINTOUT Host Interrupt Out (Output; Active High)

HINTOUT is used to generate an interrupt to the host processor. This signal goes active High when the local processor sets bit 0 of the Semaphore Register to '1'. HINTOUT is deactivated Low by a pulse on the HINTACK pin or by Reset.

$\overline{\text{HRDY}}$ Host Ready (Output; Active Low; Open Drain)

$\overline{\text{HRDY}}$ is an output from the IDPC used by the host processor to complete a shared RAM memory cycle. $\overline{\text{HRDY}}$ is normally High. It is pulled Low when a request for shared RAM is received from the host processor (HREQ) and is returned High at the end of the memory cycle, or by Reset.

HREQ Host Processor Bus Request (Input; Active High)

The HREQ is a active High input to the IDPC from the host processor requesting access to the shared RAM. HREQ is sampled on the falling edge of every IDPC Master clock cycle. When sampled active, HREQ drives $\overline{\text{RAMCS}}$ and $\overline{\text{HABE}}$ active Low, and $\overline{\text{HRDY}}$ active Low. HREQ is an asynchronous input with respect to the IDPC's Master Clock and is synchronized internally.

$\overline{\text{LABE}}$ Local Address Bus Enable (Output; Active Low)

This signal is driven Low by the IDPC to enable the address lines from the local processor bus onto the shared memory bus when a Local Processor Bus Request ($\overline{\text{LREQ}}$) is received from the local processor. $\overline{\text{LABE}}$ remains active Low until the end of the memory cycle.

$\overline{\text{LDBE}}$ Local Data Bus Enable (Output; Active Low)

This signal is used to place the data from the local processor bus onto the shared RAM data bus. $\overline{\text{LDBE}}$ is driven active Low as a result of LDT-$\overline{\text{R}}$ being sampled High. $\overline{\text{LDBE}}$ remains Low until the end of a memory cycle.

LDLE Local Data Latch Enable (Output; Active High)

This signal is driven High to latch data from shared RAM onto the local processor data bus. LDLE is driven High as a result of LDT-$\overline{\text{R}}$ being sampled Low, and is deactivated Low at the end of a memory cycle.

$\overline{\text{LDLOE}}$ Local Data Latch Output Enable (Output; Active Low)

This signal is an active Low output from the IDPC that enables the output of the data bus latch onto the local processor. $\overline{\text{LDLOE}}$ is driven active Low when LDT-$\overline{\text{R}}$ is sampled Low, and is cleared when $\overline{\text{LREQ}}$ goes inactive High.

LDT-$\overline{\text{R}}$ Local Data Transmit-Receive (Input)

LDT-$\overline{\text{R}}$ indicates whether a read or write cycle takes place to shared memory from the local processor. When this signal is sampled High, a shared RAM write cycle occurs. As a result, $\overline{\text{RAMWE}}$ and $\overline{\text{LDBE}}$ are driven active Low.

When LDT-$\overline{R}$ is sampled Low, a shared RAM read cycle occurs, $\overline{RAMOE}$ and $\overline{LDLOE}$ are driven active Low, and LDLE is driven active High .

LINTOUT Local Interrupt Out (Output; Active High)

LINTOUT is driven active High when the HINTIN pin is pulsed high by the host processor, and goes Low when bit 1 in the Semaphore Register is cleared to "0" by software, or after a Reset.

$\overline{LRDY}$ Local Ready (Output; Active Low; Open Drain)

$\overline{LRDY}$ is an active Low output from the IDPC used by the local processor to complete a shared RAM memory cycle. $\overline{LRDY}$ is normally High, and is driven Low when a request for shared RAM is received from the local processor ($\overline{LREQ}$) and the host processor is currently accessing shared RAM.

$\overline{LREQ}$ Local Processor Bus Request (Input; Active Low)

This active Low signal is an input to the IDPC from the local processor when it requests access to the shared RAM. $\overline{LREQ}$ is sampled on the falling edge of every IDPC Master Clock cycle.

$\overline{LREQ}$ must be synchronous to CLK.

$\overline{RAMCS}$ RAM Chip Select (Output; Active Low)

This signal is an active Low output from the IDPC used by the shared RAM as its chip select. $\overline{RAMCS}$ is a driven Low when either $\overline{LREQ}$ or HREQ is sampled active. $\overline{RAMCS}$ remains active until the end of a memory cycle.

$\overline{RAMOE}$ RAM Output Enable (Output; Active Low)

This signal is an active Low output signal from the IDPC used by the shared RAM to enable its output drivers. $\overline{RAMOE}$ is driven active Low when either LDT-$\overline{R}$ or HDT-$\overline{R}$ is sampled Low and is deactivated High at the end of the memory cycle.

$\overline{RAMWE}$ RAM Write Enable (Output; Active Low)

This signal is an active Low output from the IDPC used by the shared RAM as a write strobe. $\overline{RAMWE}$ is driven Low when either LDT-$\overline{R}$ or HDT-$\overline{R}$ is sampled High and remains active until the end of a memory cycle.

Power/Ground

V_{CC} +5 V Power Supply

V_{SS} Ground

FUNCTIONAL DESCRIPTION

IDPC Block Diagram Description

The IDPC contains three major functional modules which include:

- Data Link Controller (DLC)
- Universal Synchronous/Asynchronous Receiver/ Transmitter (USART)
- Dual-Port Memory Controller (DPMC)

Data Link Controller (DLC)

The DLC consists of a transmitter, receiver, and of Control/Status registers (Figure 1).

DLC Transmitter

The transmitter resides between the IDPC's parallel bus and the serial communication network. The local processor builds a data block in memory containing the address, control, and information fields of an HDLC frame. This block of data is then moved into the transmit FIFO under either DMA or programmed I/O control.

The transmitter functions include: opening flag transmission, data transparency (via zero insertion), generation and transmission of the Frame Check Sequence (FCS) characters (if enabled), and transmission of the closing flag.

The transmitter may also be programmed to perform such functions as inverting the polarity of the data stream, transmitting an abort sequence, and transmitting an all "1s" pattern (Mark Idle) or back-to-back flags (Flag Idle) between packets.

A block diagram of the DLC transmitter is shown in Figure 2.

Transmit FIFO—The transmit FIFO consists of a 16-byte FIFO buffer, transmit byte count register, transmit byte counter, and DMA request logic. Data can be loaded into the transmit FIFO under programmed I/O or Direct Memory Access (DMA) control.

Data Register—The "user-addressable" portion of the FIFO is termed the data register. The transmit FIFO sets bit 3 (XMIT BUFFER AVAIL) in the FIFO Status Register to "1" to indicate when the Data Register is available. This bit is set any time the Data Register is empty, and is cleared when the Data Register is written to and the FIFO becomes full or the last byte of a packet is loaded into the FIFO.

Parallel-to-Serial Shift Register—The output of the transmit FIFO is loaded one byte at a time into the parallel-to-serial shift register then shifted out to the zero bit insertion logic before appearing at the SBOUT pin.

Flag and abort characters are loaded into the parallel-to-serial shift register for transmission by the DLC when a flag or abort sequence is to be sent. During the transmission of a flag or abort sequence the zero bit insertion logic is disabled.

Bit Residue—The transmitter also has provisions for handling bit-residue. Bit-residue refers to the number of bits left over after the I (Information) field of a frame (excluding inserted zeros) is divided into 8-bit bytes. Protocols such as LAPD and SDLC specify that data be sent in 8-bit quantities. In HDLC, however, the information field can be any number of bits and not necessarily an integral number of 8-bit characters. On the IDPC a programmable 3-bit field is provided that specifies the number of valid data bits received or transmitted during the last byte of a frame. Transmitting packets with bit-residue I-fields requires that the user load a 3-bit register field (Residue Bit Status Control Register) with the number of residue

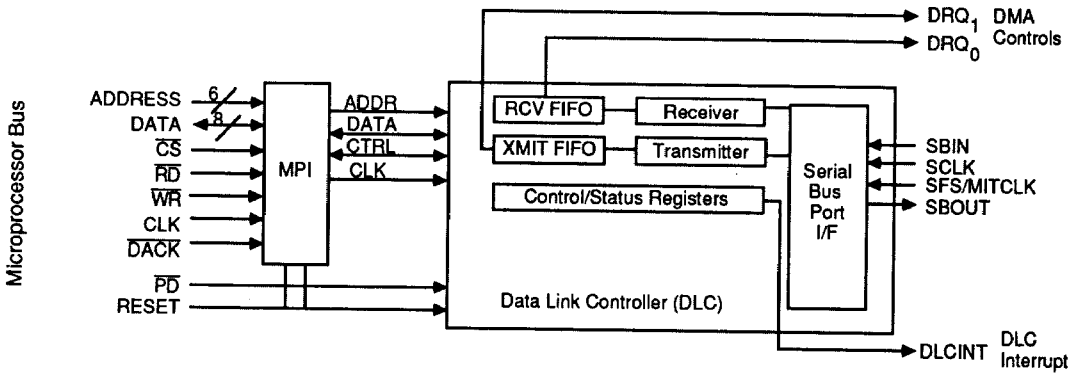


Figure 1. DLC Block Diagram

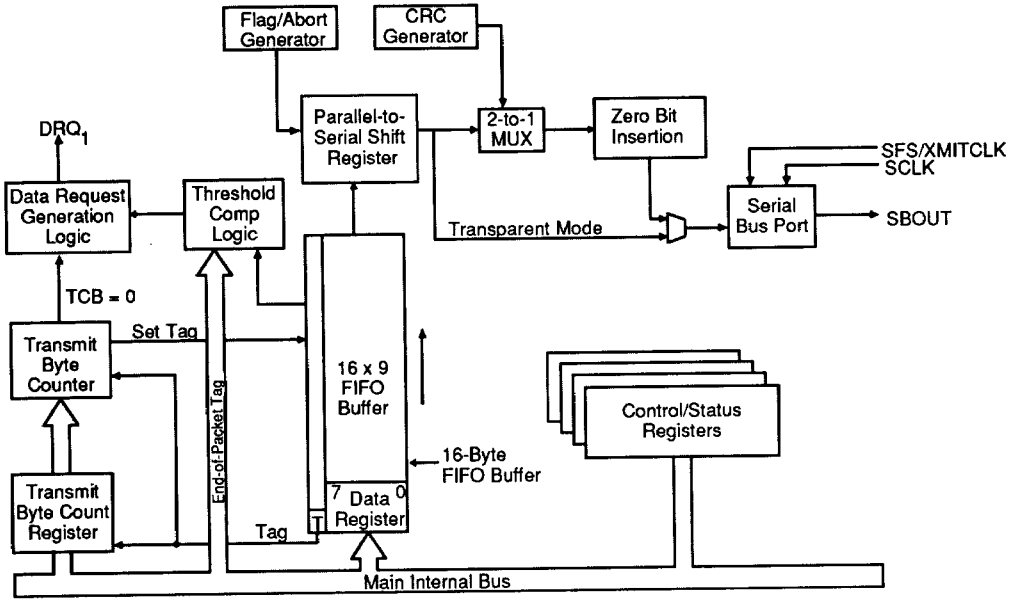


Figure 2. DLC Transmitter

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bits in the packet (in the last byte of the I-field just prior to transmitting the FCS). When the last byte of the I-field is to be transmitted, the contents of the Residue Bit Status Control Register are used to determine when the FCS is actually sent.

CRC Generator—The Frame Check Sequence (FCS) is 16 bits long and contains the generated CRC code for the frame being transmitted. All data transmitted between the opening and closing flags (excluding inserted zeros) is included in the CRC calculation. The standard CCITT generator polynomial, $X^{16}+X^{12}+X^5+1$, is used.

Zero Bit Insertion—The zero bit insertion logic provides data transparency by ensuring that flag or abort characters embedded in the data is not recognized by the remote receiver as actual data link control characters. The zero bit insertion logic monitors the data stream between the opening and closing flags of a frame and inserts a "0" after detecting five contiguous "1"s.

Flag/Mark Idle Generation —The DLC transmitter may be programmed to either flag or mark idle when the transmitter is enabled and is not actively sending a data packet or an abort sequence.

Abort Generation —An abort sequence will be sent by the DLC transmitter whenever the Send Abort bit (bit 0 in the DLC Command/Control Register) is set. The transmitter will continue sending an abort sequence as long as this bit is set; however, if the Send Abort bit is set and cleared on two successive writes to the DLC Command/Control Register at least one abort character will be sent.

Serial Bus Port—The Serial Bus Port (SBP) sits at the output of the transmitter and performs a number of functions related to time slot assignment, clock selection, data inversion, transmitter enable/disable, and loopback testing.

Time Slot Multiplexer: The time slot multiplexer operates in two modes: multiplexed and non-multiplexed. In the multiplexed mode, one of 31 time slots may be programmed to transmit data; in the non-multiplexed mode, the data is transmitted directly without multiplexing. In addition, time slots 0 and 1 can be concatenated in multiplexed mode into one 16-bit wide slot by holding the frame sync signal, SFS/XMIT , active through the first bit time of time slot 1.

Transmit Enable/Disable Logic: The transmit enable/disable logic monitors bit 1 of the DLC Command/Control Register. When this bit is reset to "0," the SBOUT pin is set to a physical mark idle state (i.e., the SBOUT pin is pulled High). Note that if the transmitter is disabled or en-

abled during the programmed time slot (in multiplex mode), the disabling or enabling of the transmitter will occur at the end of the time slot.

Local Loopback Logic: The DLC can be placed in a local Loopback mode for test purposes by setting bit 6 in the SBP Control Register to "1." Local loopback disconnects the SBIN pin and connects the transmitter output to the receiver input. The selected transmit clock is used as the receive clock.

Remote Loopback Logic: The DLC can be placed in the remote loopback mode for diagnostic purposes by setting bit 7 of the SBP Control Register to "1." In remote loopback mode, the transmitter is disabled and data received at the SBIN pin is echoed out the SBOUT pin. The receiver operates normally in this mode.

Transparent Mode: In Transparent Mode, all HDLC protocol functions are bypassed. Data is transmitted exactly as it is loaded in the transmit FIFO. Transparent Mode is enabled when bit 7 of the DLC Residual Bit Status Control Register is set to "1." Two modes of operation are available in Transparent Mode using bit 6 of the DLC Residual Bit Status Control Register.

Transparent Mode 1—If bit 6 and bit 7 of the DLC Residual Bit Status Control Register are set to "1," the number of bytes to be sent, after the XMIT Enable bit in the DLC Command/Control Register is set to "1," is determined by the count programmed in the DLC Transmit Byte Count Register. When the number of bytes loaded into the transmit FIFO equals the programmed count further DMA requests are inhibited and, when the last bit of the last byte is transmitted, the XMIT Enable bit will be cleared to "0" and the Valid Packet Sent Status bit in the DLC Interrupt Source Register will be set to "1" to indicate that transmission has completed.

Transparent Mode 2—If bit 6 is set to "0" and bit 7 is set to "1" in the DLC Residual Bit Status Control Register, the number of bytes transmitted will be controlled by the XMIT Enable bit in the DLC Command/Control Register and the DLC Transmit Byte Count Register will be ignored. In this mode of operation the DLC will start generating DMA requests and sends data for as long as the XMIT Enable bit is set to "1." When this bit is cleared to "0" further DMA requests are inhibited and, when the last bit of the last byte is transmitted, the Valid Packet Sent Status bit in the DLC Interrupt Source Register will be set to "1" to indicate that transmission has completed.

56 kb/s Mode: If bit 7 of the DLC Residual Bit Status Control Register is set to "1" and the DLC is programmed for multiplex operation, the DLC will transmit data at a 56 kb/s data rate instead of the normal 64 kb/s data rate. In this mode, the DLC will send data within an 8-bit time slot period, but will always disable the SBOUT pin High during the eighth bit time period.

DLC Receiver

The receiver (shown in Figure 3) processes serial data packets from the SBP and transfers the data to a 32-byte receive FIFO, where it is transferred to "off-chip" RAM memory under DMA or processor control. Data rates from 0 to 2.048 Mb/s are allowed. The hardware can receive an entire packet and move the information to off-chip RAM without processor intervention if DMA is used in the design. Packet status information is then reported on a packet-by-packet basis at the time that the last byte of the packet has been moved to memory.

Dedicated hardware modules perform bit-level operations on each frame of data including mark-Idle and flag-Idle detection, data inversion, flag/abort recognition, zero bit deletion, CRC checking, and address recognition.

Functionally, the receiver consists of the following major circuits:

Serial Bus Port
Zero bit Deletion Unit
Short Frame Byte Counter
CRC Checker
Serial-to-Parallel Shift Register
Address Detection Unit
Receive FIFO
Receive Byte Counter

Serial Bus Port—The Serial Bus Port (SBP) receives serial data from the SBIN pin and sends it to the flag/abort detection unit and the zero bit deletion unit.

The SBP performs three operations on the incoming data:

1) Mark Idle Detection
2) Programmable data inversion
3) Time slot de-multiplexing

Zero Bit Deletion Unit—The zero bit deletion unit monitors the data stream between the opening and closing flags and removes a zero that appears after a string of five consecutive "1"s ("0"s are added during transmission to prevent a data pattern from resembling an abort, opening, or closing Flag).

Short Frame Byte Counter—The Short Frame Byte Counter is a 4-bit counter that counts the number of characters that have reached the serial-to-parallel shift register. If a frame ends in a flag, and the number of bytes received is less than the value programmed into the Minimum Packet Size Register, and data has been placed in the FIFO (Receive Byte Counter > 0), the SHORT FRAME ERROR status bit in the Receive Frame Status Register will be set to "1" when the last byte of the packet is read from the receive FIFO. Note that packet status is reported to the user and interrupts are generated, when the last byte of the received packet is read by

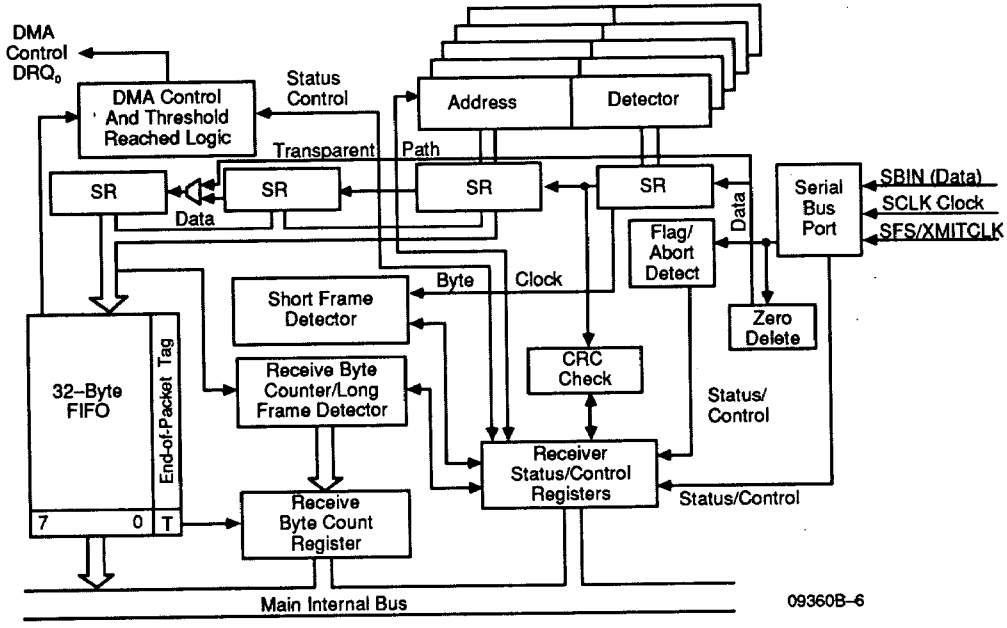

Figure 3. DLC Receiver

the processor or placed in off-chip RAM by the DMA controller.

CRC Checker—The output of the flag/abort detection unit is shifted into the CRC Checker. When the closing flag is detected, the 16-bit Frame Check Sequence has just been shifted into the checker. At this point, the contents of the CRC Checker is examined. If an error is detected, the CRC ERROR status bit is set in the Receive Frame Status Register (bit 2) when the last byte of the packet is read from the receive FIFO. The FCS can optionally be placed in the receive FIFO by setting the ENABLE FCS PASS-THRU bit (bit 7) to "1" in the DLC Command/Control Register. If this bit is set to "0" the FCS is discarded by the DLC and is not available for use.

Serial-to-Parallel Shift Register—The output of the zero bit deletion unit is fed into a 32-bit shift register which converts the serial stream into bytes.The parallel output of the shift register is fed to the receive FIFO, one byte at a time.

Address Detection Unit—The address detection unit identifies packets that are addressed to the receiver. Depending on programming, the first, second, or both of the first two bytes of each received packet (after receipt of an opening flag) are compared with the contents of five address registers (four user-programmable registers and one broadcast). If address recognition is enabled and the incoming packet's address field matches one of the address registers, the packet is received; otherwise, the packet is discarded and the receiver goes into a wait pattern looking for the next flag. As a programmable option, the Command/Response (C/R) bit (bit 1 of the first byte) can be ignored. If address recognition is disabled (i.e., bits 4–0 of the DLC Address Control Register are reset to "0"), all packets are accepted by the DLC.

Receive FIFO—The receive FIFO is a 32-byte buffer located between the serial-to-parallel shift register and the Microprocessor Interface (MPI). The FIFO is loaded by the shift register and unloaded by either the local processor or DMA controller. When the user-visible Data Register contains data, the RECV DATA AVAIL status bit in the DLC FIFO Status Register is set to "1" and a maskable interrupt is generated. This status bit is cleared to "0" when the byte is read from the Data Register and the receive FIFO becomes empty.

Receive FIFO Threshold Logic: This logic generates a receive FIFO Threshold Reached signal. This signal is High whenever the number of bytes in the receive FIFO are equal to or greater than the threshold level programmed into the FIFO Threshold Register (bits 7–4). This signal is used to set the RECV TRSHLD REACHD status bit to "1" in the DLC FIFO Status Register and generate a maskable interrupt. The Threshold Reached signal is also used to generate DRQ_0.

Data Movement Control: Data is moved from the receive FIFO either by DMA or Programmed I/O. The DRQ_0 pin is the receive FIFO's Data Request output to

the off-chip DMA controller. DRQ_0 is activated when the level in the FIFO reaches the programmed threshold, or the last byte of a packet is placed in the FIFO. Once activated, DRQ_0 remains active until the FIFO becomes empty or the last byte of a packet is removed from the FIFO. DRQ_0 will not be re-activated until the status of the previous packet has been read (by reading the least significant byte of the Receive Byte Count Register).

When programmed I/O is used, a maskable interrupt is generated when the programmed threshold is reached. The user removes data by reading the receive FIFO Data Register. If the last byte of a packet is placed in the FIFO, the end-of-packet Interrupt (maskable) indicates that the FIFO requires servicing. In this case, the user reads a data byte and then polls the RECV DATA AVAIL bit in the DLC FIFO Status Register. The user continues to remove data in this read-a-byte, poll RECV DATA AVAIL bit, read-a-byte fashion until the RECV DATA AVAIL bit is no longer set to "1." Since this procedure is in response to an end-of-packet Interrupt, the lack of a valid RECV DATA AVAIL bit indicates that the previously read data byte was the last in the packet and packet status should be read. The RECV DATA AVAIL bit de-activated by the receive is FIFO in response to the packet's last byte being removed. This happens even if the FIFO is not empty (for example, data from a new packet has been received). The RECV DATA AVAIL status bit will not be re-activated until the least significant byte of the Receive Byte Count Register is read (and additional data is in the FIFO).

Receive Byte Counter—The Receive Byte Counter keeps track of the number of current packet bytes transferred into the receive FIFO. When the last byte is removed from the FIFO, the contents of the counter are loaded into the Receive Byte Count Register.

The receive byte count is used to identify long frames and frames that have terminated prior to any data being placed in the buffer. Software uses the receive byte count to determine the length of a received frame.

Long Frame Error—A long frame error occurs when the closing flag of a frame is not detected before the number of received bytes equals the value programmed in the Maximum Packet Size Register. When this occurs, the byte that caused the long frame error is tagged as the last byte and the LONG FRAME ERROR status bit is set to "1" in the DLC Receive Frame Status Register.

Bit Residue—As data is shifted into the serial-to-parallel shift register, the bits in each byte are counted. When the counter reaches eight, a byte of data is transferred into the receive FIFO. If a closing flag is detected and this count does not equal eight the NON-INT # BYTES RECV status bit in the DLC Receive Frame Status Register will be set to "1" to indicate that a non-integer number of bytes has been received. When this occurs the 3-bit field (bits 2–0) in the DLC Residual Bit Status Control Register reports the number of data bits received at the time the closing flag was detected. This register is a delayed-reporting type register like the Receive Byte Count Register. The residue bits are right-justified before being placed in the receive FIFO.

Transparent Mode—In Transparent Mode, all receive HDLC functions (i.e., flag/abort detection, CRC checking, and zero bit deletion) are bypassed. Two modes of operation are provided through the use of bit 6 and bit 7 of the DLC Residual Bit Status Control Register. When the RECVER ENABLE bit in the DLC Command/Control Register is set to "1" data is loaded into the receive FIFO exactly as it is received. The FIFO operates normally. In addition, if bit 6 of the DLC Residual Bit Status Control Register is set to "1," the DLC Maximum Packet Receive Register is used to determine when the IDPC disables data reception.

Transparent Mode 1—If bit 6 and bit 7 of the DLC Residual Bit Status Control Register are set to "1," the number of bytes to be received, after the RECVER ENABLE bit in the DLC Command/Control Register is set to "1," is determined by the count programmed in the DLC Maximum Packet Receive Register. When the number of bytes loaded into the receive FIFO equals the programmed count further DMA requests are inhibited and, when the last byte is read from the FIFO, the VALID PACKET RECVD status bit in the DLC Interrupt Source Register is set to "1" to indicate that data reception is complete.

Transparent Mode 2—If bit 6 is reset to "0" and bit 7 is set to "1" in the DLC Residual Bit Status Control Register, the number of bytes received is controlled by the RECVER ENABLE bit in the DLC Command/Control Register. and the DLC Maximum Packet Receive Register is ignored. In this mode of operation, the DLC accumulates 8-bit characters and operates as in normal mode of operation as long as the RECVER ENABLE bit is set to "1." When this bit is reset to "0" further DMA requests are inhibited and, when the last byte is read from the FIFO, the VALID PACKET RECVD status bit in the DLC Interrupt Source Register will be set to "1" to indicate that data reception is complete.

56 kb/s Mode: If bit 7 of the DLC Residual Bit Status Control Register is set to "1" and the DLC is programmed for multiplexed operation, the DLC receives data at a 56 kb/s data rate instead of the normal 64 kb/s data rate. In this mode, the DLC receives 7 bits of data within an 8-bit time slot period, but always accumulates eight bits in the receive shift register before transferring it to the receive FIFO.

Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The IDPC's USART provides a superset of the 8250 UART features and supports both synchronous and asynchronous serial communications. The USART is capable of full-duplex operation at speeds up to 64 kb/s us-

ing either the on-chip programmable Baud Rate Generator or external clock sources.

The USART consists of the following major circuits:

- USART Receiver
- USART Transmitter
- Modem Control Unit
- Interrupt Controller
- Baud Rate Generator
- Clock Selector Unit

A simplified block diagram of the USART is shown in Figure 4.

USART Receiver

The receiver performs serial-to-parallel conversion, verifies framing, buffers the data in a FIFO, and detects break conditions, parity errors, and special characters. A maskable interrupt is generated if a parity error, framing error, or a break condition is detected. Data can be read out of the receive FIFO into external RAM memory under control of the external processor or DMA.

Parity Checking—If the ENABLE PARITY bit (bit 3) in the USART Line Control Register is set to "1," the parity generation/checking logic is enabled and parity is checked on all characters loaded into the receive FIFO. When the parity check bit generated by the receiver does not match the parity bit appended by the transmitter, the PARITY ERROR IN FIFO status bit in the USART Line Status Register is set to "1" and, if the RECV LINE STATUS bit in the USART Interrupt Enable Register is set to "1," an interrupt will be generated when that character is transfered to the receive FIFO. The CHAR w/ PARITY ERROR AVAIL status bit in the USART Status Register is then set to "1" when the character with the parity error reaches the output of the receive FIFO. No interrupt is generated by this bit. The selection of odd or even parity is made via bit 4 of the USART Line Control Register. Parity checking is available only in asynchronous mode.

Stick Parity—Stick parity is a test mode that forces the parity bit to be generated and detected as the logical inversion of the USART Line Control Register bit 4 when USART Line Control Register bits 5 and 3 are set. For example, if bits 5, 4, and 3 are set then the parity bit is always generated and detected as a "0." If bits 5 and 3 are set and bit 4 is cleared then the parity bit is always generated and detected as a "1."

Break Detection—Break Detection is performed in the asynchronous mode only. If the receive data input is held spacing ("0"s) for more than a full character time (start bit, data bits, parity bit, and stop bits), the USART sets the BREAK DETECT status bit (bit 4) in the USART Line Status Register to "1" and, if bit 2 in the USART Interrupt Enable Register, RECV LINE STATUS is set to "1" an interrupt is generated.

Framing Error Detection—Frame errors are detected in only the asynchronous mode. In this mode, if a received character does not have a valid stop bit and a Break condition is not present, the USART reports a framing error by setting bit 3 of the USART Line Status Register. If bit 2 in the USART Interrupt Enable Register, RECV LINE STATUS, is set to "1" an interrupt is generated.

Receive Shift Register—The receive shift register provides serial-to-parallel conversion for the serial data entering the Receive Data (RxD) pin.

Receive FIFO—The receive FIFO is a 4-byte, 10-bit-wide buffer used for temporary storage of receive data from the receive shift register. The FIFO provides storage for 8 data bits, one special character flag, and one parity error flag. Parity and special character conditions are checked when data is loaded into the FIFO.

The presence of a character with either a special character or parity error flag is reported in the USART Line Status Register. Maskable interrupts are generated when an error condition is detected. Data is read out of the FIFO from the receive FIFO Data Register. Only the 8 data bits are accessible by the external processor or DMA controller.

While special character and parity error interrupts are generated when the character is loaded into the FIFO, the parity error present and special character available status bits (in the USART Line Status Register) are not set until the character is at the FIFO output. This allows the user to identify which character caused the interrupt.

The receive FIFO Data Register is the equivalent of the Receive Buffer Register in the 8250 UART. The presence of valid data in the receive FIFO Data Register is indicated by bit 0 (RECV DATA AVAIL bit) in the USART Line Status Register.

Receive Overrun Error Detection—If the receive FIFO is full when a newly received character is to be loaded into the FIFO, receive overrun error is reported via bit 1 (RECV BUFFER OVERUN) in the USART Line Status Register, and, if the RECV LINE STATUS bit in the USART Interrupt Enable Register is set to "1," an interrupt is generated.

Receive Character Length—If the USART Line Control Register is programmed to receive characters with fewer than 8 bits, the unused bit positions are filled with "0"s as the character is placed in the receive FIFO.

Receive FIFO Timeout—If the FIFO level is below the programmed threshold and no new characters are received within approximately 2048 receiver clocks, and, if the RECV FIFO TIMEOUT bit in the USART Interrupt Enable Register is set to "1," an interrupt is generated to in-

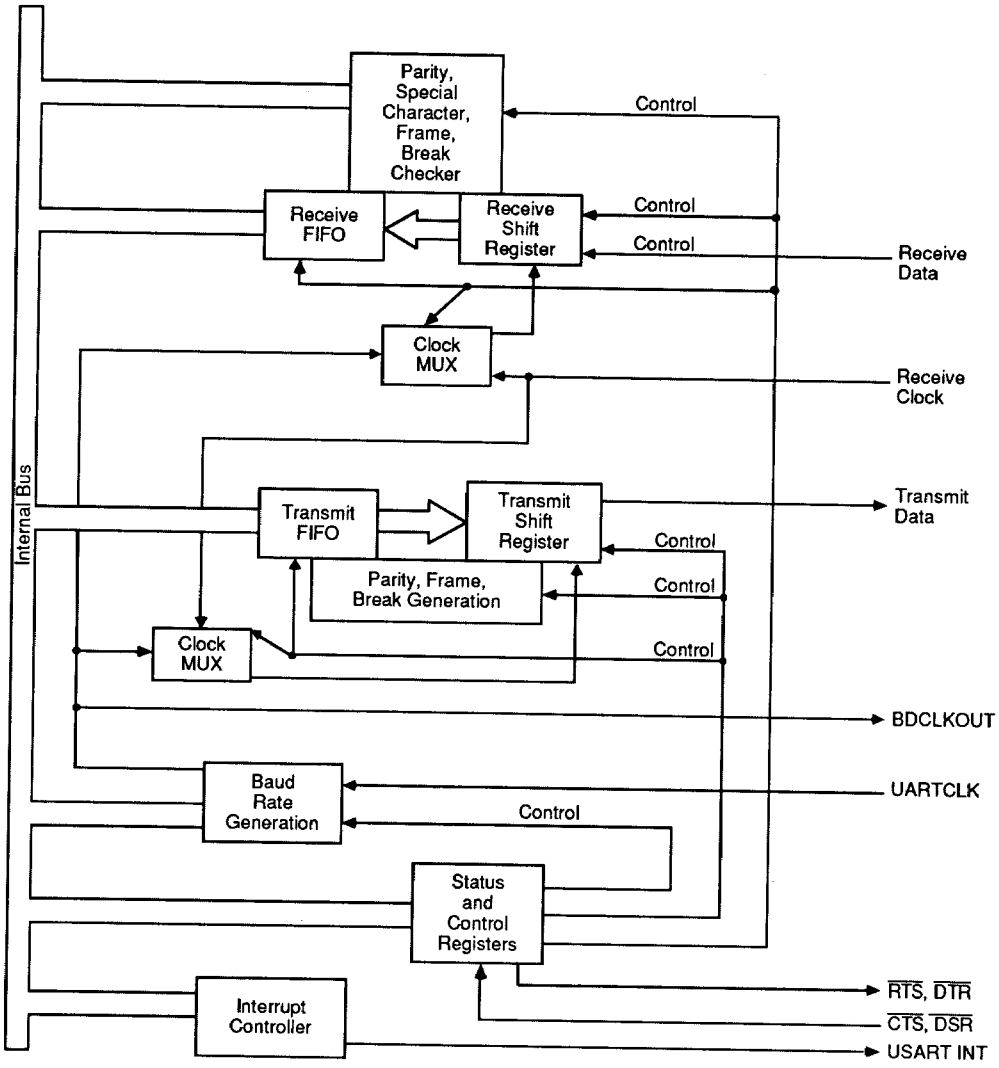

Figure 4. USART Simplified Block Diagram

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dicate that data is available in the FIFO. This function is available only in the asynchronous mode.

Special Character Recognition Logic—Special character recognition is performed by using the lower order 7 bits of each received character as a pointer into a 128-bit RAM. If the addressed RAM bit has been programmed by the user to "1," the SPCHL CHAR IN FIFO status bit (bit 7) in the USART Line Status Register is set to "1," and, if the SPCHL CHAR bit (bit 5) in the USART Interrupt Enable Register is set to "1," an interrupt is generated. The SPCHL CHAR AVAIL status bit (bit 2) in the USART Status Register is set when the special character reaches the output of the receive FIFO.

Synchronous Mode—The synchronous mode of operation is enabled when the SYNC/ASYNC SELECT bit (bit 2) in the USART Control Register is set to "1." In this mode of operation, the receiver clocks in data bits on each rising edge of the selected clock. Each 8 bits received are placed in the receive FIFO without regard for framing or breaks. This mode allows for transparent reception of a data stream, regardless of protocol.

USART Transmitter

The USART Transmitter consists of the following major circuits:

Transmit FIFO
Parallel-to-Serial Shift Register
Frame, Break, and Parity Generation Logic

Transmit FIFO—The transmit FIFO serves as a buffer for data being moved from memory to the parallel-to-serial shift register. As the shift register becomes empty, the next character is moved from the FIFO to the parallel-to-serial shift register.

When the number of bytes in the transmit FIFO becomes less than or equal to the programmed transmit threshold level in the USART Control Register (bits 6 and 5), the XMIT TRSHLD REACHD status bit (bit 5) in the USART Line Status Register is set to "1," and , if the XMIT FIFO TRSHLD bit (bit 1) in the USART Interrupt Enable Register is set to "1," an interrupt is generated.

Bit 5 in the USART Line Status Register is the equivalent of the Transmitter Holding Register Empty in the 8250 UART.

Parallel-to-Serial Shift Register—The parallel-to-serial shift register converts parallel data from the FIFO into serial form for transmission.

The shift register clock can come from either the Baud Rate Generator (BDCLKOUT) or from the RxCLK pin. The clock source for the shift register should be 16 times the data rate in asynchronous mode and the same as the data rate in synchronous mode. Bit 6 (XMIT SHIFT REG EMPTY) of the USART Line Status Register is set to "1" when the transmit FIFO is empty and the last bit of the transmit shift register has been shifted out. An interrupt is generated by this condition if the SHFTREG EMPTY bit (bit 6) in the USART Interrupt Enable Register is set to "1."

Frame, Break, and Parity Generation Logic—Frame generation takes place only in the asynchronous mode of operation. The number of stop bits and character length are programmed via the USART Line Control Register. The same parameters apply to the receiver. Even, odd, and no parity can be selected via the USART Line Control Register.

Break Generation—The USART will generate a break condition (all "0"s) when bit 6 (BREAK) in the USART Line Control Register is set to "1." When this bit is set the USART transmits a minimum 10 consecutive "0"s immediately after completing any character transmission in progress, and continues sending this pattern until the bit is cleared. When the bit is set and the current character being transmitted clears the shift register the transmit FIFO is cleared. When the bit is reset, the TxD pin will be returned High for at least one bit time before a new character is transmitted. This allows the start bit of the new character to be generated.

Modem Control Unit

The USART contains modem handshake signals for use in controlling communications between the IDPC and a RS232 type terminal. The modem handshake signals include: $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, and $\overline{DTR}$.

$\overline{RTS}$ and $\overline{DTR}$ are outputs and are controlled by the local processor via bits 1 and 0 in the USART Modem Control Register, respectively. $\overline{CTS}$ and $\overline{DSR}$ are inputs and their status can be read via the USART Modem Status Register, bits 4 and 5 respectively. The Change in $\overline{DSR}$ and Change in $\overline{CTS}$ bits in the Modem Status Register indicate pin status since the USART Modem Status Register was last read. A maskable Modem Status Interrupt is generated if bit 3 of the USART Interrupt Enable Register and either bit 1 or bit 0 of the USART Modem Status Register are set. The Change in $\overline{DSR}$ and Change in $\overline{CTS}$ bits are cleared when the USART Modem Status Register is read.

Interrupt Controller

The USART interrupt controller issues an interrupt request to the external processor if an interrupt occurs and that particular interrupt is enabled in the USART Interrupt Enable Register. The interrupt request remains active until the source of the interrupt is cleared. Bits 1, 2, and 3 of the USART Interrupt Identification Register define the source of the interrupt. Bit 0, when cleared, indicates that an interrupt is pending.

Baud Rate Generator

The USART Baud Rate Generator is a programmable 16-bit divider that receives its input from the USARTCLK pin and can provide the clock to the USART transmitter and receiver. The Baud Rate Generator is configured by loading the USART Baud Rate Divisor LSB and MSB Registers. These registers are accessed by setting the DIV LATCH ACCESS BIT (bit 7 in the USART Line Control Register) and then writing to USART hexadecimal addresses 20 and 21 (USART Data Registers and Interrupt Enable Register addresses when the DIV LATCH ACCESS BIT is cleared).

In asynchronous mode, the Baud Rate Generator must be programmed to a value 16 times the data rate. The output of the Baud Rate Generator is fed to the USART transmitter and receiver and BDCLKOUT pin. Programming the Baud Rate Generator to divide-by-1 passes the USARTCLK unaffected. An internal divide-by-16 circuit generates the appropriate clock rate for the transmitter.

Clock Selector Unit

The sources of the transmitter and receiver clocks are independently selectable. For example, when bit 0 is set to "1" in the USART Control Register, the Receiver uses the output of the Baud Rate Generator for its clock. When bit 0 is cleared, the RxCLK input is used. The same options apply to the transmitter, except in this case, bit 1 in the USART Control Register specifies the clock source.

Dual-Port Memory Controller (DPMC)

The DPMC permits the use of shared memory in a multiprocessing environment. The local processor exchanges data with the host processor via shared memory and interprocessor hardware interrupts. The local processor also accesses any device on the IDPC external bus. The host processor can only access the RAM on the IDPC external bus. Any contention between the local processor and the host processor is arbitrated by the DMPC logic internal to the IDPC, providing for transparent access to shared memory. Both processors communicate via memory-resident data buffers and "mailboxes." An inter-processor interrupt scheme notifies the other processor when one of the processors has written data to a buffer or a command to a mailbox.

Functionally, the Dual-Port Memory Controller consists of the following major circuits:

Memory Cycle Arbitration and Control
Buffer/Latch Control
Inter-processor Interrupt Controller

A simplified block diagram of the Dual-Port Memory Controller is shown in Figure 5.

Memory Cycle Arbitration and Control

The DPMC generates the cycle timing for all accesses to shared RAM. The length of each cycle is fixed and independent of the cycle times of either the local or host processors. This logic generates memory cycles in response to processor requests. In case of conflicting requests, the logic arbitrates the conflict, granting the first memory access cycle to one processor while holding off the other processor via the appropriate ready line. The DPMC always arbitrates in favor of the local processor (L-port). If a request from the host port (H-port) is present during a local memory cycle, the host processor is granted the next memory cycle.

Buffer/Latch Control

The Buffer/Latch Control logic performs such functions as enabling RAM output drivers, enabling data bus latches, and generating RAM cycle timing.

Inter-Processor Interrupt Controller

The inter-processor interrupt controller provides for inter-processor interrupts via the Semaphore Register. The Semaphore Register is located in the IDPC and is used to coordinate inter-processor interrupts. The local processor can access the Semaphore Register directly, but the host processor cannot (access is provided via strobes to specific pins on the IDPC).

For a local-to-host-processor interrupt, the local processor writes a "1" in bit 0 of the Semaphore Register. When this bit is set, the Interrupt Controller activates the Host Interrupt Out (HINTOUT) pin. The host then responds by pulsing the Host Interrupt Acknowledge (HINTACK) line, clearing the bit and thus the interrupt.

A host-to-local-processor interrupt is initiated when the host pulses the Host Interrupt In (HINTIN) pin. When this happens, Bit 1 in the Semaphore Register is set, activating the Local Interrupt Out (LINTOUT) line. The local processor then acknowledges the interrupt by clearing bit 1 in the Semaphore Register.

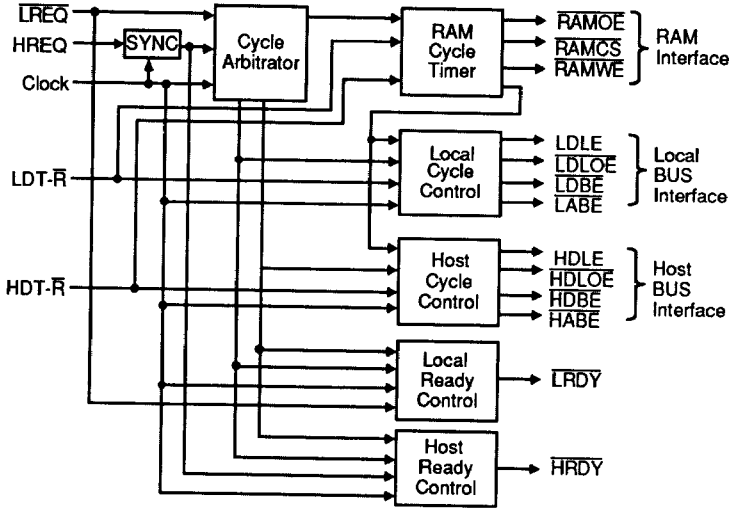

Figure 5. Dual-Port Memory Controller (DPMC)

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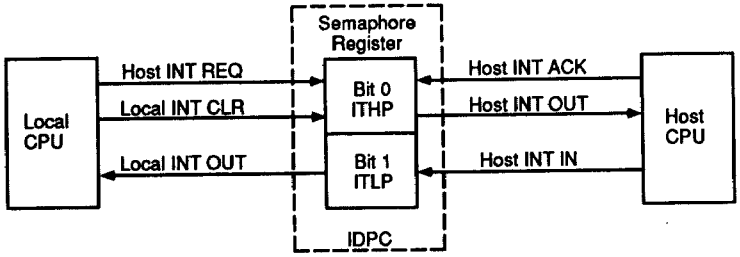

Notes: Local Interrupt Clear and Host Processor Requests are writes to the Semaphore Register by the local processor.
ITLP = Interrupt to Local Processor
ITHP = Interrupt to Host Processor

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Figure 6. Inter-Processor Interrupt Structure

Programmable Features

The IDPC is controlled via internal registers that are written and read by software running on the local processor connected to the IDPC external bus. These internal registers may be mapped into either memory or I/O space.

The internal registers occupy a 64-byte block located in the local processor's memory address space. The starting address of the memory block is determined by address decode logic (external to the IDPC) that is used to generate the IDPC chip select signal ($\overline{CS}$). The registers and their respective memory offset values are provided in Tables 1–4.

In systems containing more than one processor (e.g., a workstation application with host processor and local processor), only the local processor can access the IDPC registers. The host processor, however, can control IDPC operations indirectly by issuing requests to the local processor via shared memory supported by the IDPC's Dual Port Memory Controller.

The programmable registers are used for establishing modes of operation, configuring the IDPC, and monitoring/reporting status.

Table 1. IDPC Address Map

Offset (Hex)	Block
00–1F	DLC
20–2A	USART
2B–3E	Reserved
3F	DPMC

Data Link Controller (DLC)

DLC Transmitter

The programmable features associated with the DLC transmitter include:

Transmit Enable—the transmitter may be disconnected from the output pin (SBOUT), leaving other transmit functions intact.

Abort Generation—interrupts a frame and places the transmitter in the abort condition.

Flag/Mark Idle—either condition may be selected as an idle state between frames.

CRC Generation—may be enabled or disabled.

FIFO Threshold—user selectable threshold of 0 to 15 bytes. When the level of the transmit FIFO falls to this level or below, status is reported and a DMA request is generated.

Transparent Mode—transmit HDLC control functions (i.e., flag generation, CRC generation, abort generation, and zero bit insertion) are disabled and data is sent as received from the transmit FIFO.

Interrupts–the following transmitter-related interrupts can be selectively enabled or disabled:

- Valid Packet Sent
- FIFO Buffer Available
- Transmit Threshold Reached
- Transmit Underrun

DLC Receiver

The DLC receiver programmable features include:

Receiver Enable—when disabled, the receive data input pin (SBIN) is disconnected leaving other receiver functions intact.

CRC Check—selectively enables or disables the internal CRC compare operation.

CRC Pass-Thru—the FCS field can be placed into the receive FIFO with the data.

Address Recognition—program any combination of four unique one- or two-byte addresses and the broadcast address, performing address filtering on all incoming packets. In the 1-byte mode, either the first or second byte can be selected. In addition, the Command/Response bit (bit 1 of the first byte) can be ignored.

Minimum Packet Size—defines the minimum packet size in use. A short frame error is indicated if a packet is received containing fewer than the programmed number of bytes (0–15 bytes).

Maximum Packet Size—defines the maximum packet size in use. This prevents buffer overruns in the event of lost flags or protocol violations (65,536 bytes).

FIFO Threshold—select threshold of 2 to 32 bytes. When the level of the receive FIFO reaches this level or above, status is set (unless the last byte of a packet has already been read from the FIFO and status for that packet has not yet been read by the user) and a DMA request is generated. This forms an interlock that maintains synchronization between packet status and data.

Transparent Mode—receive HDLC related control functions (i.e., abort detection, CRC generation and checking, flag detection, and zero bit deletion) are disabled and data is received unaltered.

56 kb/s Mode—data is received at a 56 kb/s data rate instead of the usual 64 kb/s rate while in multiplex mode.

Interrupts—the following DLC receiver interrupts may be selectively enabled or disabled:

- Valid Packet Received
- Abort Received
- Non-Integer Number of Bytes Received (bit residual)
- Receive Data Available
- End-of-Packet in Receive FIFO

DLC Transmit/Receive Options

The following programmable options affect both the DLC transmitter and receiver:

Data Inversion—the output of the transmitter and the input of the receiver are inverted when this option is selected.

Channel Selection—up to 31 8-bit time slots for multiplexing transmitted serial data and demultiplexing received serial data may be chosen. In non-multiplexed mode, received serial data is continuous and the SFS/XMITCLK pin is used as a transmit clock input independent of the receive clock input.

Local Loopback—the DLC can be programmed to route transmitted data to the receiver for diagnostic purposes.

Remote Loopback—the DLC can be programmed to route received data to the transmit data output for remote testing capabilities.

Reset—a software reset can be generated to stop all functions, clear the FIFOs, and set all registers to their default values.

Delayed Status Reporting

The DLC contains several registers that report status in a delayed fashion (see Figure 7). The Receive Frame Status Register, Receive Byte Count Register, Receive Link Address bit field (bits 2–0 of the Interrupt Source Register), and the Receive Field of the Residue Status Control Register (bits 2–0 require this specific implementation in order to support the reception of contiguous (back-to-back) frames. These registers, and residue bit fields, maintain a "history" of frame status, and byte counts of up to three previously received frames while a fourth frame is actually being received. This allows status storage for up to 4 frames.

Each of these registers and bit fields are comprised of the following four stages: current, holding, master, and slave.

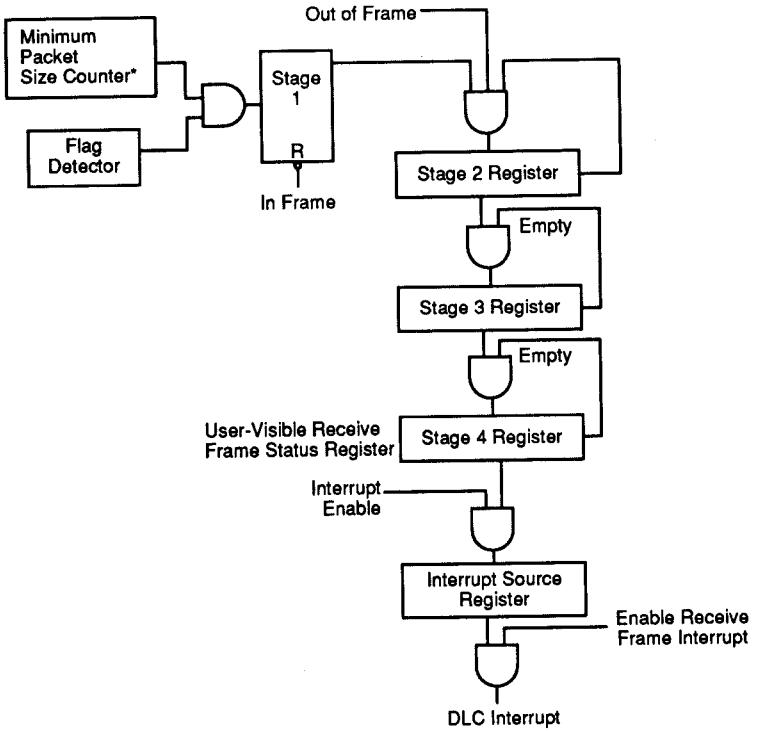
As shown in Figure 7, stage 1 holds the current status of the frame presently being received on the link. This stage is updated with the current DLC receiver status as changes occur in real-time.

Stage 1 is transferred to stage 2 when stage 2 is empty and the last byte of another packet is transferred to the DLC receive FIFO. If stage 2 is not empty, then stage 1 retains its status. When stage 1 has transferred to stage 2, stage 1 is free to acquire status of the next packet.

Stage 2 status is transferred to stage 3 as soon as stage 3 becomes empty, allowing status to move from stage 1 to stage 2.

Stage 3 status is transferred to stage 4 (which is the actual status register read by user software) when stage 4 is empty and the last byte of a packet is received. If stage 4 is not empty, then stage 3 retains its status. Stage 4 is cleared when read by software or when DLC reset occurs.

The frame status can back up. If stage 4 has not been read when an event occurs that would cause stage 3 to be transferred to stage 4, stage 3 is not transferred to stage 4. What happens is as follows: existing stages 1, 2,



*Minimum packet size is used as one possible example.

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Figure 7. Four-Stage Delayed Status Mechanism

3, and 4 are not disturbed, the DLC receiver freezes stage 1 and data at the SBIN pin is ignored.

Additional received packets are lost until stage 4 is read. As soon as stage 4 is read, stage 3 is transferred to stage 4, stage 2 moves to stage 3, and stage 1 is transferred to stage 2. At this point, the DLC receiver logic enters a "hunt-for-flag" state, and frame reception can begin again.

The valid and invalid packet received bits of the DLC Interrupt Source Register are also reported in a delayed fashion.

Note: If the various delayed-stacked status registers have not been read since the Interrupt Source Register was last read, and the LSB of the Receive Byte Count Register is read, these status registers will be cleared. This ensures that the four-layer stack will remain in sync if a packet is received and the status registers are not read.

Detailed Description of User-Visible DLC Registers

The DLC contains 23 registers, as shown in Table 2.

Table 2. DLC Registers

Offset (Hex)	Register Name	Size (Bytes)	Type
00	Command/Control Register	1	Read/Write
01	Address Control Register	1	Read/Write
02	Link Address Recognition Register 0	2	Read/Write
04	Link Address Recognition Register 1	2	Read/Write
06	Link Address Recognition Register 2	2	Read/Write
08	Link Address Recognition Register 3	2	Read/Write
0A	Serial Bus Port Control Register	1	Read/Write
0B	Minimum Receive Packet Size Register	1	Read/Write
0C	Maximum Receive Packet Size Register	2	Read/Write
0E	Interrupt Source Interrupt Enable Register	1	Read/Write
0F	Receive Frame Interrupt Enable Register	1	Read/Write
10	Receive Link Interrupt Enable Register	1	Read/Write
11	FIFO Status Interrupt Enable Register	1	Read/Write
12	Transmit Byte Count Register	2	Read/Write
14	FIFO Threshold Register	1	Read/Write
15	Interrupt Source Register	1	Read Only
16	Receive Byte Count Register	2	Read Only
18	Receive Frame Status Register	1	Read Only
19	Receive Link Status Register	1	Read Only
1A	FIFO Status Register	1	Read Only
1B	Receive FIFO Data Register	1	Read Only
1C	Transmit FIFO Data Register	1	Write Only
1D	Residual Bit Control Status Register	1	Read/Write
1E–1F	Reserved	2	–

DLC Command/Control Register (00 HEX)

This register is used to control basic transmitter and receiver functions.

7	6	5	4	3	2	1	0
ENABLE FCS PASS-THRU	DLC RESET	ENABLE CRC GENER.	ENABLE CRC CHECK	FLAG/ MARK IDLE SELECT	RECVER ENABLE	XMIT ENABLE	SEND ABORT

Bit 7: FCS Pass-Thru Enable (Default = 0)—The Frame Check Sequence (CRC) bytes will be transferred to the receive FIFO if this bit is set to "1"; otherwise, they will be discarded by the DLC.

Bit 6: DLC Reset (Default = 0)—When this bit is set to "1," all DLC FIFOs, latches and status/control bits are forced to their default values. A delay of ten Master Clock (CLK) cycles is required before any DLC registers can be accessed, after resetting the DLC.

Bit 5: CRC Generate Enable (Default = 1)—If this bit is set to "1," the frame is terminated by appending the calculated CRC bytes and closing flag to the last byte of a packet in the transmit FIFO. If it is cleared to "0," the frame is terminated by appending the closing flag to the byte last byte of a packet.

Bit 4: CRC Check Enable (Default = 1)—If this bit is set to "1," then on reception of the closing flag, the result of the CRC check is transferred to the CRC Error bit (bit 2) in the Receive Frame Status Register; otherwise, the CRC result is ignored.

Bit 3: Flag/Mark Idle (Default = 0)—This bit determines what the transmitter sends when not in-frame. If it is set to "1," a flag pattern (01111110) is sent. If it is reset to "0," a mark pattern (11111111) is sent.

Bit 2: Receiver Enable (Default = 0)—When this bit is set to "1" data is clocked into the Serial Bus Port; otherwise, the DLC receiver is disabled and data on the SBIN pin is ignored.

Note that if this bit is cleared while the DLC receiver is in the process of receiving a frame (i.e., the receiver is in-frame), the SBIN pin will not be disabled until the closing flag of the frame being received is detected.

Bit 1: Transmitter Enable (Default = 0)—When set to "1," data from the DLC is shifted out the SBOUT pin under control of SCLK or SFS/XMITCLK; otherwise, the SBOUT pin is disabled.

Note that if this bit is cleared while in the process of sending a frame, the DLC will complete sending the frame before disabling the SBOUT pin.

Bit 0: Send Abort (Default = 0)—When set to "1," the DLC transmitter abort generator transmits abort characters (01111111, LSB on right). If this bit is set and cleared on two successive writes, the DLC will transmit at least one abort character. The transmitter will continue to send these abort patterns for as long as this bit is set. Abort characters are always sent in whole bytes.

Note that when this bit is set the DLC transmit FIFO, DLC byte counter, and the DLC Transmit Byte Count Register will be cleared.

DLC Address Control Register (01 HEX)

All bits in the DLC Address Control Register are set and cleared by software except when initialized to default values as the result of a reset.

The DLC Address Control Register can be written and read by the local processor. When all link address enable bits (bits 3–0) and the broadcast enable bit (bit 4) are cleared to "0," the DLC does not perform address detection, and passes all received frame bytes to the DLC receive FIFO. In this case, bits 7–5 are ignored.

If one or more of the link address enable bits (bits 4–0) are set, then a successful link address compare must occur before any frame bytes can be transferred to the DLC receive FIFO.

7	6	5	4	3	2	1	0
FIRST/ SECOND BYTE SELECT	ENABLE C/R BIT CMPARE	1–2 BYTE ADDR SELECT	ENABLE BRDCST ADDR DETECT	ENABLE ADDR DETECT 3	ENABLE ADDR DETECT 2	ENABLE ADDR DETECT 1	ENABLE ADDR DETECT 0

Bit 7: First/Second Byte Selection (Default = 0)—This bit is ignored unless bit 5 of this register is set to "1." When this bit is set, only the second byte is monitored by the address recognizers (first eight bits are don't cares). When this bit is cleared, only the first byte is examined.

Bit 6: C/R Address Enable (Default = 0)—At least one of the enable bits (4–0) must be set for this bit to have any effect on DLC operation.

If any of the enable bits are set, and the C/R address enable bit is cleared, then bit 1 of the first address byte of each received frame will be ignored.

If this bit is set, then bit 1 of the first received frame address byte must compare successfully along with the other address bits for address recognition to occur.

Bit 5: Address Size 1–2 (Default = 0)—At least one of the enable bits (4–0) must be set for this bit to have any affect on DLC operation.

If any of the enable bits are set and bit 5 is cleared, then the first two address bytes of each received frame will be compared.

If bit 5 is set to "1," only one byte is compared (bit 7 specifies whether the first or second byte is compared).

Bit 4: Broadcast Address Enable (Default = 1)—When set to "1," this bit enables comparison of a receive frame address with an all "1"s (broadcast address) register. The comparison is conditioned by bits 7–5 of this register. When bits 4–0 are cleared, address detection by the DLC is inhibited. If bit 4 is cleared to a zero and one or more of the enable bits (3–0) is set, then the all "1"s pattern is ignored.

Bit 3: Address Register 3 Enable (Default = 0)—Link address 3 enable.

Bit 2: Address Register 2 Enable (Default = 0)—Link address 2 enable.

Bit 1: Address Register 1 Enable (Default = 0)—Link address 1 enable.

Bit 0: Address Register 0 Enable (Default = 0)—Link address 0 enable.

Note: When set to "1," bits 3–0 enable comparison of a received frame address with the contents of the DLC Link Address Recognition Registers 0 through 3, respectively.

The comparison of a received frame address with the contents of all enabled Address Recognition Registers is conditioned by bits 7–5 of this register.

DLC Link Address Recognition Registers (02–03, 04–05, 06–07, 08–09 Hex)

These four registers are two bytes wide with the LSB having the lower address. The LSB of each pair corresponds to the second byte following the flag. The MSB corresponds to the first byte following the flag.

All of the bits in the four Link Address Recognition Registers are set and cleared by software except when initialized to "0"s by a DLC reset or IDPC reset.

Each of these four registers has a corresponding enable bit in the DLC Address Control Register (bits 3–0). If the corresponding enable bit is set, then the value in the Link Address Recognition Register is conditioned by bits 7–5 of the DLC Address Control Register. Default = Hex 0000.

DLC Serial Bus Port Control Register (0A HEX)

All bits in the Serial Bus Port Control Register are set and cleared by software, except when initialized to default values by a DLC reset or IDPC reset. This register can be written and read by the local processor.

7	6	5	4	3	2	1	0
ENABLE REMOTE LOOP BACK	ENABLE LOCAL LOOP BACK	INVERT DATA	CHAN SELECT MSB	CHAN SELECT —	CHAN SELECT —	CHAN SELECT —	CHAN SELECT LSB

Bit 7: Remote Loopback Enable (Default = 0)—This bit is set to enable loopback for diagnostic purposes. When set, the SBIN pin is connected directly to SBOUT. In this manner, receive data is presented to SBOUT as transmitted data. In this mode, the appropriate receive clock is SCLK. Receive data may be presented to the DLC receiver depending on the setting of the receive enable bit.

Bit 6: Local Loopback Enable (Default = 0)—This bit is set to enable loopback for diagnostic purposes. When set, the transmit data path (SBOUT) is connected internally to the receive data path (SBIN is disconnected). The selected transmit clock (either SCLK or SFS/XMITCLK) is used for both the transmit and receive clocks.

Bit 5: Data Invert (Default = 0)—If this bit is set to "1," the serial bit stream being sent or received is inverted at the SBOUT and SBIN pins, respectively. If it is cleared to "0" no inversion takes place.

Bits 4–0: Channel Select—These five bits select Serial Bus Port time slots for multiplexing transmitted serial bit streams/de-multiplexing received serial bit streams.

Bit 4	3	2	1	0	Channel Selection
0	0	0	0	0	Channel 0
0	0	0	0	0	Channel 1
0	0	0	1	0	Channel 2
		⋮			⋮
1	1	1	1	0	Channel 30
1	1	1	1	1	Non-Multiplex Mode

In non-multiplexed mode, a single channel is available with the receiver clocked by the SCLK pin and the transmitter clocked by the SFS/XMITCLK pin. For all settings except non-multiplexed, both the transmitter and the receiver are clocked by the SCLK pin.

If the SFS/XMITCLK pin is held active through the first bit time of time slot 1 in multiplex mode, data in time slot 0 and 1 can be transmitted, and received 16 bits at a time.

DLC Minimum Receive Packet Size Register (0B Hex)

This register specifies the Minimum Receive Packet Size.

7	6	5	4	3	2	1	0
56 kb/s MODE	0	0	0	MIN PKT SIZE MSB	MIN PKT SIZE —	MIN PKT SIZE —	MIN PKT SIZE LSB

Bit 7: 56 kb/s Mode Enable—This bit enables the DLC transmitter and receiver to transmit and receive data at a 56 kb/s data rate instead of the usual 64 kb/s rate.

Bits 6–4: Not used and must be cleared to "0."

Bits 3–0: Minimum Receive Packet Size (Default = Hex 5)—Bits 3–0 of this register are set and cleared by software except when initialized to a default value by a DLC reset or IDPC hardware reset. This register indicates the minimum packet length (exclusive of opening and closing flags) that can be received without generating a short frame error in the Receive Frame Status Register.

At the time that the short frame interrupt is generated, the Receive Byte Count Register reflects the number of bytes in the short frame.

Bit 3	Bit 2	Bit 1	Bit 0	Minimum Packet Size
0	0	0	1	1 Byte
0	0	1	0	2 Bytes
0	0	1	1	3 Bytes
	...	...		...
1	1	1	1	15 Bytes
0	0	0	0	Not Used

Note: Although reception of packets containing only 1, 2, or 3 bytes can be programmed, a minimum of 3 bytes must be received before data is moved into the FIFO and the packet is reported.

DLC Maximum Receive Packet Size Register (OC(LSB) – OD(HSB) Hex) (Default = 0000 Hex)

This register indicates the maximum packet length (exclusive of opening and closing flags) that can be received without generating a long frame error in the Receive Frame Status Register. The value programmed into the register should be equal to the desired packet size minus three.

Note that the receive byte counter is incremented on 8-bit boundaries and therefore is compared with the Maximum Receive Packet Size register each time a character is transferred from the receive shift register to the receive FIFO. The LONG FRAME ERROR status bit (bit 4) in the DLC Receive Frame Status Register will be set to "1" when the programmed value is exceeded. When this occurs, the state of the ENABLE FCS PASS-THRU ENABLE bit (bit 7) in the DLC Command/Control Register will determine the total number of characters passed to system memory. If this bit is set to "1," the total number of characters passed through to the receive FIFO and system memory will equal to the maximum count programmed plus 3. If this bit is reset to "0," the maximum characters transferred will equal the maximum count programmed plus 1.

DLC Interrupt Source Interrupt Enable Register (0E Hex)

7	6	5	4	3	2	1	0
ENABLE RECVR LINK STATUS	ENABLE FIFO STATUS	ENABLE RECV FRAME STATUS	ENABLE VALID PACKET SENT	ENABLE VALID PACKET RECVD	0	0	0

Bits 4 and 3 provide single-level interrupt enable/disable control for valid packet received and valid packet sent status conditions. For bits 7–5, the Interrupt Source Interrupt Enable Register contains the first-level enable of a two-level interrupt enable structure. Bits 7–5 enable three corresponding Interrupt Enable Registers:

Receive Frame Interrupt Enable Register
Receive Link Interrupt Enable Register
FIFO Status Interrupt Enable Register

The valid packet received and valid packet sent interrupts have a single-level interrupt enable structure (bits 3 and 4 of the Interrupt Source Interrupt Enable Register).

When an event occurs that causes a bit to be set in one of the three status registers (Receive Frame, Receive Link, and FIFO Status Registers), and both levels of status interrupt enable are set to "1," the DLC interrupt is generated and the bit corresponding to that register is set in the DLC Interrupt Source Register. Unless both levels of interrupt enable are set, no interrupt is generated.

Bit 7: Enable Receive Link Status (Default = 0)—This bit is set as the first level of enable for the Receive Link Status Enable Register. If a status bit is set in the Receive Link Status Register, and the corresponding bit is set in the Receive Link Status Interrupt Enable Register, and bit 7 of this register is set, an interrupt is generated and bit 7 of the Interrupt Source Register is set to indicate the interrupt originated in the Receive Link Status Register.

Bit 6: Enable FIFO Status Interrupt (Default = 0)—This bit is set as the first level of enable for the FIFO Status Interrupt Enable Register. If a status bit is set in the FIFO Status Register, and the corresponding bit is set in the FIFO Status Interrupt Enable Register, and bit 6 of this register is set, an interrupt is generated and bit 6 of the Interrupt Source Register is set to indicate the interrupt originated in the FIFO Status Register.

Bit 5: Enable Receive Frame Status Interrupt (Default = 0)—This bit is set as the first level of enable for the Receive Frame Interrupt Enable Register. If a status bit is set in the Receive Frame Status Register, and the corresponding bit is set in the Receive Frame Interrupt Enable Register, and bit 5 of this register is set, an interrupt is generated and bit 5 of the Interrupt Source Register is set to indicate the interrupt originated in the Receive Frame Status Register.

Bit 4: Enable Valid Packet Sent Interrupt (Default = 0)—If this bit is set and the valid packet sent bit is set in the Interrupt Source Register, a DLC interrupt is generated. If this bit is cleared, setting of the valid packet sent bit in the Interrupt Source Register does not generate an interrupt.

Bit 3: Enable Valid Packet Received Interrupt (Default = 0)—If this bit is set and the valid packet received bit is set in the Interrupt Source Register, a DLC interrupt is generated. If this bit is cleared, setting of the valid packet received bit in the Interrupt Source Register does not generate an interrupt.

Bits 2–0:—Not used and must be cleared to "0."

1

DLC Receive Frame Interrupt Enable Register (0F Hex)

The Receive Frame Interrupt Enable Register contains a bit-for-bit image of the Receive Frame Status Register. If a status bit is set in the Receive Frame Status Register corresponding to a set bit in the Receive Frame Interrupt Enable Register, and bit 5 of the first-level enable register (Interrupt Source Interrupt Enable Register) is set, a DLC interrupt is generated and bit 5 of the Interrupt Source Register is set indicating the interrupt originated in the Receive Frame Status Register.

7	6	5	4	3	2	1	0
0	0	ENABLE OVRRUN ERROR	ENABLE LONG FRAME ERROR	ENABLE SHORT FRAME ERROR	ENABLE CRC ERROR	ENABLE NON-INT # BYTES ERROR	ENABLE ABORT RECVD

Bits 7-6:—Not used and must be cleared to "0."

Bit 5: Enable Overrun Error Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 5) is set, setting this bit enables a DLC interrupt if the overrun error bit (bit 5) is set in the Receive Frame Status Register.

Bit 4: Enable Long Frame Error Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 5) is set, setting this bit enables a DLC interrupt if the long frame error bit (bit 4) is set in the Receive Frame Status Register.

Bit 3: Enable Short Frame Error Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 5) is set, setting this bit enables a DLC interrupt if the short frame error bit (bit 3) is set in the Receive Frame Status Register.

Bit 2: Enable CRC Error Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 5) is set, setting this bit enables a DLC interrupt if the CRC error bit (bit 2) is set in the Receive Frame Status Register.

Bit 1: Enable Non-Integer Number Bytes Received Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 5) is set, setting this bit enables a DLC interrupt if the non-integer number bytes received bit (bit 1) is set in the Receive Frame Status Register.

Bit 0: Enable Abort Received Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 5) is set, setting this bit enables a DLC interrupt if the abort received bit (bit 0) is set in the Receive Frame Status Register.

DLC Receive Link Interrupt Enable Register (10 HEX)

This register is used to enable/disable interrupts from the Receive Link Status Register (Default = 0).

7	6	5	4	3	2	1	0
0	0	0	0	0	ENABLE IN-FRAME ERROR	ENABLE FLAG IDLE RECVD	ENABLE MARK IDLE RECVD

Bits 7–3:—Not used and must be cleared to "0."

Bit 2: Enable Change In In-Frame Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 7) is set, setting this bit enables a DLC interrupt if the change in in-frame bit (bit 2) is set in the Receive Link Status Register.

Bit 1: Enable Change In Flag Idle Received Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 7) is set, setting this bit enables a DLC interrupt if the change in flag idle received bit (bit 1) is set in the Receive Link Status Register.

Bit 0: Enable Change In Mark Idle Received Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 7) is set, setting this bit enables a DLC interrupt if the change in mark idle received bit (bit 0) is set in the Receive Link Status Register.

DLC FIFO Status Interrupt Enable Register (11 HEX)

This register is used to enable/disable interrupts from the FIFO Status Register (Default = 0).

7	6	5	4	3	2	1	0
0	0	ENABLE EOP RECV FIFO	ENABLE XMIT UNDRUN REACHD	ENABLE XMIT BUFFER AVAIL	ENABLE XMIT TRSHLD REACHD	ENABLE RECV DATA AVAIL	ENABLE RECV TRSHLD REACHD

Bits 7-6:—Not used and must be cleared to "0."

Bit 5: Enable EOP In Receive FIFO Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 6) is set, setting this bit enables a DLC interrupt if the EOP in receive FIFO bit (bit 5) is set in the FIFO Status Register.

Bit 4: Enable Transmit Underrun Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 6) is set, setting this bit enables a DLC interrupt if the transmit underrun bit (bit 4) is set in the FIFO Status Register.

Bit 3: Enable Transmit Buffer Available Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 6) is set, setting this bit enables a DLC interrupt if the transmit buffer available bit (bit 3) is set in the FIFO Status Register.

Bit 2: Enable Transmit Threshold Reached Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 6) is set, setting this bit enables a DLC interrupt if the transmit threshold reached bit (bit 2) is set in the FIFO Status Register.

Bit 1: Enable Receive FIFO Data Available Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 6) is set, setting this bit enables a DLC interrupt if the receive FIFO data available bit (bit 1) is set in the FIFO Status Register.

Bit 0: Enable Receive Threshold Reached Interrupt (Default = 0)—If the first level of interrupt (Interrupt Source Interrupt Enable Register, bit 6) is set, setting this bit enables a DLC interrupt if the receive threshold reached bit (bit 0) is set in the FIFO Status Register.

DLC Transmit Byte Count Register (12 (LSB) – 13(MSB) Hex) (Default = 0)

This register is written by software when the number of bytes to be transmitted is different from the current value stored in the Transmit Byte Count Register (exclusive of opening and closing flags and FCS bytes).

The register contents are written to the transmit byte counter whenever software writes the least significant byte of this register pair (if the transmitter is out of frame), or when the last byte of a packet is loaded from the transmit FIFO into the parallel-to-serial shift register. If a write to this register occurs as the last byte of a packet is being loaded, the transfer to the transmit byte counter is delayed until the write is complete. The MSB of the this register must be written first because the transmit byte counter is loaded immediately after the LSB of this register is written. A transmit FIFO underrun error clears this register.

Transmit Byte Count Decode:

Bits																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Value Selected
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1 Byte
							...									...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65,535 kbytes
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Not Assigned

DLC FIFO Threshold Register (14 Hex)

This register is used to specify the transmit and receive FIFO threshold levels.

7	6	5	4	3	2	1	0
RECV TRSHLD MSB	RECV TRSHLD —	RECV TRSHLD —	RECV TRSHLD LSB	XMIT TRSHLD MSB	XMIT TRSHLD —	XMIT TRSHLD —	XMIT TRSHLD LSB

Bits 7–4: Receive FIFO Threshold (Default = Hex 8)—The receive FIFO threshold counts by two since the receive FIFO buffer is 32 bytes deep.

Bit 7	6	5	4	Receive Threshold
0	0	0	1	2 Bytes
0	0	1	0	4 Bytes
0	0	1	1	6 Bytes
	...	...		...
1	1	1	1	30 Bytes
0	0	0	0	32 Bytes

Bits 3–0: Transmit Threshold Value (Default = Hex 8)—The contents of this register are set and cleared under software control except when initialized by a DLC reset or IDPC reset or when an abort is issued.

Bit 3	2	1	0	Receive Threshold
0	0	0	1	1 Byte
0	0	1	0	2 Bytes
0	0	1	1	3 Bytes
	...	...		...
1	1	1	1	15 Bytes
0	0	0	0	16 Bytes

DLC Interrupt Source Register (15 HEX)

This register is used to identify the source of interrupting conditions and to report valid-packet-transmitted, valid-packet-received.

7	6	5	4	3	2	1	0
RECV LINK STATUS	FIFO STATUS	RECV FRAME STATUS	VALID PACKET SENT	VALID PACKET RECVD	RECV ADDR MSB	RECV ADDR —	RECV ADDR LSB

Bit 7: Receive Link Status (Default = 0)—This bit is set to "1" when any bit in the Receive Link Status Register is set and both of the corresponding bits in the Receive Frame Interrupt Enable Register and bit 7 (enable received link status interrupt bit) are set in the Interrupt Source Interrupt Enable Register.

It is cleared to "0" when the Receive Link Status Register is read by software, a DLC reset is executed, or an IDPC reset is received from the processor.

Bit 6: FIFO Status (Default = 0)—This bit is set to "1" when any bit in the FIFO Status Register is set and both of the corresponding bits in the Receive Frame Interrupt Enable Register and enable FIFO status interrupt (bit 6) are set to "1" in the Interrupt Source Interrupt Enable Register.

It is cleared to "0" when the FIFO Status Register is read by software, a DLC reset is executed, or an IDPC reset is received from the processor.

Bit 5: Receive Frame Status (Default = 0)—This bit is set to "1" when any bit in the Receive Frame Status Register and both of the corresponding bits in the Receive Frame Interrupt Enable Register and enable receiver frame interrupt bit (bit 5) are set in the Interrupt Source Interrupt Enable Register.

This bit is gated when stage 3 status is actually transferred to stage 4. (See description of delayed status reporting.)

Bit 5 is cleared to 0 when the Receive Frame Status Register is read by software, a DLC reset is executed, or an IDPC reset is received from the processor.

Bit 4: Valid Packet Sent (Default = 0)—This bit is set to "1" when the last bit before the closing flag has been transmitted by the DLC transmitter (transmit byte counter = 0 and no underrun and transmitter out of frame). It is cleared when the transmitter goes in-frame, this register is read, a DLC reset is executed, or an IDPC reset occurs.

Bit 3: Valid Packet Received (Default = 0)—This bit is reset to its default value when a DLC reset is executed or an IDPC reset is received. It is set to "1" when the last byte of a packet is read from the receive FIFO buffer and no receive error has been detected for that packet. It is cleared when software reads this register, or a DLC reset or IDPC reset occurs.

Bits 2–0: Receive Address Field (Default = 110 (0 = LSB))—The receive link address field is written by hardware whenever a packet is received (with or without errors). It is a delayed-stacked field.

The link address for up to four received packets can be stored at any given time. The address field for any packet is not presented to the user until the last byte of that packet is read from the FIFO.

Bits 2	1	0	Definition
0	0	0	Contents of Link Address 0 Recognized
0	0	1	Contents of Link Address 1 Recognized
0	1	0	Contents of Link Address 2 Recognized
0	1	1	Contents of Link Address 3 Recognized
1	0	0	Broadcast Link Address (All "1"s) Recognized
1	0	1	Not Used
1	1	0	Default Value—No Packet Received
1	1	1	Packet Received with no Address Recognized enabled (Bits 4–0 of DLC Address Control Register cleared to "0s")

DLC Receive Byte Count Register (16(LSB) –17(MSB)Hex) (Default = 0)

This 16-bit register indicates the number of bytes received in a packet, not including the opening and closing flags, whether the packet was received in error or not. The actual counter is incremented each time a byte is loaded into the FIFO.

This register is a "read-only" register, and is cleared to "0" when a DLC reset is executed or an IDPC reset is received from the processor.

This register presents information in a delayed fashion. When the last byte of a packet is read from the receive FIFO, the receive byte count is made available to the user. If a new packet is received before the status from the previous packet is read by the user, the status for the new packet is stacked behind the previous packet. Status for up to four packets can be stacked at any given time. When the four-deep stack is full, the DLC receiver ignores new packets until the status from at least one packet is read by the user.

There are two mechanisms that ensure synchronization between packet data and status: 1) data from one packet cannot be read from the FIFO until status from the previous packet is read; and 2) when the least-significant byte of the Receive Byte Count Register is read, all of the delayed stacked registers for that packet are cleared (Receive Byte Count Register, Receive Frame Status Register, Residual Bit Register, and the received address field of the Interrupt Source Register). For this reason, the LSB of the Receive Byte Count Register should always be read last.

Receive Byte Count Decode:

Bits 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Value Selected
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1 byte
							...									...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65,535 kbytes

DLC Receive Frame Status Register (18 HEX)

This is a "read-only" register. The setting of any bit in this register will result in the setting of bit 5 in the Interrupt Source Register if the corresponding bit is set in the Receive Frame Interrupt Enable Register, and the receive frame status bit is set in the Interrupt Source Interrupt Enable Register.

This register is a delayed-stacked register. Status is not reported until the last byte of the packet is read from the FIFO. At that time maskable interrupts are generated. Status for up to four packets can be stacked at any given time.

The bits of this register are cleared to "0" (default setting) when a DLC reset is executed, the IDPC reset pin is activated, or when this register or the LSB of the Receive Byte Count Register is read.

It is possible that more than one receive error may occur simultaneously on the same receive bit. However, only one bit in this register may be set to "1" at any time. The following table indicates the precedence of the various errors and exception conditions flagged by this register (listed in descending order of precedence):

If the Receive Frame Status Register is not read (not normally read for a valid packet) before the LSB of the Receive Byte Count Register, reading the Receive Byte Count Register will clear the Receive Frame Status Register to keep the register in sync (i.e., read Receive Byte Count Register LSB last).

7	6	5	4	3	2	1	0
0	0	OVRRUN ERROR	LONG FRAME ERROR	SHORT FRAME ERROR	CRC ERROR	NON-INT # BYTES RECVD	ABORT RECVD

Bits 7–6: Not used and must be cleared to "0."

Bit 5: Overrun Error (Default = 0)—This bit is set to "1" as a result of the DLC receive FIFO detecting an overrun condition (i.e., the receive FIFO contains 32 bytes when receive data needs to be moved into the FIFO from the Parallel-to-Serial Shift Register).

Bit 4: Long Frame Error (Default = 0)—This bit is set to "1" as a result of the DLC receiver detecting a long frame error.

Bit 3: Short Frame Error (Default = 0)—This bit is set to "1" as a result of the DLC receiver detecting a short frame error.

Bit 2: CRC Error (Default = 0)—This bit is set to "1" as a result of the DLC CRC checker detecting an error when CRC check is enabled in the DLC Command/Control Register.

Bit 1: Non-Integer Number Bytes Received (Default = 0)—This bit is set to "1" as a result of the DLC receiver flag detector recognizing a closing flag character with at least three bytes received when a non-integer number of bytes has been received in a non-short frame (i.e., at least one but less than eight bits were received after zero bit deletion in the byte immediately preceding the closing flag).

Bit 0: Abort Received (Default = 0)—This bit is set to "1" as a result of the DLC receiver abort detector detecting an abort character (seven "1"s while in-frame) while the DLC receiver is in-frame and at least three bytes have been received.

DLC Receive Link Status Register (19 HEX)

The Receive Link Status Register reflects the status of the data link at the receiver input. Three conditions are monitored: mark idle, flag idle, and in-frame. Bits 5–3 reflect the current status of the link and do not generate interrupts. Bits 2–0 reflect changes in the link since the register was last read; maskable interrupts are associated with these bits. At reset, bits 2–0 are cleared and bits 5–3 are cleared by the hardware that sets them.

Bits 7–6: Not used and must be cleared to "0."

Bit 5: In-Frame Received (Default = 0)—This bit is set to "1" when the receiver goes in-frame and is cleared when the receiver is not in-frame.

Bit 4: Flag Idle Received (Default = 0)—This bit is set to "1" to indicate a flag idle condition on the data link and is cleared when flag idle is not being received.

7	6	5	4	3	2	1	0
0	0	INFRAME RECVD	FLAG IDLE RECVD	MARK IDLE RECVD	CHANGE IN INFRAME	CHANGE IN FLAG IDLE	CHANGE IN MARK IDLE

Bit 3: Mark Idle Received (Default = 0)—This bit, is set to "1" to indicate a mark idle condition on the data link and is cleared when mark idle is not being received.

Bit 2: Change In In-Frame (Default = 0)—This bit, when set, indicates that the in-frame bit (bit 5) has changed (either set or cleared) since the last time the register was read. This bit is cleared by reading the register, a DLC reset, or an IDPC reset.

Bit 1: Change In Flag Idle (Default = 0)—This bit, when set, indicates that the flag idle bit (bit 4) has changed (either set or cleared) since the last time the register was read. This bit is cleared by reading the register, a DLC reset, or an IDPC reset.

Bit 0: Change In Mark Idle (Default = 0)—This bit, when set, indicates that the mark idle bit (bit 3) has changed (either set or cleared) since the last time the register was read. This bit is cleared by reading the register, a DLC reset, or an IDPC reset.

DLC FIFO Status Register (1A HEX)

Each of the FIFO Status Register bits are set and cleared by DLC hardware to indicate the real-time status of the various conditions.

The bits of this register will be set or cleared to their default values by either a DLC or IDPC reset.

Setting any bit in this register will set bit 6 of the Interrupt Source Register providing the corresponding enable bit is set in the FIFO Status Interrupt Enable Register and the enable FIFO status interrupt bit 6 is set in the Interrupt Source Interrupt Enable Register.

7	6	5	4	3	2	1	0
0	0	EOP IN RECV FIFO	XMIT UNDRUN	XMIT BUFFER AVAIL	XMIT TRSHLD REACHD	RECV DATA AVAIL	RECV TRSHLD REACHD

Bits 7–6: Not used and must be cleared to "0."

Bit 5: EOP In Receive FIFO (Default = 0)—This bit is set to "1" to indicate that the last byte of a packet has been loaded into the receive FIFO. It remains set until no EOP tags remain in the FIFO. This is the packet received indication, and is normally used in non-DMA applications to indicate that the FIFO requires servicing.

Bit 4: Transmit Underrun (Default = 0)—This bit is set to "1" during data transmission when the transmit FIFO goes empty and the transmit byte counter is not equal to zero, and is cleared when the FIFO Status Register is read.

An abort will automatically be transmitted in response to a transmit underrun condition.

Bit 3: Transmit Buffer Available (Default = 0)—This bit is set to "1" whenever the DLC FIFO Data Register is empty, and the transmit byte counter is not equal to zero (i.e., available to be written into). This bit remains active as long as the transmit FIFO is not full, and is cleared when the last byte of a packet is loaded in the FIFO. This prevents multiple packets from existing in the FIFO at the same time (non-DMA users).

Bit 2: Transmit Threshold Reached (Default = 0)—This bit is set to "1" when the number of bytes in the DLC transmit FIFO is less than or equal to the count in the transmit FIFO threshold bit field (bits 3–0 of the FIFO Threshold Register).

This bit is cleared to a "0" when the number of bytes in the transmit FIFO becomes greater than the transmit FIFO threshold bit field value. This status bit is used to condition the DLC transmit DMA data request signal.

Bit 1: Receive Data Available (Default = 0)—This bit is set to "1" whenever a byte is available in the DLC receive FIFO Data Register, and is cleared to "0" when a byte is read and the receive FIFO becomes empty. It is also cleared when the last byte of a packet is read from the FIFO. Under this condition, it is not re-enabled until the user reads the LSB of the Receive Byte Count Register. This, in conjunction with the packet received interrupt, notifies the non-DMA user when the last byte of a packet has been read.

Bit 0: Receive Threshold Reached (Default = 0)—This bit is set to "1" when the number of bytes in the DLC receive FIFO becomes equal to the value programmed in the receive FIFO threshold bit field of the DLC FIFO Threshold Register.

This bit is cleared to "0" when the number of bytes in the receive FIFO byte counter becomes less than the receive threshold value programmed in the DLC FIFO Threshold Register.

DLC FIFO Data Registers

The receive FIFO and transmit FIFO Data Registers are 8-bit registers.

The receive FIFO Data Register is read by DMA or software to remove a byte from the receive FIFO. If read by software, the user should first poll the receive FIFO data available status bit (bit 1 in the FIFO Status Register), unless data is being read in response to a threshold reached indication in which case the number of bytes to be read is known.

The transmit FIFO Data Register is written by DMA or software. If written by software, the user should first poll the transmit FIFO buffer available status bit (bit 3 in the FIFO Status Register) to ensure that a byte is available in the FIFO (unless the data is being loaded in response to a threshold reached indication, in which case the number of bytes that can be loaded is known).

DLC Residual Bit Status/Control Register (1D Hex)

This read/write register controls the number of bits transmitted in the last byte of a packet and displays the number of valid data bits received in the last byte of a packet. It is also the register used to enable the Transparent mode.

7	6	5	4	3	2	1	0
TRANS. MODE ENABLE	TRANS. MODE SELECT	XMIT RESIDUE COUNT MSB	XMIT RESIDUE COUNT —	XMIT RESIDUE COUNT LSB	RECVD RESIDUE COUNT MSB	RECVD RESIDUE COUNT —	RECVD RESIDUE COUNT LSB

Bit 7: Transparent Mode Enable—This bit enables data to be sent or received without any HDLC protocol related format.

Bits 6: Transparent Mode Select—This bit determines whether data transmission and reception is controlled by their respective transmitter/receiver enable control signals or maximum byte counts programmed. This bit is ignored if bit 7 of this register is cleared to "0."

Bits 5–3: Transmitter Residue Count (Default = 000)—These three bits specify the number of residue bits to be transmitted in the last byte of a packet. This is a read/write field that is cleared under software control.

Bits 5	4	3	Residue Bits
0	0	0	8 Bits
0	0	1	1 Bit
0	1	0	2 Bits
	...		...
1	0	0	7 Bits

Bits 5	4	3	Residue Bits
0	0	0	8 Bits
0	0	1	1 Bit
0	1	0	2 Bits
	...		...
1	0	0	7 Bits

Bits 2–0: Received Residue Count (Default = 000) —These three bits form a "read-only" field displaying the number of residue bits received. This field is cleared to "0"s upon reset or by reading this register or reading the LSB of the receive byte counter. This field is a delayed-stacked field. Status for up to four packets may be stacked at any one time.

Detailed Description of User-Visible USART Registers

Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The programmable features of the USART include:

Character Length—character length is user-selectable (5-, 6-, 7-, or 8-bit characters).

Parity— even, odd, or no parity options are selectable. In addition, "stick" Parity test mode is provided.

Stop Bits—1 or 2 Stop Bits may be selected for 6-, 7-, or 8-bit characters; 1 or 1½ Stop Bits may be selected for use with 5-bit characters.

Data Rates—USART supports data rates from 300 to 64 kb/s in both asynchronous and synchronous modes.

Handshake Lines—the USART provides $\overline{RTS}$ and $\overline{DTR}$ assertion through software control and allows for status checking of $\overline{CTS}$ and $\overline{DSR}$.

Operational Modes—the USART may be programmed for asynchronous or synchronous operation.

Baud Rate Generator—a programmable internal baud rate generator allows a selectable clock rate for asynchronous operation. Either mode allows selection of an external clocking source.

Break Generation—software break character generation.

FIFO Thresholds—each 4-byte transmit and receive FIFO has a selectable threshold value up to 4 bytes. Upon reaching the threshold value, the USART may be programmed to interrupt the external processor.

Special Character Recognition—the user may define one or more characters as special characters, and can enable when a special character is detected. Up to 128 characters can be selected as special. If 5-, 6-, or 7-bit character lengths are selected, any combination of characters may be selected as special. If 8-bit character length is used, characters with bit patterns of 0–127 may be selected as special.

Interrupts—any of the following interrupts may be selectively enabled or disabled:

- Change in $\overline{CTS}$
- Change in $\overline{DSR}$
- Parity Error
- Receive FIFO Threshold Reached
- Receive FIFO Timeout
- Transmit Shift Register Empty
- Break Detect
- Special Character Detect
- Framing Error
- Buffer Overrun

The USART contains 14 registers, as shown in Table 3.

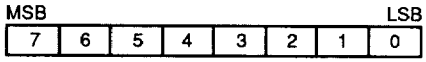
Table 3. USART Registers

Offset (Hex)	Register Name	Size (Bytes)	Type
20	Receive FIFO Data Register (DLAB = 0)*	1	Read Only
	Transmit FIFO Data Register (DLAB = 0)	1	Write Only
	Baud Rate Divisor LSB Register (DLAB = 1)	1	Read/Write
21	Interrupt Enable Register (DLAB = 0)	1	Read/Write
	Baud Rate Divisor MSB Register (DLAB = 1)	1	Read/Write
22	Interrupt Identification Register	1	Read Only
23	Line Control Register	1	Read/Write
24	Modem Control Register	1	Read/Write
25	Line Status Register	1	Read Only
26	Modem Status Register	1	Read Only
27	Control Register	1	Read/Write
28	Status Register	1	Read Only
29	Special Character Bit-Map Address Pointer Register	1	Read/Write
2A	Special Character Bit Map Command Register	1	Read/Write
2B–3E	Reserved	20	—

*Divisor Latch Access Bit (DLAB) in the Line Control Register.

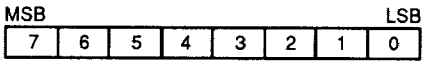
USART Receive FIFO Data Register (Default = 0) (20 Hex, DLAB =0)

The Receive FIFO Data Register is a "read-only" register. Data received by the USART is read from the receive FIFO by the CPU at this address.



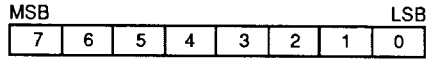
USART Transmit FIFO Data Register (Default = 0) (20 Hex, DLAB = 0)

The Transmit FIFO Data Register is a "write-only" input to the transmit FIFO. Data written in this 8-bit register is transmitted out of the TxD pin LSB first.



USART Baud Rate Divisor LSB Register (Default = 0) (20 Hex, DLAB = 1)

The Baud Rate Divisor LSB Register is an 8-bit register used to hold the LSB of the 16-bit baud rate divisor.



USART Baud Rate Divisor MSB Register (Default = 0) (21 Hex, DLAB = 1)

The Baud Rate Divisor MSB Register is an 8-bit register used to hold the MSB of the 16-bit baud rate divisor.

Note: Divide-by-one passes the USARTCLK unaffected. This allows the receiver and transmitter to operate from separate clocks in synchronous mode. A write to either the MSB or LSB Divisor Registers loads the baud rate generator with a 16-bit value.

Note: When executing a reset, the register pair is cleared to all zeros, but the baud rate generator will divides the USARTCLK by 64 until the Baud Rate Registers are programmed.

Bits															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**Divide By:**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Reserved
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1 Byte
							...									...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65,535 kbytes

USART INTERRUPT ENABLE REGISTER (21 HEX, DLAB = 0)

The Interrupt Enable Register is an 8-bit read/write register used to enable specific interrupt sources (Default = 0). Setting a bit enables its corresponding interrupt. Clearing a bit disables the interrupt and resets the interrupt pin if the corresponding condition is present.

7	6	5	4	3	2	1	0
0	XMIT STATUS: SHFTREG EMPTY	USART STATUS: SPCL CHAR.	USART STATUS: Rx FIFO TIMEOUT	MODEM STATUS: CTS DSR	RECV LINE STATUS	XMIT FIFO TRSHLD	RECV FIFO TRSHLD

USART INTERRUPT IDENTIFICATION REGISTER (22 HEX)

The Interrupt Identification Register is an 8-bit read-only register that identifies which status register contains an interrupt condition. Unused bit positions (bits 7–4) return "0"s when this register is read.

7	6	5	4	3	2	1	0
0	0	0	0	INTR SOURCE MSB	INTR SOURCE —	INTR SOURCE LSB	INTR PEND

Bits 7–4: Not Used and must be cleared to "0."

Bits 3–1: Interrupt Source (Default = 000)—This 3-bit field identifies the highest priority source of all existing interrupts.

Bit 0: Interrupt Pending (Default = 1)—This bit is cleared to "0" if any interrupt is pending.

Interrupt Source Decode

Bits 3	2	1	Priority	Source	Reset By*
0	0	0	4th	CTS or DSR	Reading the Modem Status Register
0	0	1	3rd	Transmit FIFO Threshold Reached	Reading this Register and Interrupt Source = 001
0	1	0	2nd	Receive FIFO Threshold Reached	Reading this Register and Interrupt Source = 010
0	1	1	1st**	Overrun, Parity, Special Character Received, Framing, or Break	Reading Line Status Register
1	0	0	5th	Receive FIFO Timeout	Reading USART Status Register
1	0	1	6th	Transmit Shift Register Empty	Reading this Register and Interrupt Source = 101

* All bits are reset by a USART reset or an IDPC reset.

** Simultaneous receipt of a special character or a character with a parity error, and a threshold reached condition generates the interrupt for the special character or parity error before the threshold reached interrupt.

USART LINE CONTROL REGISTER (23 HEX)

This register controls access to the Baud Rate Generator Divisor registers and sets the mode of operation for the USART.

7	6	5	4	3	2	1	0
DIV LATCH ACCESS BIT	BREAK	STICK PARITY	EVEN/ ODD PARITY SELECT	PARITY ENABLE	STOP BIT LENGTH	CHAR LENGTH MSB	CHAR LENGTH LSB

Bit 7: Divisor Latch Access Bit—This bit is used to enable access to the Baud Rate Divisor Registers. If it is set to "1," access to these registers is enabled, but must be reset to "0" before accessing the receive/ transmit FIFO Data Registers and the Interrupt Enable Register.

Bit 6: Break—This bit is set to request that a break condition be transmitted. The USART will transmit the break pattern immediately after completing any character transmission in progress when this bit is set. The transmit shift register and transmit FIFO contents are discarded. The line returns to normal operation when the bit is cleared. Breaks are transmitted only in asynchronous mode.

Bit 5: Stick Parity—If parity is enabled (bit 3 set) and this bit is set to "1," parity is expected to be received opposite to that indicated by bit 4. Parity is transmitted with a value opposite that of bit 4.

Bit 4: Even/Odd Parity Select—This bit selects the parity sense used by the transmitter and receiver. If it is set to "1"; even parity is selected. If it is reset to "0"; odd parity is selected.

Bit 3: Parity Enable—When this bit is set to "1," parity generation and checking is enabled. When this bit is cleared, parity generation and checking is disabled.

Bit 2: Stop Bit Length—This bit selects the number of stop bits used in serial data transfers.

0 = 1 Stop Bit
1 = 1.5 Stop Bits (5-bit characters) or 2 Stop Bits (6-, 7-, or 8-bit characters)

Bit 1–0: Character Length—Bits 1 and 0 define the character length.

Bits 1	0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

USART Modem Control Register (24 HEX)

This register specifies modem control parameters (Default = 0).

7	6	5	4	3	2	1	0
0	0	0	LOCAL LOOPBK ENABLE	RESRVD	RESRVD	$\overline{\text{RTS}}$ PIN CONTR	$\overline{\text{DTR}}$ PIN CONTR

Bits 7–5: Not used and must be cleared to "0."

Bit 4: Local Loopback Enable—Setting this bit to "1" places the USART in a local loop back condition for diagnostic purposes.

Bits 3–2: Reserved

Bit 1: $\overline{\text{RTS}}$ Pin Control—When this bit is set to "1," $\overline{\text{RTS}}$ pin goes active-Low. This bit does not directly control the transmitter.

Bit 0: $\overline{\text{DTR}}$ Pin Control—When this bit is set to "1," the $\overline{\text{DTR}}$ pin goes active-Low. This bit does not directly control the transmitter or receiver.

USART Line Status Register (25 HEX)

The USART Line Status Register contains flag bits that are set to indicate the presence of a condition that can generate an interrupt if the appropriate interrupt enable bits are set in the Interrupt Enable Register. Bits 1 through 4 and 7 are cleared by reading this register. Bit 5 is cleared when the condition goes away, but the interrupt is cleared by reading the Interrupt Identification Register (when the Interrupt Identification Register is reporting this interrupt). Bits 0 and 6 are cleared when the associated conditions are no longer present.

7	6	5	4	3	2	1	0
SPCHL CHAR IN FIFO	XMIT SHIFT REG EMPTY	XMIT TRSHLD REACHD	BREAK DETECT	FRAMING ERROR	PARITY ERROR IN FIFO	RECV BUFFER OVRRUN	RECV DATA AVAIL

Bit 7: Special Character In FIFO (Default = 0)—This bit is set to "1" when a special character is transferred into the receive FIFO, and cleared when the USART Line Status Register is read.

Bit 6: Transmit Shift Register Empty (Default = 1)—This bit is set to "1" when the transmit shift register is empty (i.e. the last character transmitted) and cleared when the transmit shift register and FIFO are not empty.

Bit 5: Transmit FIFO Threshold Reached (Default = 1)—This bit is cleared when the number of bytes in the transmit FIFO rises above the programmed threshold, and is set to "1" when the FIFO level is equal to or below the threshold.

Bit 4: Break Detected (Default = 0)—This bit is set to "1" when a break condition is detected by the receiver, and is cleared when the USART Line Status register is read.

Bit 3: Framing Error (Default = 0)—This bit is set to "1" when an invalid stop bit is detected. A character with a framing error is not loaded into the FIFO, and is cleared when the USART Line Status register is read.

Bit 2: Parity Error in FIFO (Default = 0)—This bit is set to "1" when a character with a parity error is transferred into the receive FIFO from the receive shift register, and is cleared when the USART Line Status register is read.

Bit 1: Receive Buffer Overrun (Default = 0)—This bit is set to "1" when an overrun error results in lost receive data, and is cleared when the USART Line Status register is read.

Bit 0: Receive Data Available (Default = 0)—This bit is set to "1" when receive data is available in the receive FIFO Data Register.

USART Modem Status Register (26 HEX)

The 8-bit Modem Status Register is used to indicate the condition of the link handshake input signals and any change in their status. Bits 1 and 0 are cleared on reset; bits 5 and 4 reflect the input status.

7	6	5	4	3	2	1	0
RESRVD	RESRVD	$\overline{DSR}$ PIN STATUS	$\overline{CTS}$ PIN STATUS	RESRVD	RESRVD	$\overline{DSR}$ PIN CHANGE STATUS	$\overline{CTS}$ PIN CHANGE STATUS

Bits 7–6: Reserved

Bit 5: **$\overline{DSR}$ Pin Status**—This bit is set to "1" if the $\overline{DSR}$ input pin is active-Low and cleared to a "0" if $\overline{DSR}$ is inactive.

Bit 4: **$\overline{CTS}$ Pin Status**—This bit is set to "1" if the $\overline{CTS}$ input pin is active-Low and is cleared to a "0" if $\overline{CTS}$ is inactive.

Bits 3-2: Reserved

Bit 1: **$\overline{DSR}$ Pin Change Status (Default = 0)**—This bit is set to "1" when a change in the $\overline{DSR}$ input pin has occurred since this register was last read.

Bit 0: **$\overline{CTS}$ Pin Change Status (Default = 0)**—This bit is set to "1" if the input pin has changed state since this register was last read.

USART Control Register (27 HEX)

This 8-bit USART register is used to control all non-8250-UART functions. Additionally, this register contains the USART software reset bit.

7	6	5	4	3	2	1	0
RESET	XMIT FIFO TRSHLD MSB	XMIT FIFO TRSHLD LSB	RECV FIFO TRSHLD MSB	RECV FIFO TRSHLD LSB	SYNC/ ASYNC MODE SELECT	XMIT CLK SOURCE	RECV CLK SOURCE

Bit 7: Reset (Default = 0)—This bit is set to initiate a USART reset operation (identical to a reset initiated by hardware via the RST pin, except only the USART is affected). The software reset takes 2 master clock cycles, and this bit clears itself.

Bits 6–5: Transmit FIFO Threshold (Default = 00)—This field is used to hold a 2-bit count that reflects the transmit FIFO threshold. When the number of bytes remaining in the transmit FIFO is less than or equal to this level, Transmit FIFO Threshold Reached status is generated.

Bit 6	Bit 5	Transmit Threshold
0	0	0 Bytes
0	1	1 Bytes
1	0	2 Bytes
1	1	3 Bytes

Bits 4–3: Receive FIFO Threshold (Default = 11)—These two bits are used to select the receive FIFO threshold. When the number of bytes in the receive FIFO is greater than or equal to this value, the Receive FIFO Threshold Reached status is generated.

Bit 4	Bit 3	Receive Threshold
0	1	1 Byte
1	0	2 Bytes
1	1	3 Bytes
0	0	4 Bytes

Bit 2: Sync/Async Mode Select (Default = 0)—This bit determines the operating mode of the USART. If it is set to "1," the USART operates in synchronous mode where no start/stop bits are recognized and where the expected data rate is equal to the clock source programmed. If this bit is reset to "0," the USART operates in asynchronous mode and the clock source to the transmitter and receiver must be 16 times the expected data rate.

Bit 1: Transmit Clock Source (Default = 0)—The output of the internal baud rate generator is used as the clock source for the transmitter if it is set to "1"; otherwise, the RxCLK pin is used.

Bit 0: Receive Clock Source (Default = 0)—The output of the internal baud rate generator is used as the clock source for the receiver if this bit is set to "1"; otherwise, the RxCLK pin is used.

USART Status Register (28 HEX)

The USART Status Register reports status conditions that do not occur in an 8250 UART. This register also contains the Parity Error Character Available status bit. The default = 00010000.

Bits 4–1 are cleared when the corresponding condition no longer exists.

7	6	5	4	3	2	1	0
RECVR ENABLE	0	0	XMIT BUFFER AVAIL	RECV FIFO TRSHLD REACHD	SPCHL CHAR AVAIL	PARITY ERROR CHAR AVAIL	RECV FIFO TIMEOUT

Bit 7: Receiver Enable/Disable (Default = 0)—This bit is set to enable the USART receiver, and is cleared to disable the receiver.

Bits 6–5: Not used and must be reset to "0."

Bit 4: Transmit Buffer Available (Default = 1)—This bit is set to "1" whenever the FIFO Data Register is empty, and is cleared when the FIFO is full.

Bit 3: Receive FIFO Threshold (Default = 0)—This bit is set to "1" when the number of bytes in the receive FIFO is greater than or equal to the programmed receive FIFO threshold, and cleared when the number of bytes in the receive FIFO falls below the threshold value.

Bit 2: Special Character Available (Default = 0)—This bit is set to "1" when the special character reaches the output of the receive FIFO. It is cleared when the character is read from the FIFO.

Bit 1: Parity Error Character Available (Default = 0)—This bit is set to "1" when a character with the parity error reaches the output of the receive FIFO. It is cleared when the character is read from the FIFO.

Bit 0: Receive FIFO Timeout (Default = 0)—This bit is set to "1" when a receive FIFO timeout occurs. It is cleared when this register is read or when the receive FIFO becomes empty. The timeout occurs when the level in the receive FIFO is below the threshold and no characters are received in at least 2048 receiver clocks.

USART Special Character Bit-map Address Pointer Register (29 HEX)

This register is used to address the 128-bit special character bit map (Default = 0).

7	6	5	4	3	2	1	0
0	SPCHL CHAR MSB	SPCHL CHAR —	SPCHL CHAR —	SPCHL CHAR —	SPCHL CHAR —	SPCHL CHAR —	SPCHL CHAR LSB

Bit 7: Not used and must be reset to "0."

Bits 6–0: These bits represent the special character address in the bit map. A character is designated as a special character by first writing the address (which is the character itself) into bits 7–0 of the Special Character Bit-Map Address Pointer Register, and then by writing a "1" into bit 0 of the Special Character Bit-Map Command Register. A special character can be returned to normal status by writing a "0" into bit 0 of the Special Character Bit-Map Command Register (after the pointer is set).

USART Special Character Bit-map Command Register (2A HEX)

This register is used for setting and clearing the corresponding bit in the bit-map of the special character pointed to by the Special Character Bit-Map Pointer Register (Default = 0).

All bits in the bit-map are cleared on reset.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SET/ CLEAR BIT MAP

Bits 7–1: Not Used and must be reset to "0."

Bit 0: **Set/Clear Bit Map**—Writing a "0" or "1" to this bit clears or sets the Special character pointed to by the Special Character Pointer register. When this register is read bit 0 reflects the status of the special character pointed to by the Special Character Bit-MAP Pointer.

Note: When the receiver enable bit is set (bit 7 of USART Status Register), reading the Special Character Bit-Map Command Register returns all "1"s regardless of the actual state of the special character addressed. This is done to prevent simultaneous bit map accesses by the MPI and the internal logic.

A special character can be read or written to via the MPI only when the receiver enable bit (USART Status Register bit 7) is cleared.

Dual-Port Memory Controller (DPMC)

For multiprocessor applications, a common message area in RAM (i.e., a mailbox) is used for inter-processor communications.

When bit 0 of the Semaphore Register is set to "1," an interrupt (HINTOUT) is generated to the host processor indicating it has a message waiting in the mailbox. Bit 0 of the Semaphore Register is reset to "0" when the host processor acknowledges this interrupt by pulsing the HINTACK line.

When the host processor has completed placing a message in the mailbox for the local processor, it alerts the local processor by pulsing the HINTIN line. This results in setting bit 1 in the Semaphore Register which activates the interrupt line (LINTOUT) to the local processor. LINTOUT is de-activated when the local processor clears bit 1 of the Semaphore Register.

Table 4. DPMC REGISTERS

Offset (Hex)	Register Name	Size (Bytes)	Type
3F	Semaphore Register	1	Read/Write

Table 5. DPMC REGISTERS

Offset (Hex)	Register Name	Size (Bytes)	Type
3F	Semaphore Register	1	Read/Write

DPMC Semaphore Register

The Semaphore Register controls interrupt requests between the host processor and the local processor in a multiprocessor application. These interrupts coordinate processor-to-processor communication via shared memory. This register is cleared to "0"s by a hardware reset.

DPMC Semaphore Register (3F HEX)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	INTR TO LOCAL PROC	INTR TO HOST PROC

Bits 7–2: Not used and must be reset to "0."

Bit 1: Interrupt to Local Processor (Default = 0)— This bit is set to "1" when the HINTIN pin from the host processor goes active (i.e., is pulsed). Setting this bit to "1" causes the LINTOUT pin to go active High. This bit is cleared by the local processor by writing a "0" to it. LINTOUT goes inactive when this bit is cleared.

Bit 0: Interrupt to Host Processor (Default = 0)— This bit is set to "1" by the local processor to initiate communications with the host processor. Setting this bit causes the HINTOUT pin to go active High. The bit is cleared by the HINTACK pin (from the host) going High. This bit can be read by the local processor.

APPLICATIONS

Overview

Most ISDN applications of the IDPC may be grouped into two categories:

Terminal Adapter (TA)
PC or Integrated Voice/Data Workstation (IVDW)

The major difference is the number of processors in the system. In the terminal adaptor application, a single local processor (such as the 80188) controls all system functions and the USART serves as the RS-232 interface between the ISDN network and the terminal. The IDPC provides an external bus for attachment of an external processor such as the 80188, memory, "S" Interface transceiver hardware, and other ISDN support hardware.

In the PC or IVDW application, two processors (local and host) are present. The local processor (with associated circuitry and software) and the IDPC form the heart of the communication processor. The local processor on the interface card exchanges ISDN transmit/receive data with the host processor using shared memory and interprocessor interrupts (instead of using the USART as in the TA application).

Terminal Adapter (TA) Application

A typical terminal adapter application is shown in Figure 8. For the TA application, the processor attaches to the IDPC bus and runs specialized communication software to allow "dumb terminals" to attach to an ISDN network and make ISDN data calls. The low-level programming interface required for ISDN communications is available from AMD. The arbitration software required for multiple processor communications is not used in the TA application.

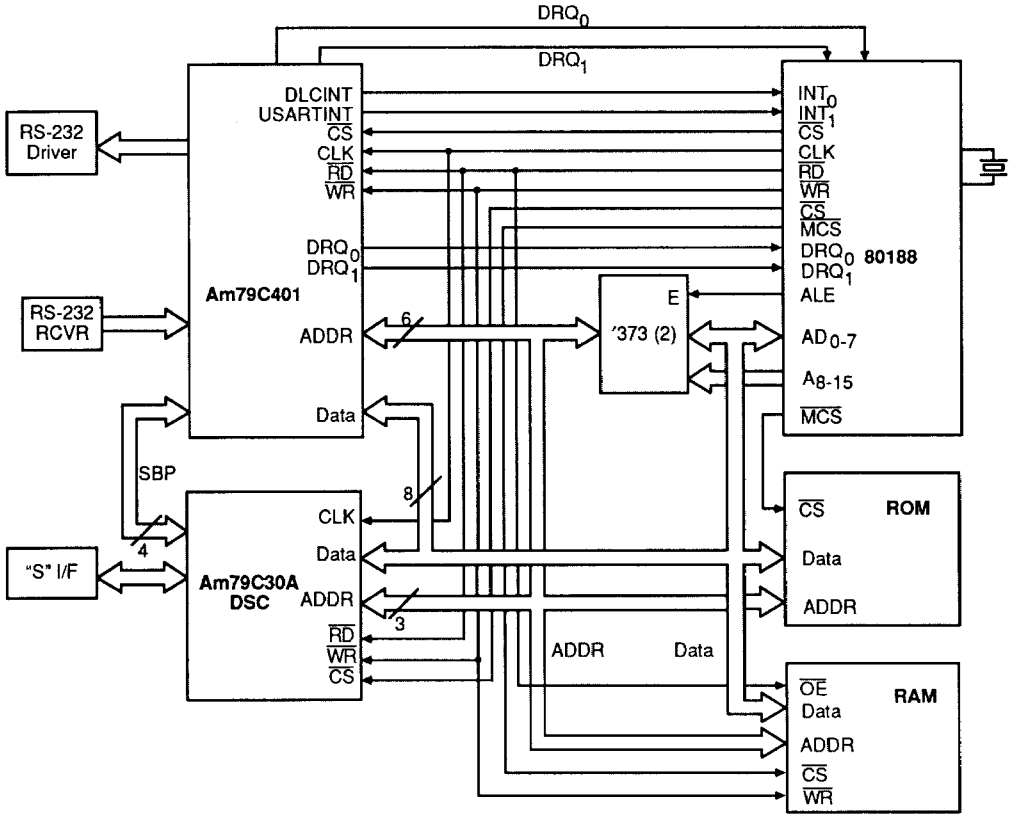


Figure 8. Typical TA Application (see 09360B-11)

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PC or Integrated Voice/Data Workstation (PC/IVDW) Application

Typically, the PC/IVDW application uses an interface card that installs in the PC or workstation. In this application, two processors (local and host) are present. The local processor (with associated circuitry and software) performs layers 2 and 3 of the communications protocol.

The local processor on the interface card exchanges ISDN transmit/receive data with the host processor using shared memory and inter-processor interrupts (instead of using the USART as in the TA application). The Dual-Port Memory Controller on the IDPC provides for effective memory sharing and handling of inter-processor interrupts.

The local processor can access any device on the IDPC external bus, whereas the host processor can only access the RAM on the IDPC external bus. Any contention between the local processor and the host processor is arbitrated by the Dual-Port Memory Controller on the IDPC. This arrangement provides for transparent access to shared memory by both the local and host processors, allowing inter-processor communications via memory-resident data buffers and mailboxes.

A combination of IDPC interrupt-related pins and IDPC register bits (which can be read and written only by the local processor) implement the interrupt mechanism. Once the local processor or host processor has written data to a buffer or a command to a mailbox, it uses the inter-processor interrupt mechanism to notify the other processor.

A sample PC/IVDW interface design is shown in Figure 9. For the PC application, the local processor attaches to the IDPC bus and runs specialized communication software (offered by AMD) to allow PCs and integrated voice/data workstations to attach to an ISDN network and make ISDN data calls.

The local processor runs a ROM-based layer 2 and 3 ISDN communication package (offered by AMD) to control ISDN operations. The local processor and the host processor in the PC or workstation communicate via IDPC interrupts and the shared RAM on the ISDN interface card.

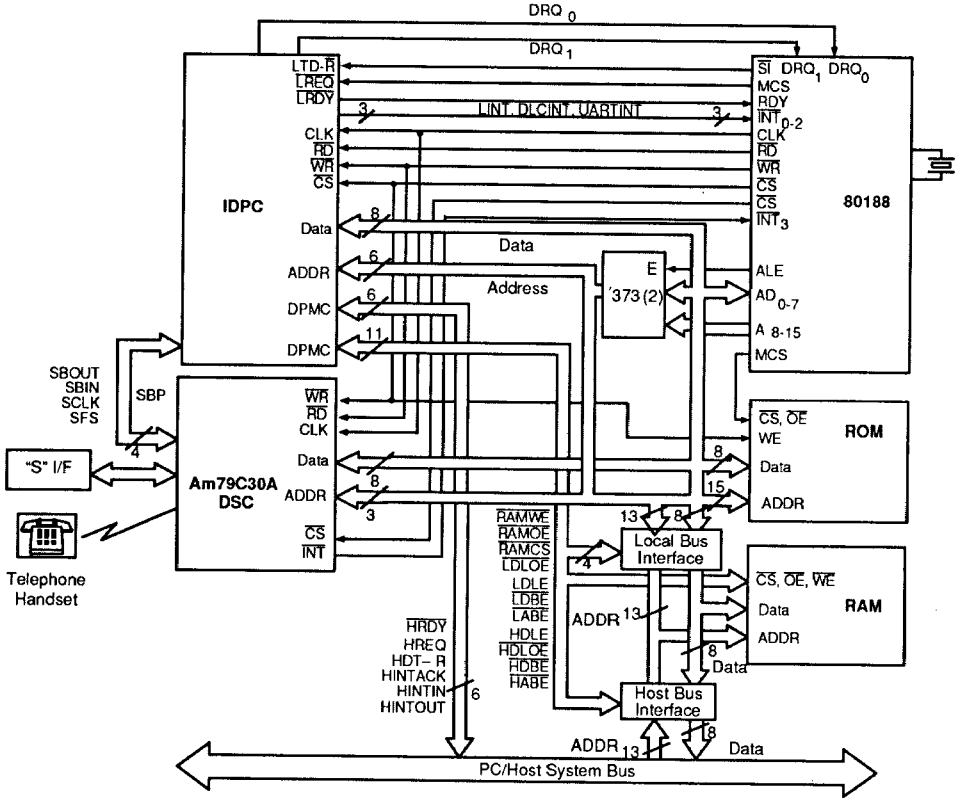

Figure 9. Typical PC Application

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The RAM is shared (transparent to the software) using the bus arbitration logic in the IDPC's Dual-Port Memory Controller.

PC-Based SNA Terminal Emulation

The following example shows the use of the IDPC in non-multiplexed mode to provide a PC-based intelligent SNA terminal emulator. The SNA processor executes all of the SNA emulation code, with the possible exception of the SNA presentation services layer. The IDPC supports SDLC at speeds up to 2.048 Mb/s.

Similar to the IVDW-PC application, the IDPC's Dual-Port-Memory Controller provides a shared RAM area to allow the local and host processors to exchange information (see Figure 10).

Communications Protocol Overview

Most communication networks used for data transfer employ a set of rules and techniques called bit-oriented protocols. These protocols allow for the transfer of data in packets. The most common bit-oriented protocols include: HDLC, SDLC, LAPB, LAPD, and DMI.

Bit-Synchronous Message Concepts

All communications over the ISDN (or any network using the bit-oriented protocols, such as X.25 or SNA) make use of message-framing formats in which specific bit patterns (Flags) rather than control characters are used to delineate message blocks.

Frame Format

Each packet, plus its opening and closing flags, is called a frame. Each frame conforms to the following format:

Flag	Address (1–N Bytes)	Control (1 or 2 Bytes)	Information (Optional)	Frame Check Sequence (FCS)	Flag

- Flags: Used to bracket the packet (leading "0" bit followed by six "1" bits and a trailing "0" bit).
- Address: Identifies the data sender or receiver. All addresses are an integer number of bytes in length. In general, an address can be 1, 2, or "n" bytes long.

The length of an "n"-byte-long address is determined by the value of the least significant bit in each byte of the address. This bit, called the Extended Address (EA) Bit, identifies the last byte of the address. All of the bytes on

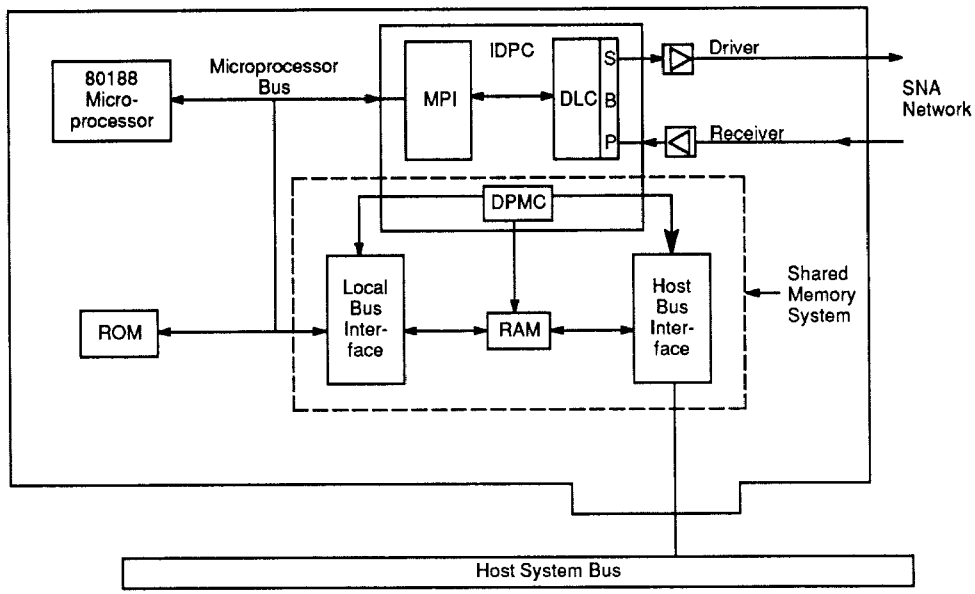


Figure 10. Typical SNA Application

an "n"-byte-long address will have the EA bit cleared to a 0 except for the last byte which has the EA bit set.

Note: The length of the address field affects the detection of a short frame (see description of short frame).

In some protocols, the second bit (bit 1) of the first byte of the address is used to indicate whether the frame is a command or a response. This bit, the Command/Response (C/R) bit, does not affect address recognition.

- Control Information: Used by higher levels of the protocol for data management (no action taken by the DLC in response to information in this field).
- Information Field (data): Variable length—up to 64K bytes long (minus address and control lengths). This field is optional and can be omitted for protocol control packets.
- Frame Check Sequence (FCS): The Frame Check Sequence is a 16-bit word that is produced by a Cyclic Redundancy Check (CRC) generator at the transmit side, reproduced by a similar circuit at the receive side, and checked against the transmitted code to determine if a bit has been dropped or picked up in error. The CRC is calculated using all bits after the Opening Flag up to the first bit of the Frame Check Sequence (excluding bits inserted for transparency).

Packet—A packet is defined as a frame minus the opening and closing flags.

Mark Idle—When frames are not being transmitted over the link, the link is idle. When the link is idle, the transmitter can be programmed to send an 'all 1s' pattern which is referred to as the mark idle condition (15 or more "1"s constitute mark idle).

Flag Idle—Prior to and between frames, the transmitter can be programmed to send back-to-back flags over the data link. This condition is referred to as flag idle.

In-Frame—The DLC receiver is said to be In-Frame when it is enabled and the first non-Flag, non-abort character is received after receiving at least one flag character.

The DLC transmitter is said to be In-Frame from the time it starts to send the first bit of the opening flag until the last bit of the closing flag has been transmitted (assuming the transmitter has not been commanded to send an abort character).

Abort Condition—The abort condition is an action that takes place in a response to the detection of an abort character while the DLC receiver is In-Frame. An abort causes the termination and discarding of the packet being received. Aborts are asynchronous events in that they can be transmitted and detected on bit boundaries.

Abort Character—The abort character is any pattern of at least seven contiguous "1"s. The DLC transmitter sends a pattern of seven "1"s and a "0" as an abort character.

Zero Insertion/Deletion (Data Transparency)—In order to prevent the data characters from appearing as flags, aborts, or mark idles, a technique called bit stuffing is employed. The contents of each packet is examined bit-by-bit (beginning with the first bit after the opening flag to the last bit of the Frame Check Sequence), and a "0" is inserted in the bit stream for any pattern containing five contiguous "1"s.

At the receiver side, "0"s are removed following the receipt of five contiguous "1"s.

Short Frame—Bit-Oriented Protocols (i.e., SDLC, HDLC) specify minimum lengths for valid packets (usually 4, 5, or 6 bytes). Any frame that is received with fewer than the minimum acceptable number of bytes is labeled as a short frame and is reported as an error.

Long Frame—In order to prevent buffer overrun, it is common practice to specify the maximum packet length for a data transfer (typically varies with each data call). Any received frame that exceeds the specified maximum frame length is terminated, identified as a long frame, and reported as an error.

Non-Integer Number of Bits Received—If a closing flag is detected and a non-integer number of bytes has been received (character preceding the closing flag contained fewer than 8 bits), a non-integer number of bytes condition is reported. This is not an error when bit-residue is allowed.

Order of Bit Transmission—All bytes are transmitted in ascending numerical order. Within a byte, the least significant bit (LSB) is transmitted first (except for the Frame Check Sequence which is transmitted MSB first).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −60 to +150° C
Ambient Temperature Under Bias .... −55 to +125° C
Voltage from Any Pin to Vss ... −0.25 to Vcc +0.25 V
Voltage from Vcc to Vss ..... −0.25 to +7 V
Lead Temperature (Soldering, 10 sec) ..... +300° C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70° C
Supply Voltage (V_{CC})	+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IH}	Input High Logic Level		2.0	Vcc	V
V_{IL}	Input Low Logic Level		−0.2	0.8	V
V_{OL}	Output Low Logic Level	I_{OL} = 2 mA		0.4	V
V_{OH}	Output High Logic Level	I_{OH} = −400 µA I_{OH} = −10 µA	2.4	 Vcc − 10	V V
I_{OL}	Output Leakage Current In	0 ≤ V_{OUT} ≤ Vcc		±10	µA
I_{IL}	Input Leakage Current	0 ≤ V_{IN} ≤ Vcc		±10	µA
Icc(S)	Vcc Supply Current (Standby)	Vcc + 5.25 V		800	µA
Icc(A)	Vcc Supply Current (Active)	T_A = 70° C		30	mA

Capacitance*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_I	Logic Input Capacitance			10	pF
C_O	Logic Output Capacitance			15	pF

*Parameters are not "tested."

SWITCHING CHARACTERISTICS over operating range unless otherwise noted

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
CLOCKS					
1	t_{CH}	CLK High Time	25		ns
2	t_{CL}	CLK Low Time	25		ns
3	t_{CLCL}	CLK Cycle Time	80	1000	ns
4	t_{CHCL}	CLK High-to-Low Transition		15	ns
5	t_{CLCH}	CLK Low-to-High Transition		15	ns
6	t_{SCH}	SCLK or SFS/XMITCLK High Time	50		ns
7	t_{SCL}	SCLK or SFS/XMITCLK Low Time	50		ns
8	t_{SCLCL}	SCLK or SFS/XMITCLK Cycle Time	488		ns
9	t_{SCHCL}	SCLK or SFS/XMITCLK High-to-Low Transition		1000	ns
10	t_{SCLCH}	SCLK or SFS/XMITCLK Low-to-High Transition		1000	ns
RESET					
11	t_{RES}	RST Active	10		Master CLK Cycles
12	t_{RESDL}	Delay after RST Low before cycle	8		Master CLK Cycles
13	t_{PD}	$\overline{PD}$ Active	10		Master CLK Cycles
14	t_{PDDL}	Delay after $\overline{PD}$ High before cycle	8		Master CLK Cycles
DMA REQUEST					
15	t_{DRQ0}	Last DMA Cycle to DRQ_0 Inactive		40	ns
16	t_{DRQ1}	Last DMA Cycle to DRQ_1 Inactive		40	ns
HOST MESSAGE AVAILABLE					
17	$t_{HIAVHIDL}$	HINTACK Active to HINTOUT Inactive		30	ns
USART ASYNCHRONOUS OPERATION					
18	t_T	Clock Low to Data Valid		50	ns

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
USART SYNCHRONOUS OPERATION					
19	t_{URDVL}	Data Setup to Clock High	15		ns
20	t_{URDH}	Data Hold from Clock High	15		ns
21	t_{UTCDV}	Clock Low to Data Valid		50	ns
SERIAL BUS PORT					
22	t_{SDC}	Data Setup to CLK High	15		ns
23	t_{SDHLD}	Data Hold from CLK High	15		ns
24	t_{CSDV}	Data Valid from CLK Low		50	ns
LOCAL CPU WRITE					
25	t_{AVAL}	Address Valid to $\overline{CS}$ Low	15		ns
26	t_{WA}	$\overline{CS}$ Valid to $\overline{WR}$ Active	15		ns
27	t_W	$\overline{WR}$ Active Width	130		ns
28	t_{DHLD}	Data Hold from $\overline{WR}$ High	15		ns
29	t_{WD}	$\overline{WR}$ Low to Data Valid		1	Master CLK Cycle
30	t_{WR}	$\overline{WR}$ Low to $\overline{RD}$ Low	4		Master CLK Cycle
30a	t_{DCE}	$\overline{WR}$ High to $\overline{RTS}$/$\overline{CTS}$ Transition		3	Master CLK Cycle
LOCAL CPU READ					
31	t_{AVAL}	Address Valid to $\overline{CS}$ Low	15		ns
32	t_{RA}	$\overline{CS}$ Valid to $\overline{RD}$ Active	15		ns
33	t_R	$\overline{RD}$ Active Width	120		ns
34	t_{RICSI}	$\overline{RD}$ High to $\overline{CS}$ High	0		ns
35	t_{RDHLD}	Data Hold from $\overline{RD}$ High	10		ns
36	t_{RDDLY}	$\overline{RD}$ Low to Valid Data	0	80	ns
37	t_{RDHDZ}	$\overline{RD}$ High to Data Bus Hi-Z		35	ns
37a	t_{INT}	$\overline{RD}$ High to INT High		80	ns

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
DUAL-PORT MEMORY CONTROLLER					
38	t_{LRQS}	$\overline{LREQ}$ Low Setup to CLK Low	10		ns
39	t_{TRS}	LDT-$\overline{R}$, HDT-$\overline{R}$ Setup to CLK High	10		ns
40	t_{TRH}	LDT-$\overline{R}$, HDT-$\overline{R}$ Hold from CLK High	15		ns
41	t_{WEADLY}	$\overline{RAMWE}$ Active Delay from CLK High		35	ns
42	t_{WEIDY}	$\overline{RAMWE}$ Inactive Delay from CLK Low		35	ns
43	t_{CSADLY}	$\overline{RAMCS}$ Active Delay from CLK Low		40	ns
44	t_{CSIDLY}	$\overline{RAMCS}$ Inactive Delay from CLK Low		40	ns
45	t_{DEADLY}	$\overline{RAMOE}$ Active Delay from CLK High		40	ns
46	t_{DEIDLY}	$\overline{RAMOE}$ Inactive Delay from CLK Low		40	ns
47	t_{BADLY}	$\overline{LDBE}$, $\overline{HDBE}$ Active Delay from CLK High		40	ns
48	t_{BIDLY}	$\overline{LDBE}$, $\overline{HDBE}$ Inactive Delay from CLK Low		40	ns
49	$t_{LDLEADLY}$	LDLE, $\overline{HDLE}$ Active Delay from CLK High		40	ns
50	$t_{LDLEIDLY}$	LDLE, $\overline{HDLE}$ Inactive Delay from CLK Low		40	ns
51	$t_{DLOADLY}$	$\overline{LDLOE}$, $\overline{HDLOE}$ Active Delay from CLK High		40	ns
52	$t_{LDLOIDLY}$	$\overline{LDLOE}$ Inactive Delay from LREQ/ High		20	ns
53	t_{ABADLY}	$\overline{LABE}$, $\overline{HABE}$ Active Delay from CLK High*		40	ns
54	t_{ABIDLY}	$\overline{LABE}$, $\overline{HABE}$ Inactive Delay from CLK Low		40	ns
55	t_{LRADLY}	$\overline{LRDY}$ Active Delay from $\overline{LREQ}$ Low**		35	ns
56	t_{LRIDLY}	$\overline{LRDY}$ Inactive Delay from CLK Low**		35	ns
57	t_{HRADLY}	$\overline{HRDY}$ Active Delay from HREQ High**		35	ns
58	t_{HRIDLY}	$\overline{HRDY}$ Inactive Delay from CLK Low		35	ns
59	$t_{HDLDIDLY}$	$\overline{HDLOE}$ Inactive Delay from HREQ Low		20	ns
60	t_{HREQSU}	HREQ Setup	10		ns

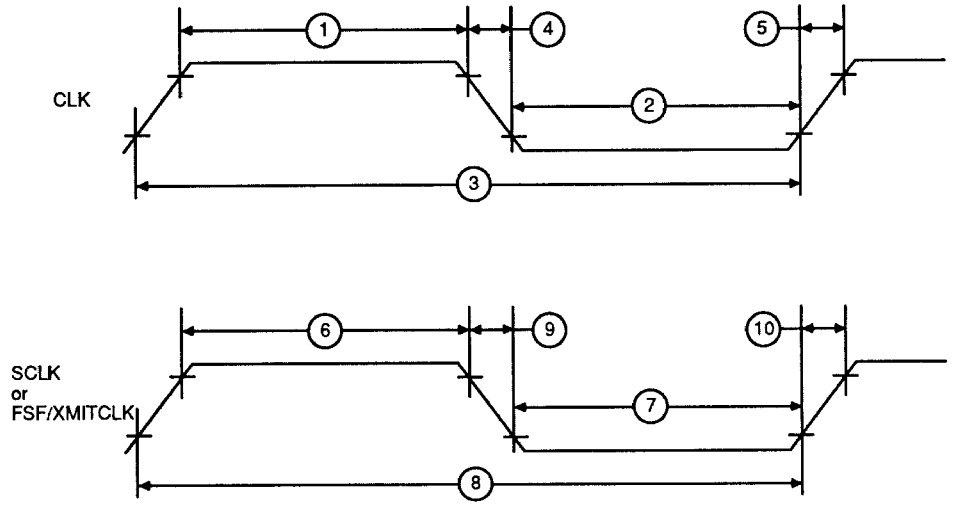
* CLK or $\overline{LABE}$/$\overline{HABE}$, whichever happens last
** With 1k pull-up resistor

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

Waveform	Inputs	Outputs
———	Must Be Steady	Will Be Steady
⟋⟋⟋	May Change From H to L	Will Be Changing From H to L
⟍⟍⟍	May Change From L to H	Will Be Changing From L to H
⟋⟍⟋⟍	Don't Care, Any Change Permitted	Changing, State Unknown

KS000010



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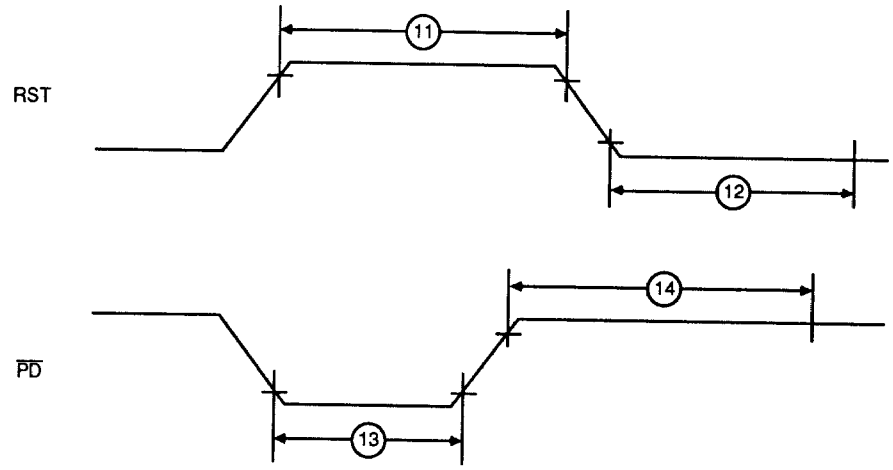
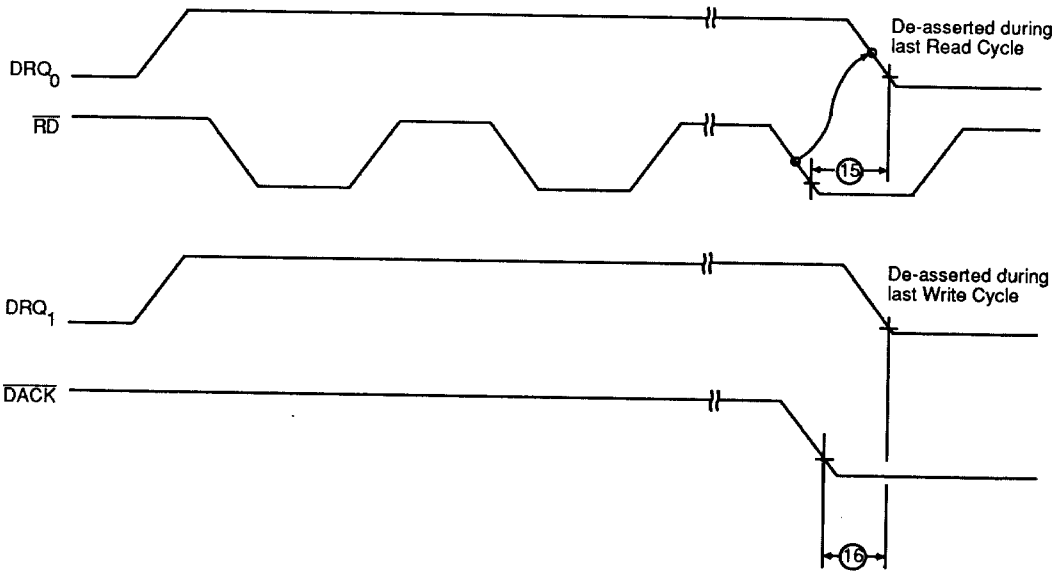
Clock Timing



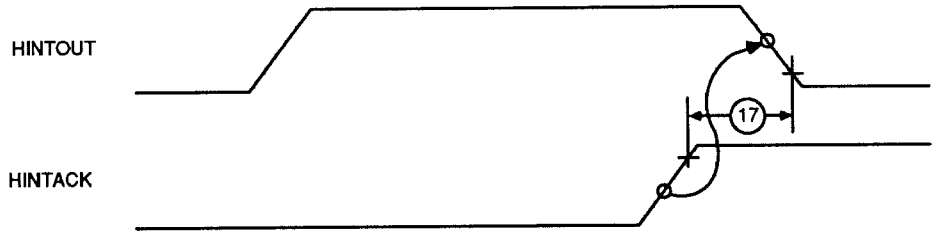
Reset Timing

09360B–15

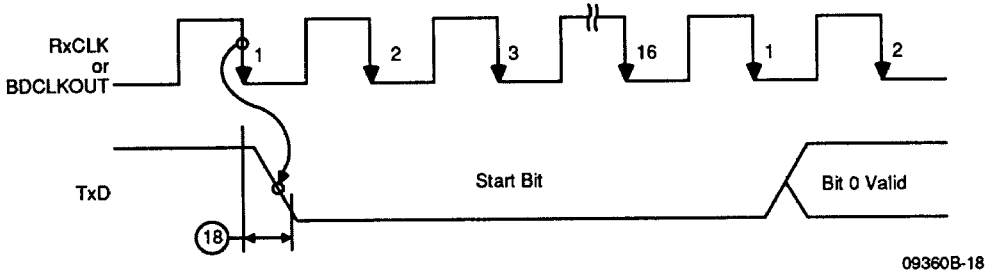


DMA Request Timing

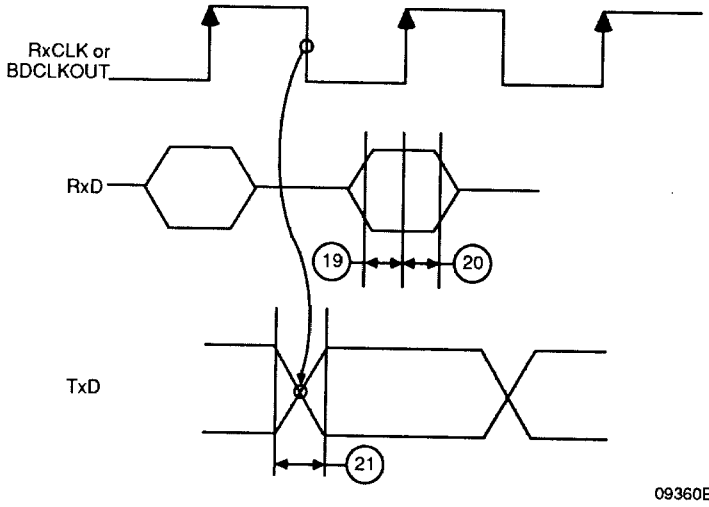
09360B–16



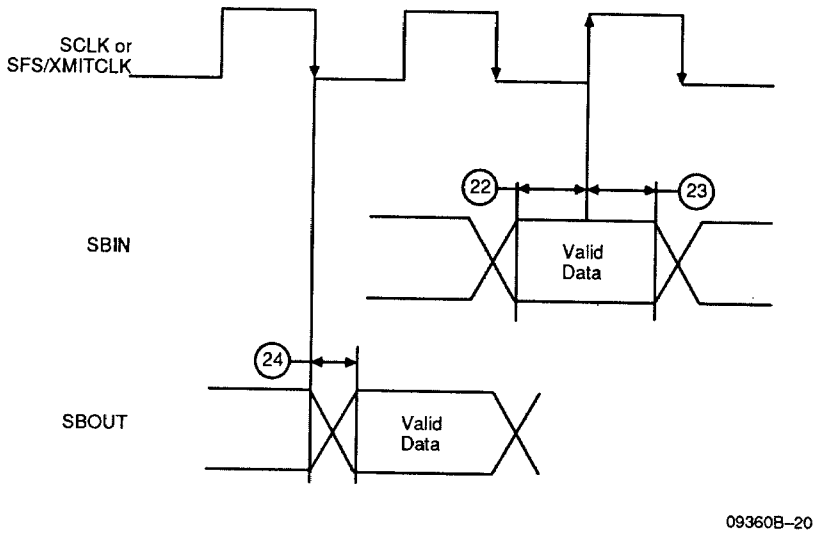
Host Message Available Timing



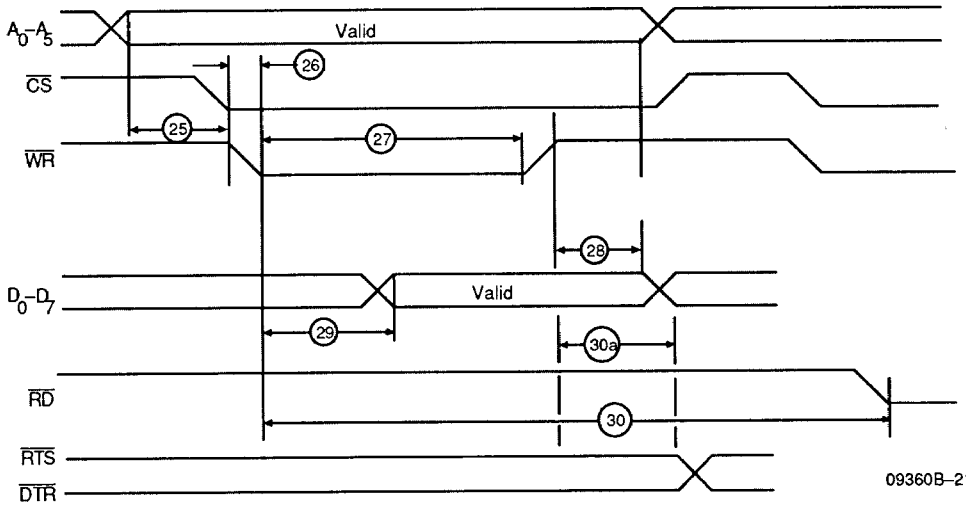
USART Asynchronous Operation



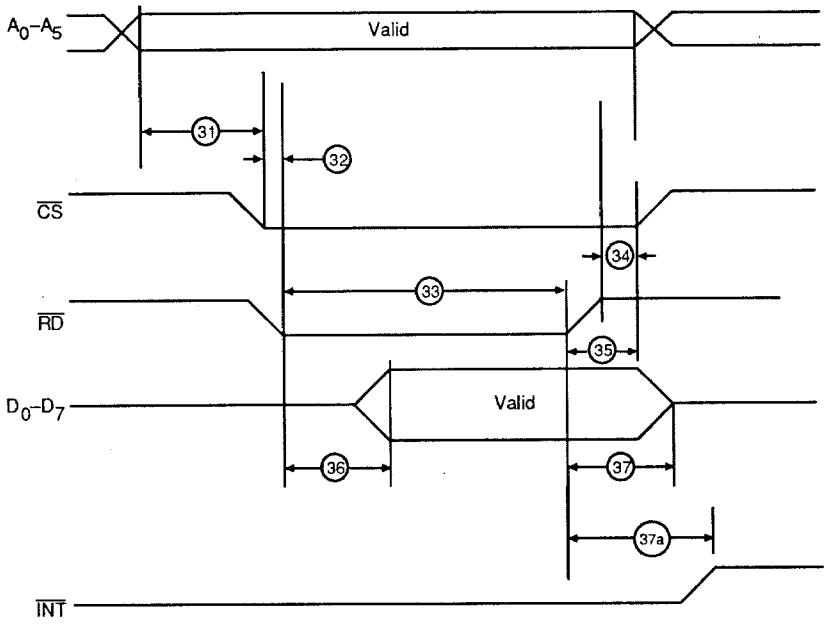
USART Synchronous Operation



Serial Bus Port Timing

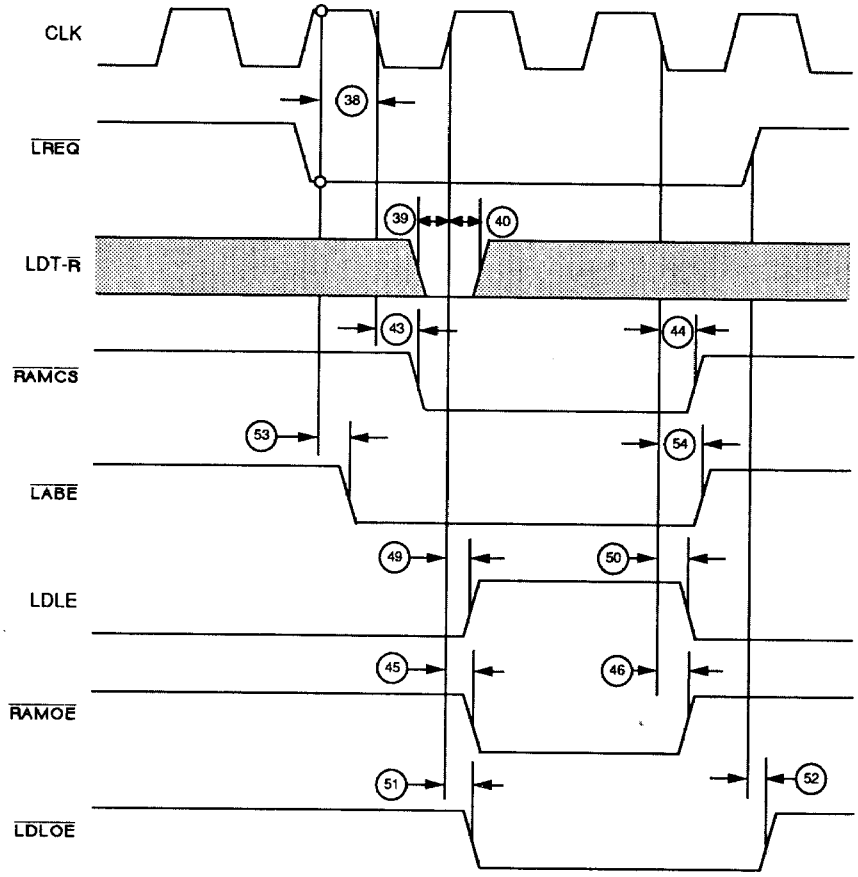


Local CPU Write Timing

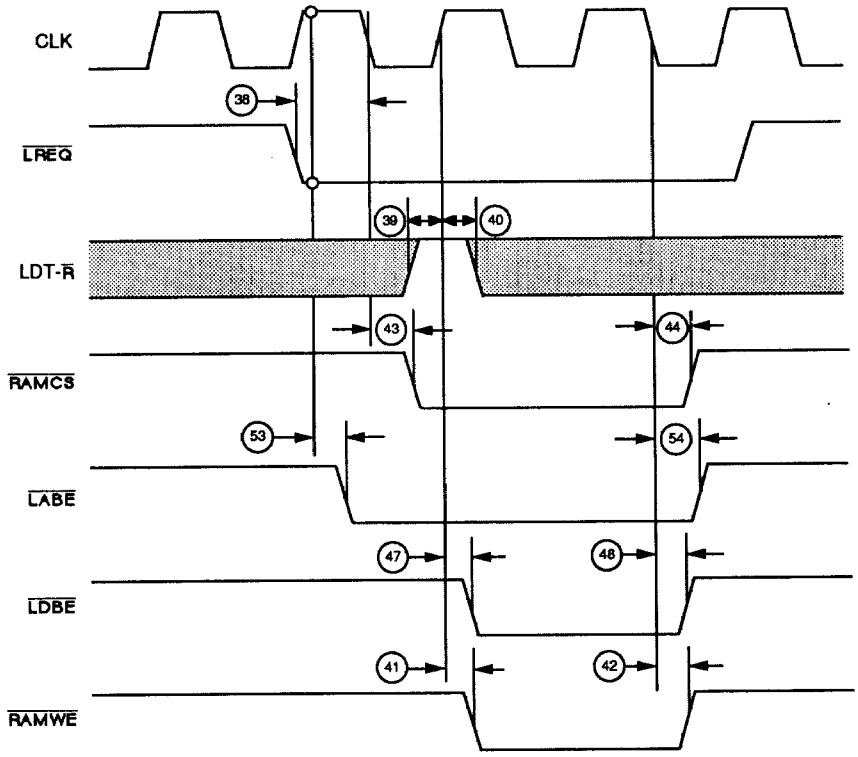


Local CPU Read Timing

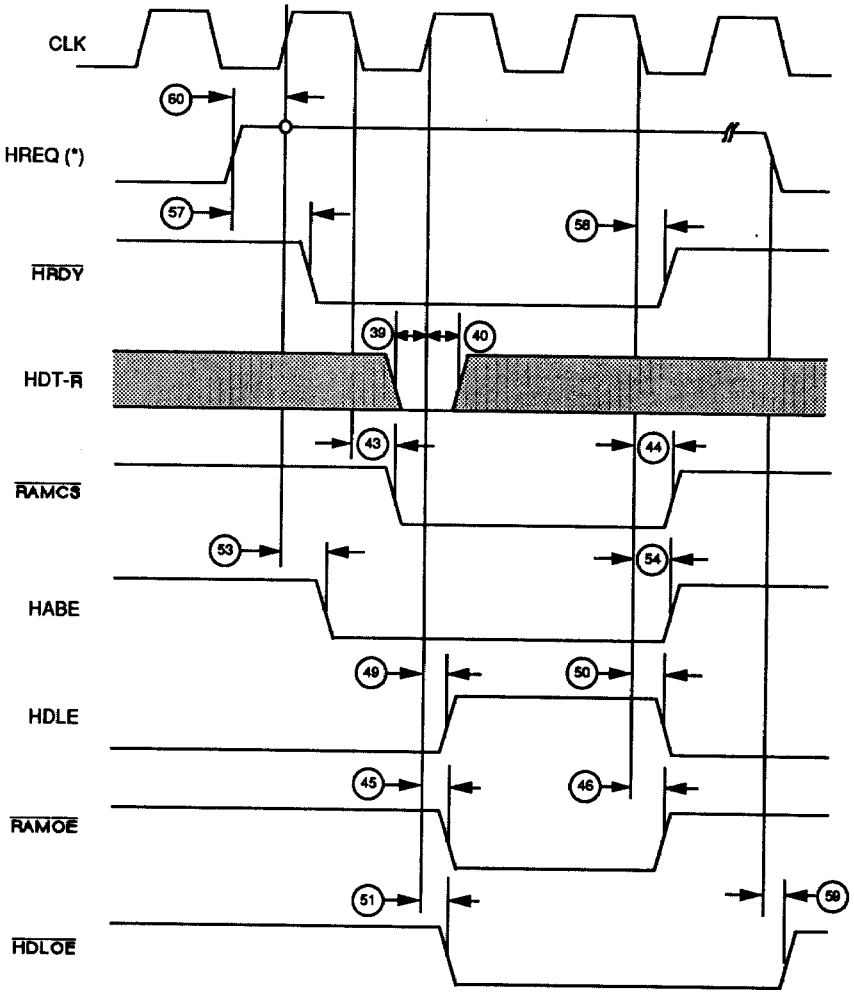
09360B–22



Dual-Port Memory Local Proc. Read Cycle (No contention)

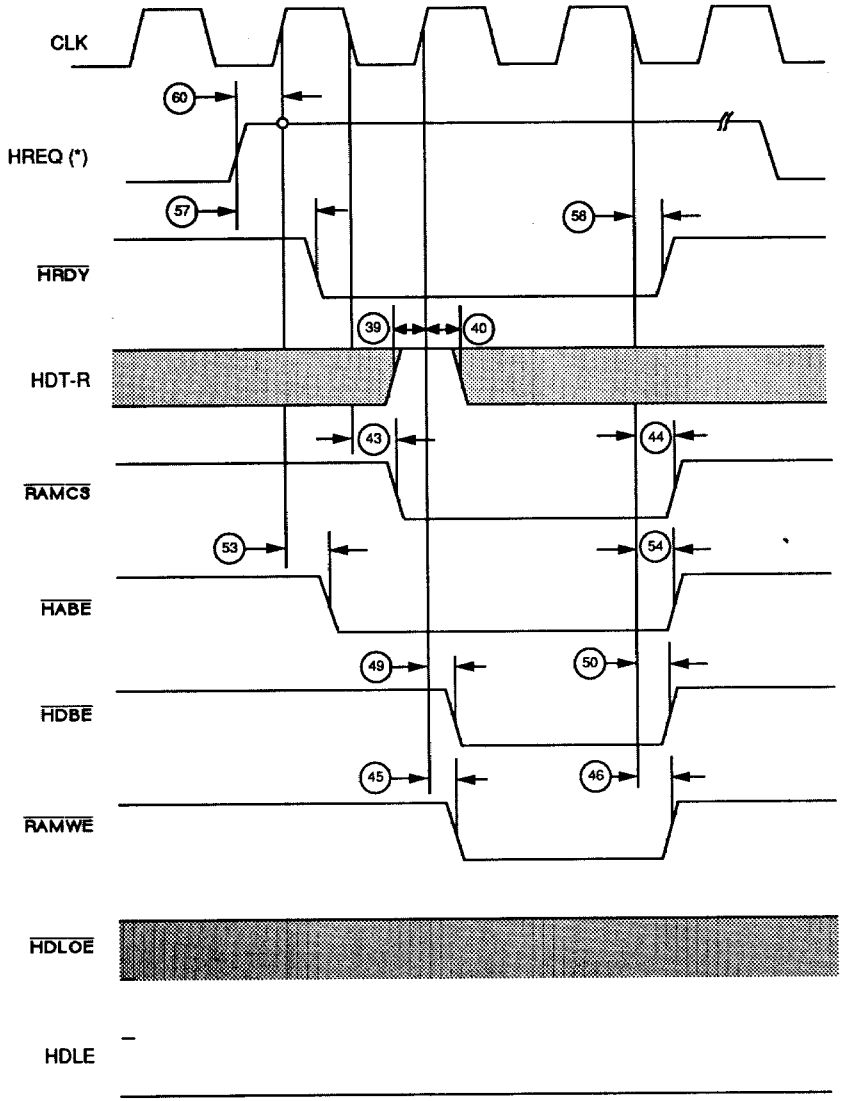


Dual-Port Memory Local Proc. Write Cycle (No contention)



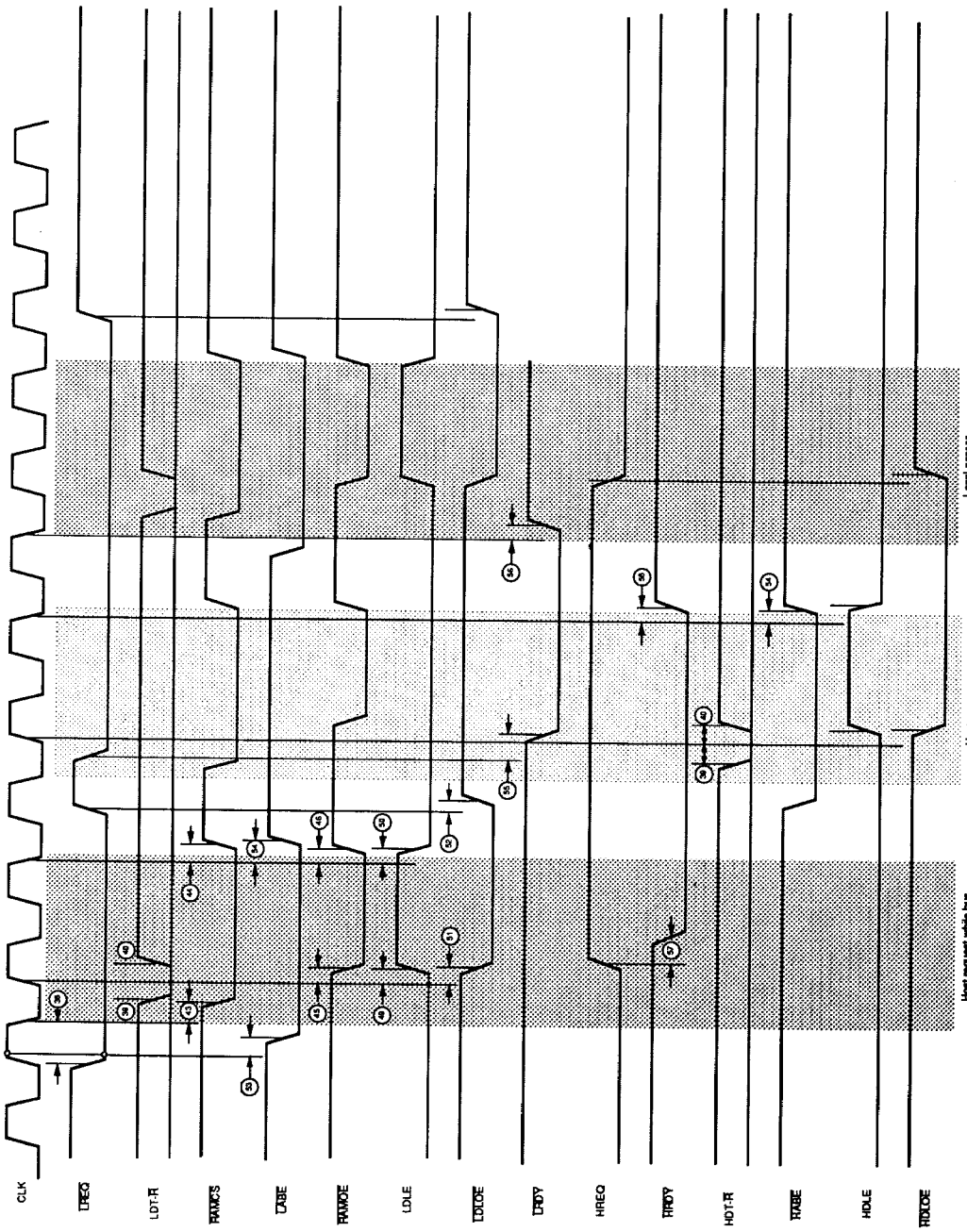
(*) HREQ is internally synchronized by the IDPC. If the setup time to the rising edge is not met, the memory cycle starts on the next rising edge of CLK.

Dual-Port Memory Host Proc. Read Cycle (No contention)



(*) HREQ is internally synchronized by the IDPC. If the setup time to the rising edge is not met, the memory cycle starts on the next rising edge of CLK.

Dual-Port Memory Host Proc. Write Cycle (No contention)

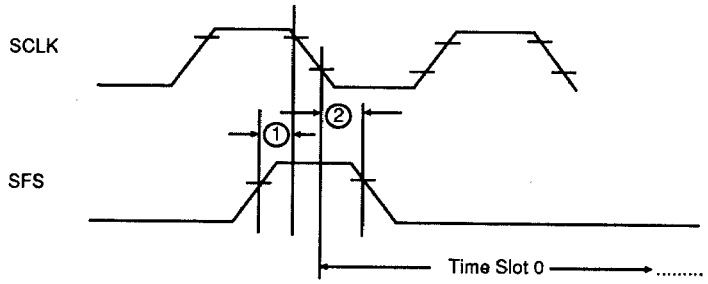


Dual-Port Memory Contention: Local Read—Host Read—Local Read

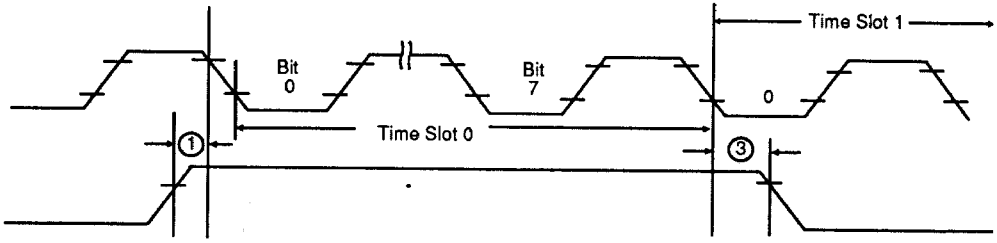
Multiplexed Mode

No.	Symbol	Description	Min.	Max.	Unit
1	t_{FSS}	Frame Sync set up time	50	t_{SCLCL} – 30	ns
2	t_{FSH1}	Frame Sync hold time	25	—	ns
3	t_{FSH2}	Frame Sync hold time	50	—	ns

*t_{SCHCL} = SCLK cycle time.



SFS Timing for Multiplexed Mode



SFS Timing for Extended Mode

PHYSICAL DIMENSIONS
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