PRELIMINARY

Intel™ 82430FX, HX, VX PCIset Pipelined L2 Cache Modules

Features

- **Secondary cache modules that are ideal for the Intel 82430FX, 82430HX, and 82430VX chip sets**
- **Complies with Intel COAST 3.0 cache module specifications**
- **High-performance cache modules based on synchronous pipelined 32Kx32 data BSRAM**
- **All modules contain series damping resistors on the data lines to improve system signal quality**
- **Operates at 50, 60, and 66 MHz**
- **160-position connector is compatible with all four Keying Options defined in COAST 3.0.**
- **3.3V compatible inputs/data outputs**

Functional Description

The cache modules are designed for Intel P54C/P55C systems with the 82430FX, 82430HX, and 82430VX chip sets.

The CYM74P430B/431B/434B/435B modules are based on industry standard 32Kx32 synchronous pipelined BSRAM.

The CYM74P430B (256-Kbyte) and CYM74P431B (512-Kbyte) are high performance modules compatible with all three chipsets.
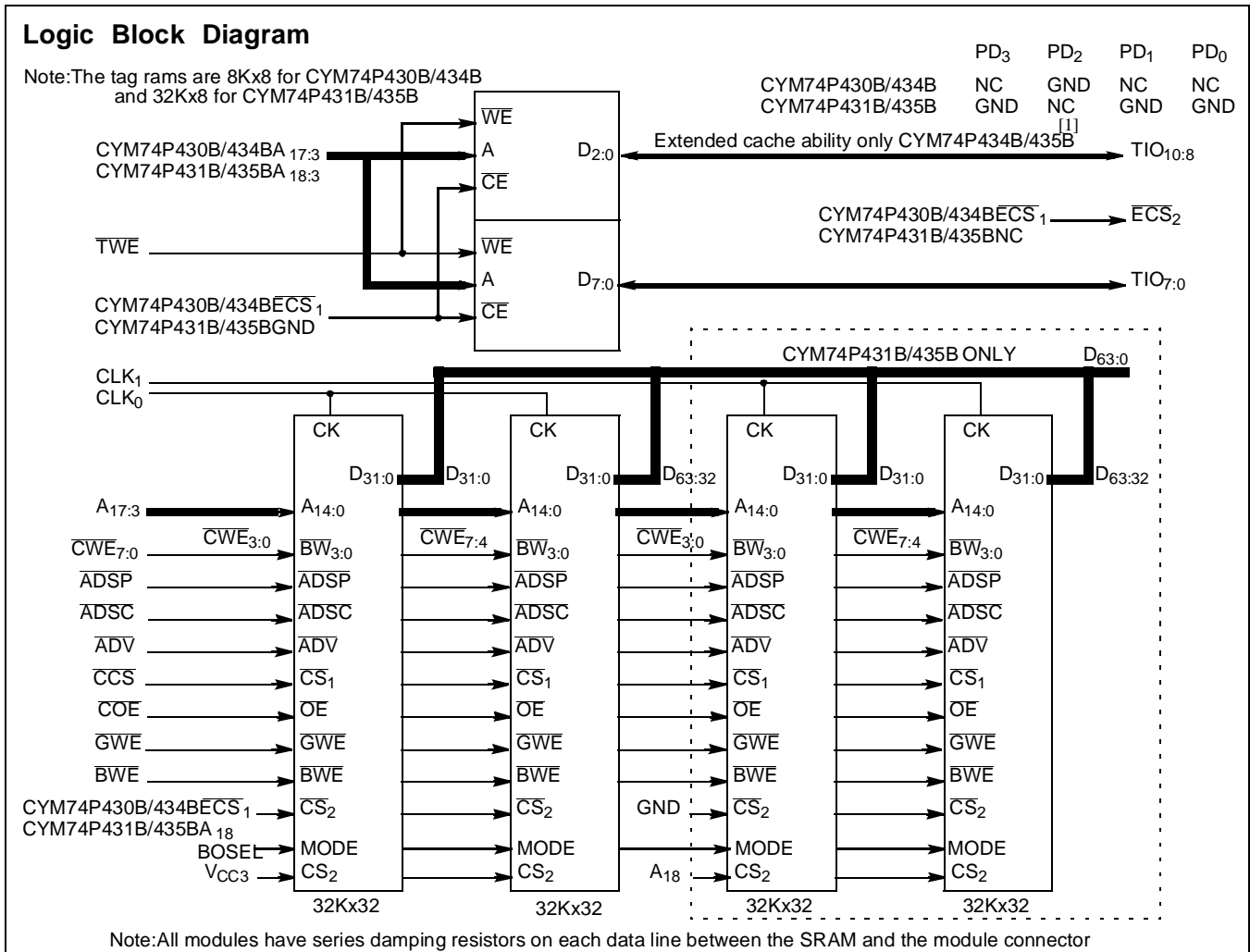
The CYM74P434B (256-Kbyte) and CYM74P435B (512-Kbyte) are high performance modules with extended cacheability for systems based on the 82430HX chipset.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity. All modules have series damping resistors on the data lines.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 30 micro-inches of gold.

Logic Block Diagram

Note: All modules have series damping resistors on each data line between the SRAM and the module connector

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Selection Guide

Part Number	Synchronous Pipelined Cache Modules					
	74P430B−50	74P430B−60	74P430B−66	74P431B−50	74P431B−60	74P431B−66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data SRAM t_{CO} w/0 pF loading	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag SRAM t_{AA}	20 ns	15 ns	15 ns	20 ns	15 ns	15 ns

Part Number	Synchronous Pipelined Cache Modules with Extended Cacheability					
	74P434B−50	74P434B−60	74P434B−66	74P435B−50	74P435B−60	74P435B−66
Cache Size	256 KB			512 KB		
System Clock (MHz)	50	60	66	50	60	66
Data SRAM t_{CO} w/0 pF loading	13.5 ns	10 ns	8.5 ns	13.5 ns	10 ns	8.5 ns
Tag SRAM t_{AA}	20 ns	15 ns	15 ns	20 ns	15 ns	15 ns

Pin Configuration

Dual Read–Out SIMM (DIMM)
Top View

Left pin	#	#	Right pin
GND	81	1	GND
TIO_1	82	2	TIO_0
TIO_7	83	3	TIO_2
TIO_5	84	4	TIO_6
TIO_3	85	5	TIO_4
[1] (CYM74P434B,CYM74P435B)TIO_9	86	6	TIO_8 (CYM74P434B, CYM74P435B) [1]
V_{CC5}	87	7	V_{CC3}
[1] (CYM74P434B,CYM74P435B)TIO_{10}	88	8	$\overline{TWE}$
$\overline{ADV}$	89	9	$\overline{ADSC}$
GND	90	10	GND
$\overline{COE}$	91	11	$\overline{CWE_4}$
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$
$\underline{V_{CC5}}$	95	15	$\underline{V_{CC3}}$
$\overline{CWE_3}$	96	16	$\overline{CCS}$
NC	97	17	$\overline{GWE}$
NC	98	18	$\overline{BWE}$
GND	99	19	GND
RSVD	100	20	A_3
A_4	101	21	A_7
A_6	102	22	A_5
A_8	103	23	A_{11}
A_{10}	104	24	A_{16}
V_{CC5}	105	25	V_{CC3}
A_{17}	106	26	A_{18} (CYM74P431B,CYM74P435B)
GND	107	27	GND
A_9	108	28	A_{12}
A_{14}	109	29	A_{13}
A_{15}	110	30	$\overline{ADSP}$
RSVD	111	31	$\overline{ECS_1}$
PD_0	112	32	$\overline{ECS_2}$
PD_2	113	33	PD_1
[2] BOSEL	114	34	PD_3
GND	115	35	GND
CLK_0	116	36	CLK_1 (CYM74P431B,CYM74P435B)
GND	117	37	GND
D_{63}	118	38	D_{62}
V_{CC5}	119	39	V_{CC3}
D_{61}	120	40	D_{60}
D_{59}	121	41	D_{58}
D_{57}	122	42	D_{56}
GND	123	43	GND
D_{55}	124	44	D_{54}
D_{53}	125	45	D_{52}
D_{51}	126	46	D_{50}
D_{49}	127	47	D_{48}
GND	128	48	GND
D_{47}	129	49	D_{46}
D_{45}	130	50	D_{44}
D_{43}	131	51	D_{42}
V_{CC5}	132	52	V_{CC3}
D_{41}	133	53	D_{40}
D_{39}	134	54	D_{38}
D_{37}	135	55	D_{36}
GND	136	56	GND
D_{35}	137	57	D_{34}
D_{33}	138	58	D_{32}
D_{31}	139	59	D_{30}
V_{CC}	140	60	V_{CC3}
D_{29}	141	61	D_{28}
D_{27}	142	62	D_{26}
D_{25}	143	63	D_{24}
GND	144	64	GND
D_{23}	145	65	D_{22}
D_{21}	146	66	D_{20}
D_{19}	147	67	D_{18}
V_{CC5}	148	68	V_{CC3}
D_{17}	149	69	D_{16}
D_{15}	150	70	D_{14}
D_{13}	151	71	D_{12}
GND	152	72	GND
D_{11}	153	73	D_{10}
D_9	154	74	D_8
D_7	155	75	D_6
V_{CC5}	156	76	V_{CC3}
D_5	157	77	D_4
D_3	158	78	D_2
D_1	159	79	D_0
GND	160	80	GND

Notes:
1. For the CYM74P434B and CYM74P435B TIO_8 and TIO_9 are pulled up on the module through a 8.2KΩ resistor. TIO_{10} is pulled to ground on the module through an 8.2KΩ resisitor.
2. BOSEL is pulled up through a 4.7KΩ resistor on the module for backward compatible operation in systems not supporting BOSEL operation.

3

Pin Definitions

Common Signals	Description
V_{CC5}	5V Supply
V_{CC3}	3.3V Supply
GND	Ground
$A_{18:3}$	Addresses from processor
$\overline{COE}$	Output Enable
$\overline{CWE}_{7:0}$	Byte Write Selects
$\overline{BWE}$	Byte Write Enable
$\overline{GWE}$	Global Write Enable
$D_{63:0}$	Data lines from processor
$TIO_{7:0}$	Tag data bits
$TIO_{10:8}$	Extended cacheability tag data bits for CYM74P434B or CYM74P435B
$\overline{TWE}$	Tag Write Enable signal
$\overline{ADSP}$	Processor Address Strobe
$\overline{ADSC}$	Cache Controller Address Strobe
$\overline{ADV}$	Burst Address Advance
$\overline{CCS}$	Cache Chip Select
$\overline{ECS}_1$	256-Kbyte Expansion Chip Select input pin (CYM74P430B or CYM74P434B)
$\overline{ECS}_2$	256-Kbyte Expansion Chip Select output pin (CYM74P430B or CYM74P434B)
$CLK_{1:0}$	Clock signals, CLK_1 is not used on CYM74P430B or CYM74P434B
$PD_{3:0}$	Presence Detect output pins
BOSEL	Burst Order Select. When LOW, linear burst sequence is selected. When HIGH, inter-leaved burst sequence is selected. If not driven (a no-connect on the motherboard) a pull-up resistor on the module will default to interleaved burst sequence.
RSVD	Reserved.
NC	Signal not connected on module.

Presence Detect Pins

	PD_3	PD_2	PD_1	PD_0
CYM74P430B, CYM74P434B	NC	GND	NC	NC
CYM74P431B, CYM74P435B	GND	NC	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −55°C to +125°C

Ambient Temperature
with Power Applied .... −0°C to +70°C

3.3V Supply Voltage to Ground Potential....... −0.5V to +4.6V

5V Supply Voltage to Ground Potential.......... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...−0.5V to +4.6V

DC Input Voltage ....−0.5V to +4.6V

Output Current into Outputs (LOW)............................ 20 mA

Operating Range

Range	Ambient Temperature	V_{CC5}	V_{CC3}
Commercial	0° to 70°C	5V ± 5%	3.3V +10%−5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0	$V_{CC3} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. $I_{OH} = -4$ mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. $I_{OL} = 8$ mA		0.4	V
I_{CC} (74P430B)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}		750	mA
I_{CC} (74P431B)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}		1400	mA
I_{CC} (74P434B)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}		900	mA
I_{CC} (74P435B)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}		1550	mA

Ordering Information

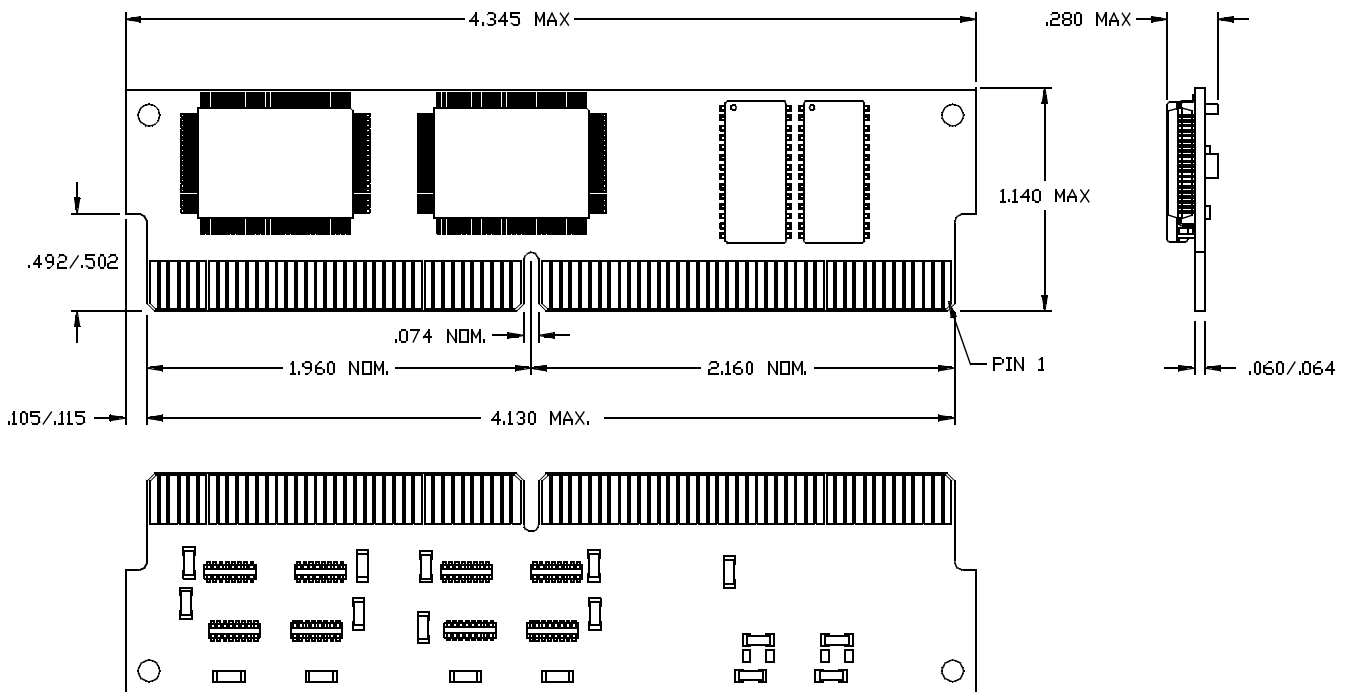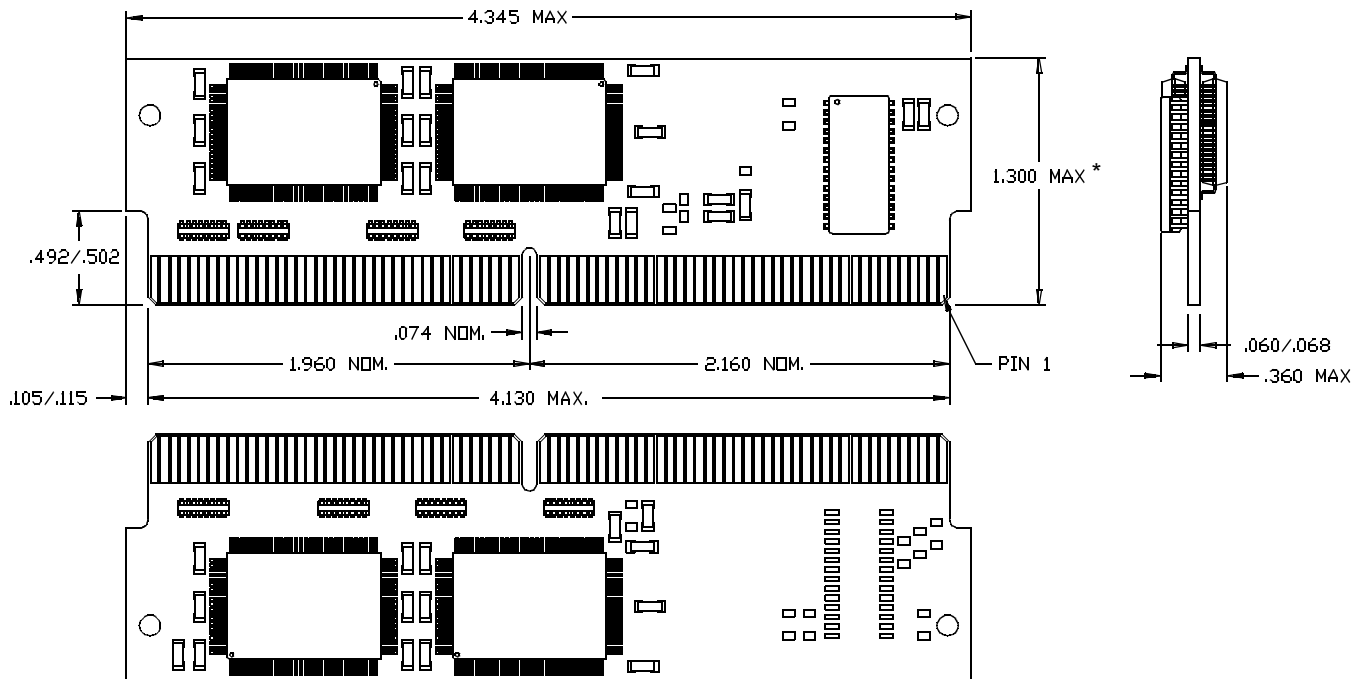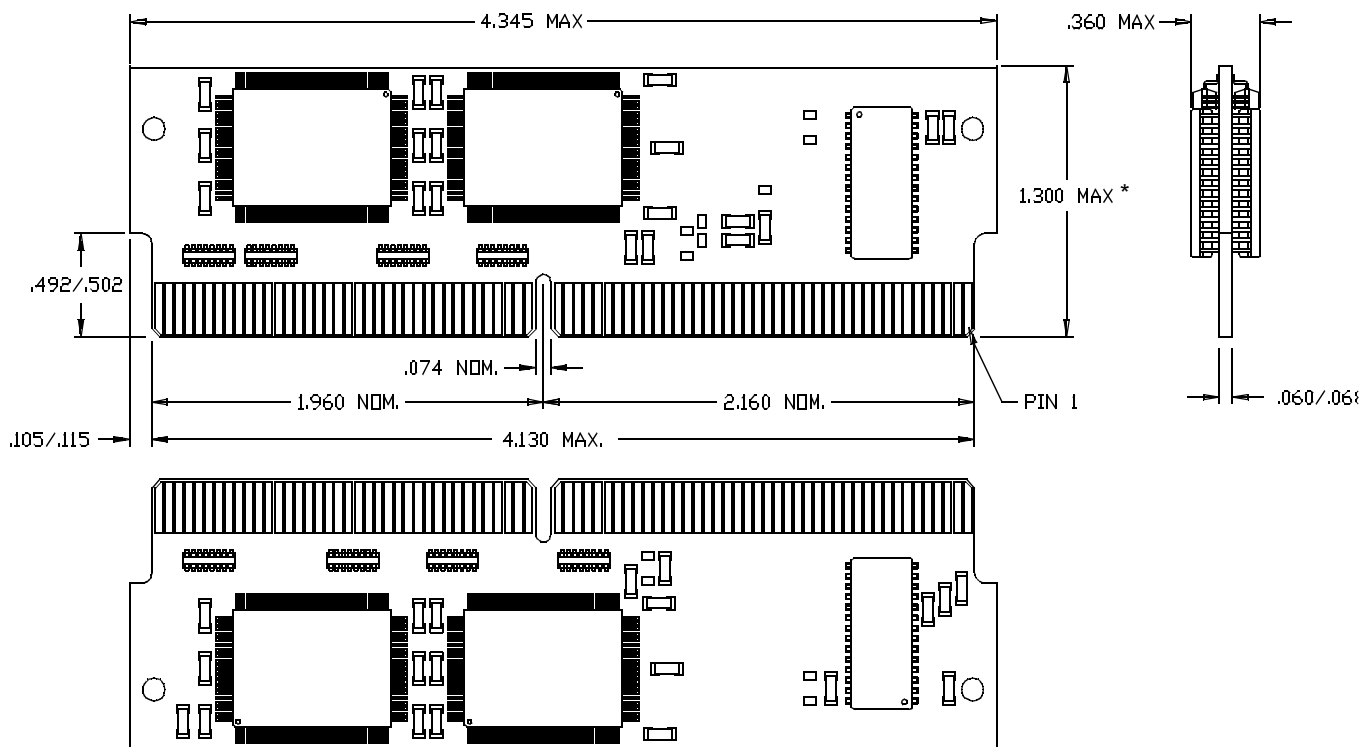| Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM74P430BPM-50C	PM38	160-Pin Dual-Readout SIMM	256 KB	Commercial
	CYM74P431BPM-50C	PM40		512 KB	
	CYM74P434BPM-50C	PM39		256 KB extended cache	
	CYM74P435BPM-50C	PM41		512 KB extended cache	
60	CYM74P430BPM-60C	PM38	160-Pin Dual-Readout SIMM	256 KB	Commercial
	CYM74P431BPM-60C	PM40		512 KB	
	CYM74P434BPM-60C	PM39		256 KB extended cache	
	CYM74P435BPM-60C	PM41		512 KB extended cache	
66	CYM74P430BPM-66C	PM38	160-Pin Dual-Readout SIMM	256 KB	Commercial
	CYM74P431BPM-66C	PM40		512 KB	
	CYM74P434BPM-66C	PM39		256 KB extended cache	
	CYM74P435BPM-66C	PM41		512 KB extended cache	

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Package Diagrams

CYM74P430BPM in 160-pin Dual Readout SIMM PM38

CYM74P434BPM in 160-pin Dual Readout SIMM PM39

Package Diagrams (continued)

CYM74P431BPM in 160-pin Dual Readout SIMM PM40

CYM74P435BPM in 160-pin Dual Readout SIMM PM41

* The 512-KByte modules CYM74P431B and CYM74P435B have a 1.300 max. height vs. 1.140 for the 256-KB modules.