

DATA SHEET

C106D Thyristors logic level

Product specification

July 2001

Thyristors logic level

C106D

GENERAL DESCRIPTION

Passivated, sensitive gate thyristor in a plastic envelope, intended for use in general purpose switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

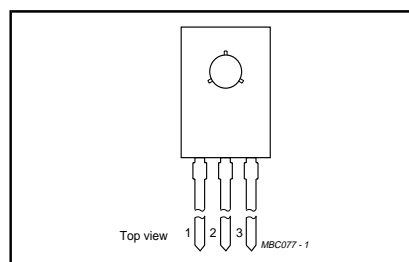
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DRM} V_{RRM}	Repetitive peak off-state voltages	400	V
$I_{T(AV)}$	Average on-state current	2.5	A
$I_{T(RMS)}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	38	A

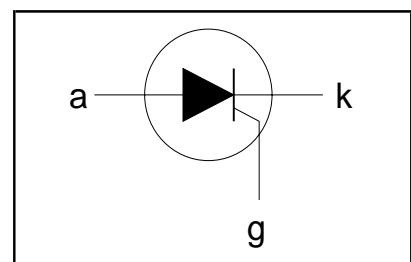
PINNING - SOT32

PIN	DESCRIPTION
1	cathode
2	anode
3	gate

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages		-	400 ¹	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 113\text{ °C}$	-	2.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	4	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge	-	35	A
		$t = 10\text{ ms}$	-	38	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	6.1	A ² s
dl_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 10\text{ A}; I_G = 50\text{ mA}; dl_G/dt = 50\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	°C
T_j	Operating junction temperature		-	125 ²	°C

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

² Note: Operation above 110°C may require the use of a gate to cathode resistor of 1k Ω or less.

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{thj-mb}	Thermal resistance junction to mounting base	in free air	-	-	2.5	K/W
R_{thj-a}	Thermal resistance junction to ambient		-	-	95	K/W

STATIC CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise stated

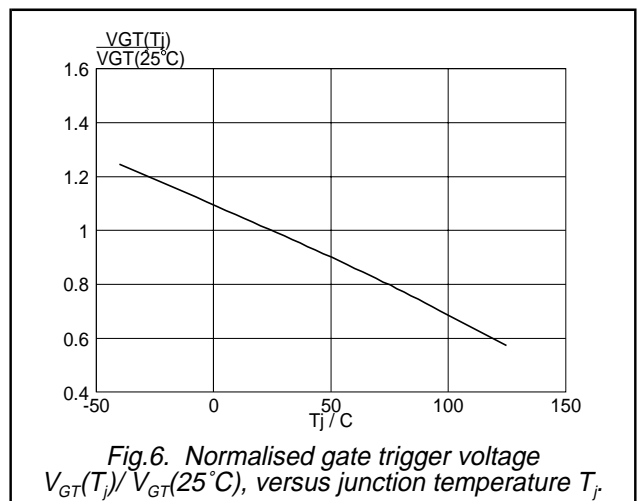
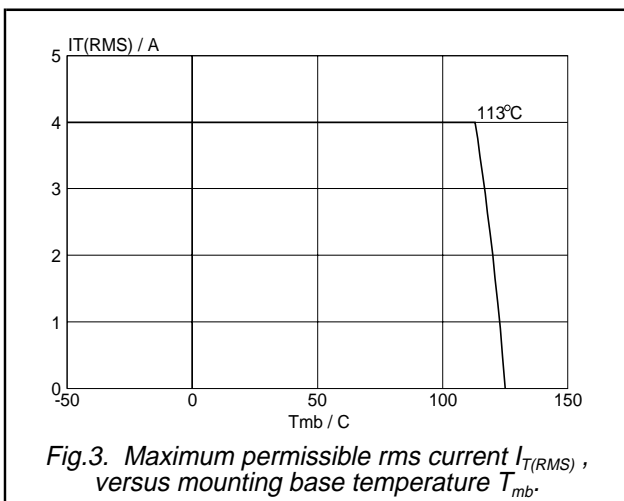
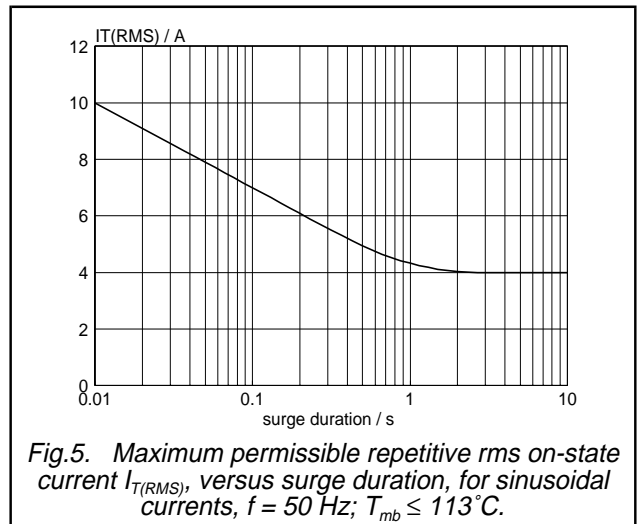
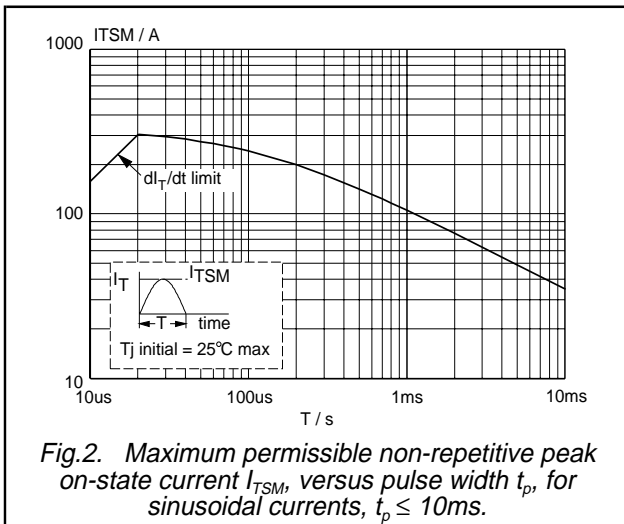
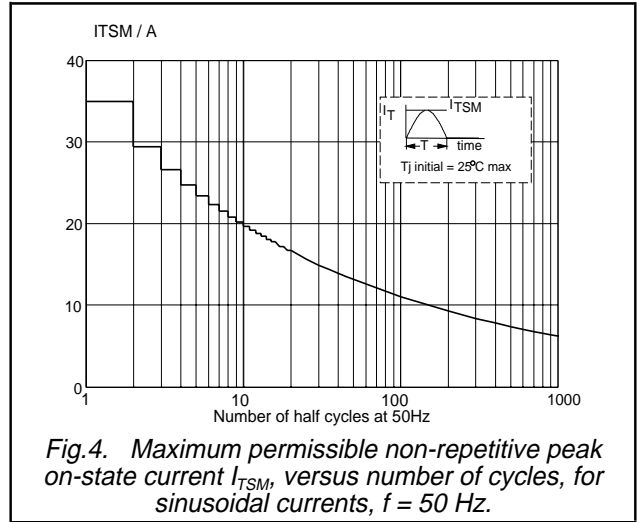
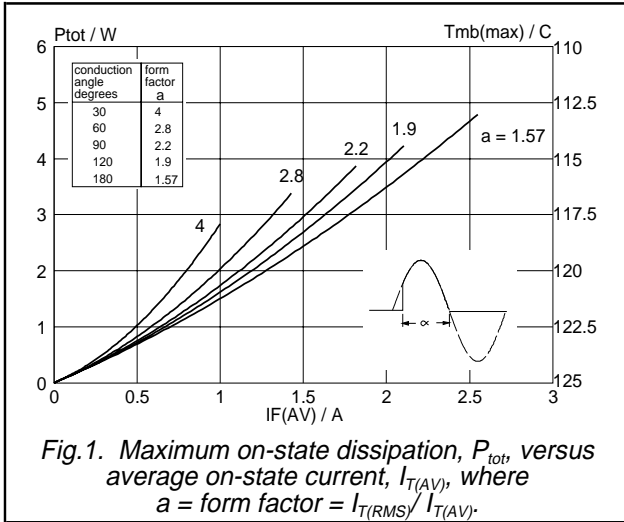
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$	-	15	200	μA
I_L	Latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$	-	0.17	10	mA
I_H	Holding current	$V_D = 12\text{ V}$; $I_{GT} = 0.1\text{ A}$	-	0.10	6	mA
V_T	On-state voltage	$I_T = 5\text{ A}$	-	1.23	1.8	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$	-	0.4	1.5	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}$; $I_T = 0.1\text{ A}$; $T_j = 110\text{ °C}$	0.1	0.2	-	V
		$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125\text{ °C}$; exponential waveform; $R_{GK} = 100\ \Omega$	-	50	-	V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM} = 10\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 5\text{ mA}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$	-	2	-	μs
t_q	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}$; $T_j = 125\text{ °C}$; $I_{TM} = 8\text{ A}$; $V_R = 10\text{ V}$; $dI_{TM}/dt = 10\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$	-	100	-	μs

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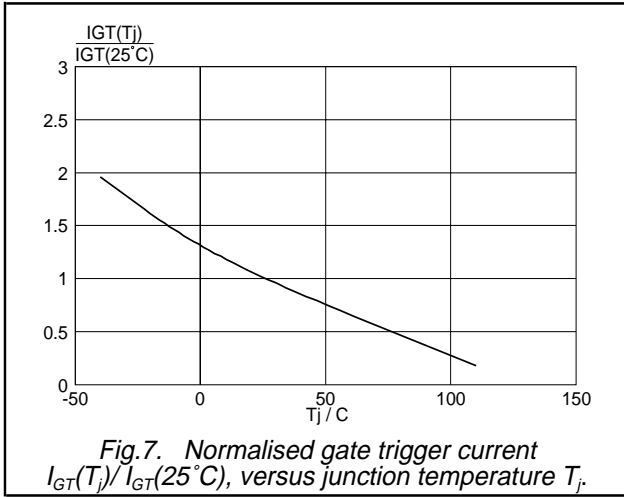


Fig.7. Normalised gate trigger current $I_{GT}(T_j) / I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

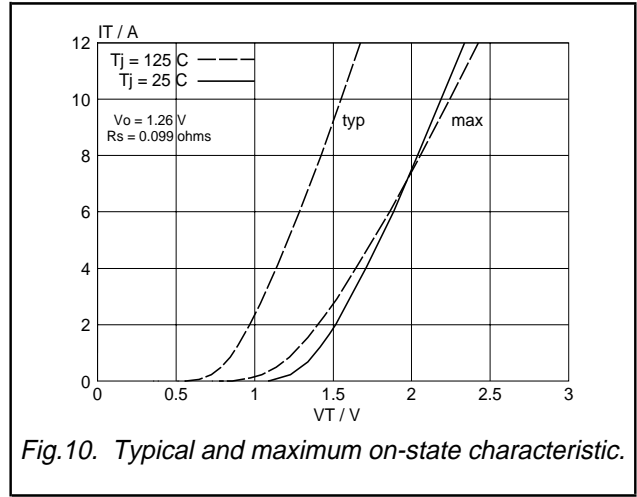


Fig.10. Typical and maximum on-state characteristic.

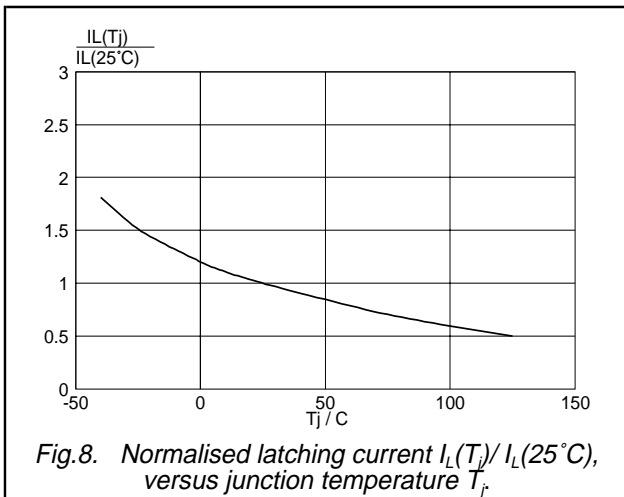


Fig.8. Normalised latching current $I_L(T_j) / I_L(25^\circ\text{C})$, versus junction temperature T_j .

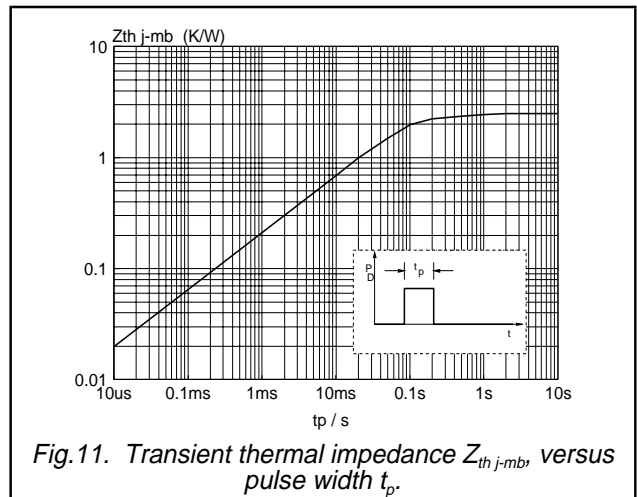


Fig.11. Transient thermal impedance $Z_{th\ j-mb}$, versus pulse width t_p .

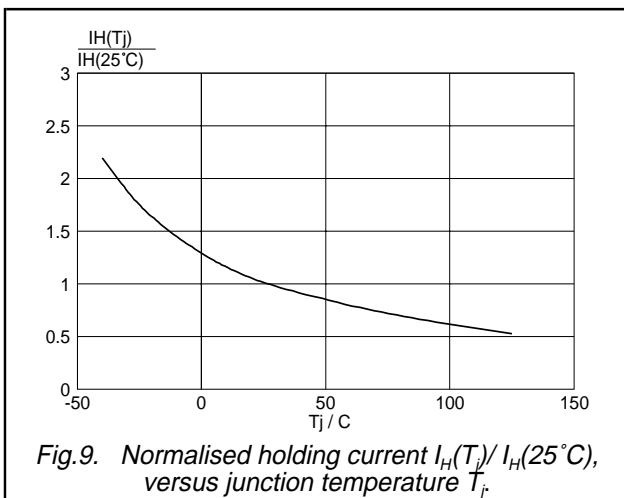


Fig.9. Normalised holding current $I_H(T_j) / I_H(25^\circ\text{C})$, versus junction temperature T_j .

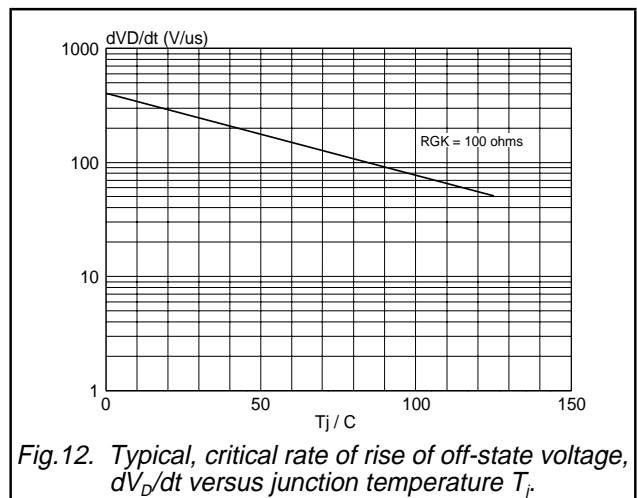


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .

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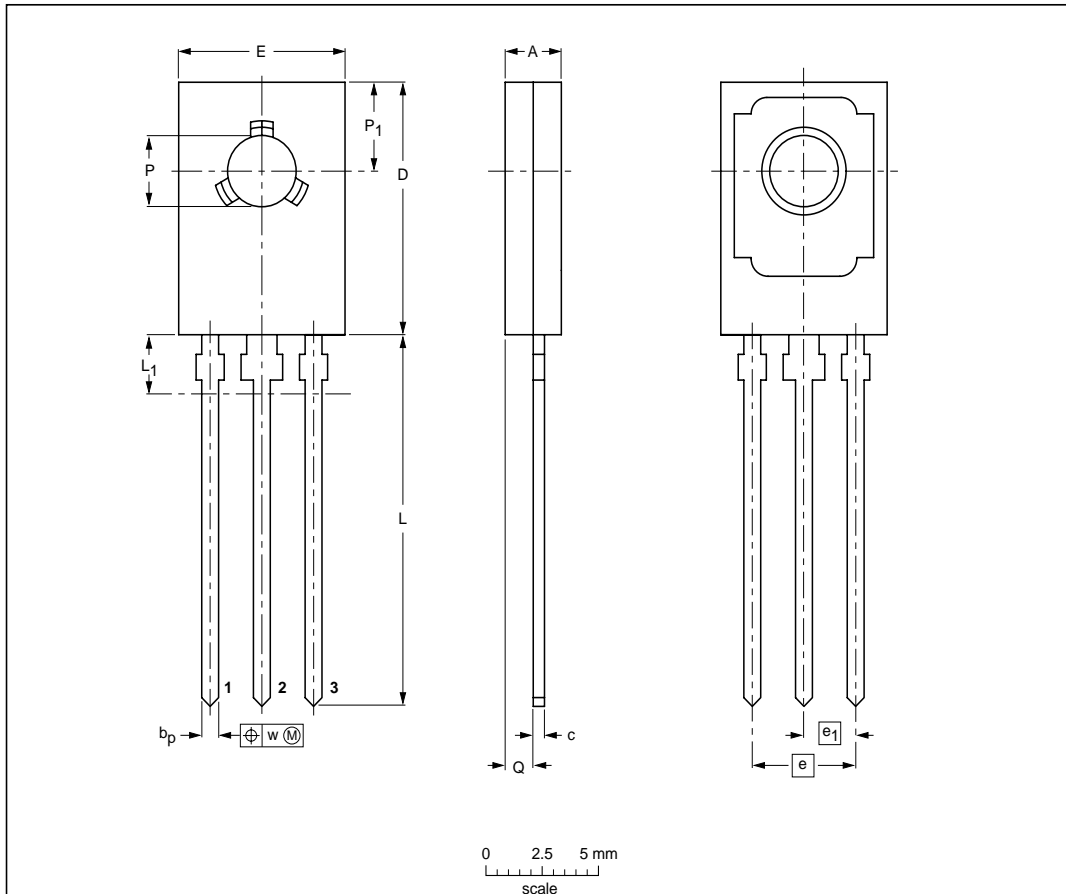
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MECHANICAL DATA

Dimensions in mm

Net Mass: 0.8 g

Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads SOT32



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	L	L ₁ ⁽¹⁾ max	Q	P	P ₁	w
mm	2.7 2.3	0.88 0.65	0.60 0.45	11.1 10.5	7.8 7.2	4.58	2.29	16.5 15.3	2.54	1.5 0.9	3.2 3.0	3.9 3.6	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT32		TO-126			97-03-04

Fig.13. SOT32.

Notes

1. Refer to mounting instructions for SOT32 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS³	PRODUCT STATUS⁴	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
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Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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