3.3V CMOS 18-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCHR16501A

FEATURES:

- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ± 0.3V, Normal Range**
- **V_{CC} = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in SSOP, TSSOP, and TVSOP packages**

DRIVE FEATURES:

- **Balanced Output Drivers: ±12mA**
- **Low switching noise**

APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
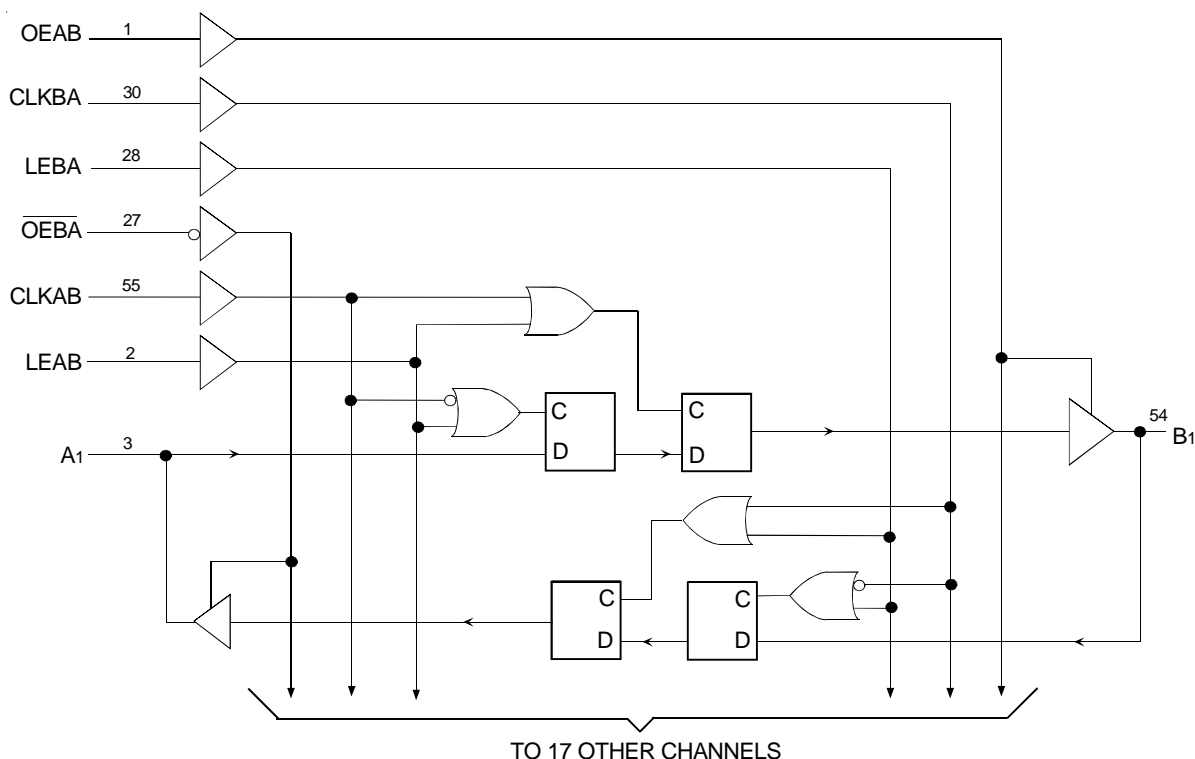- **Data communication and telecommunication systems**

DESCRIPTION:

The LVCHR16501A 18-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low power 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The LVCHR16501A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been developed to drive ±12mA at the designated thresholds.

The LVCHR16501A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.
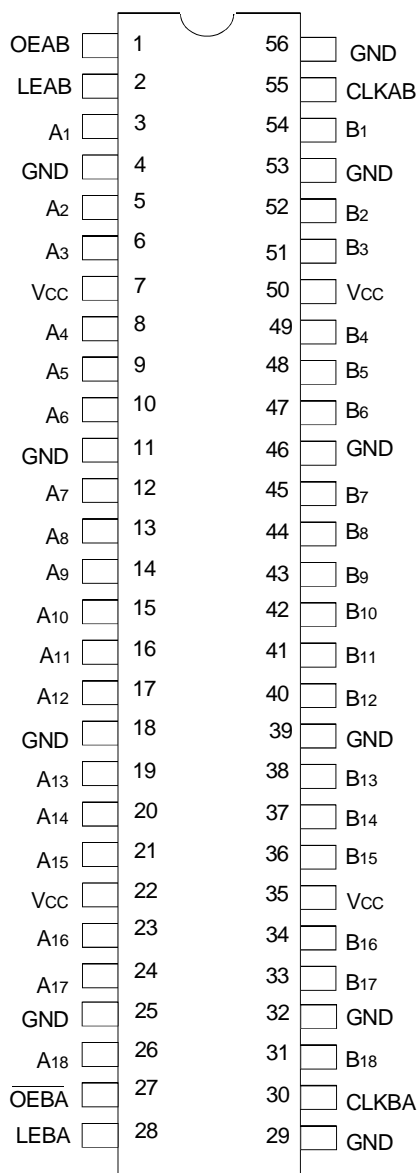
FUNCTIONAL BLOCK DIAGRAM

TO 17 OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

OCTOBER 1999

DSC-4893/1

PIN CONFIGURATION

OEAB	1		56	GND
LEAB	2		55	CLKAB
A_1	3		54	B_1
GND	4		53	GND
A_2	5		52	B_2
A_3	6		51	B_3
V_{CC}	7		50	V_{CC}
A_4	8		49	B_4
A_5	9		48	B_5
A_6	10		47	B_6
GND	11		46	GND
A_7	12		45	B_7
A_8	13		44	B_8
A_9	14		43	B_9
A_{10}	15		42	B_{10}
A_{11}	16		41	B_{11}
A_{12}	17		40	B_{12}
GND	18		39	GND
A_{13}	19		38	B_{13}
A_{14}	20		37	B_{14}
A_{15}	21		36	B_{15}
V_{CC}	22		35	V_{CC}
A_{16}	23		34	B_{16}
A_{17}	24		33	B_{17}
GND	25		32	GND
A_{18}	26		31	B_{18}
$\overline{OEBA}$	27		30	CLKBA
LEBA	28		29	GND

SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A x	A-to-B Data Inputs or B-to-A 3-State Outputs[1]
B x	B-to-A Data Inputs or A-to-B 3-State Outputs[1]

NOTE:
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ($T_A = +25°C$, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	$V_{IN} = 0V$	6.5	8	pF

NOTE:
1. As applicable to the device type.

FUNCTION TABLE[1,2]

Inputs				Output
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[3]
H	L	H	X	B[4]

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A = -40°C$ to $+85°C$

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3V$ to $2.7V$		1.7	—	—	V
		$V_{CC} = 2.7V$ to $3.6V$		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3V$ to $2.7V$		—	—	0.7	V
		$V_{CC} = 2.7V$ to $3.6V$		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6V$	$V_I = 0$ to $5.5V$	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6V$	$V_O = 0$ to $5.5V$	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0V$, V_{IN} or $V_O \leq 5.5V$		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3V$, $I_{IN} = -18mA$		—	–0.7	–1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3V$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6V$	$V_{IN} = GND$ or V_{CC}	—	—	10	µA
			$3.6 \leq V_{IN} \leq 5.5V^{(2)}$	—		10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6V$, other inputs at V_{CC} or GND		—	—	500	µA

NOTES:
1. Typical values are at $V_{CC} = 3.3V$, $+25°C$ ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	$V_{CC} = 3V$	$V_I = 2V$	–75	—	—	µA
I_{BHL}			$V_I = 0.8V$	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3V$	$V_I = 1.7V$	—	—	—	µA
I_{BHL}			$V_I = 0.7V$	—	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6V$	$V_I = 0$ to $3.6V$	—	—	±500	µA

NOTES:
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC} = 3.3V$, $+25°C$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 4mA	1.9	—	
			I_{OH} = – 6mA	1.7	—	
		V_{CC} = 2.7V	I_{OH} = – 4mA	2.2	—	
			I_{OH} = – 8mA	2	—	
		V_{CC} = 3V	I_{OH} = – 6mA	2.4	—	
			I_{OH} = – 12mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 6mA	—	0.55	
		V_{CC} = 2.7V	I_{OL} = 4mA	—	0.4	
			I_{OL} = 8mA	—	0.6	
		V_{CC} = 3V	I_{OL} = 6mA	—	0.55	
			I_{OL} = 12mA	—	0.8	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs enabled	C_L = 0pF, f = 10Mhz		pF
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs disabled			

SWITCHING CHARACTERISTICS[1]

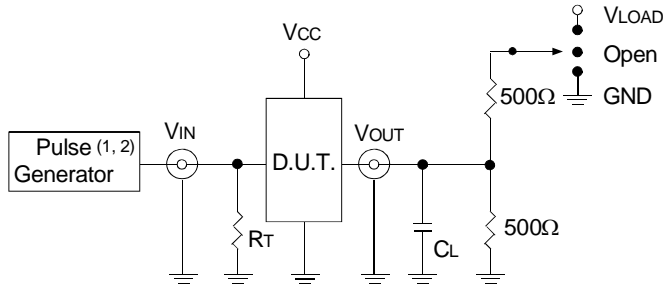| Symbol	Parameter		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
			Min.	Max.	Min.	Max.	
tPLH	Propagation Delay		1.5	7	1.5	6	ns
tPHL	Ax to Bx or Bx to Ax						
tPLH	Propagation Delay		1.5	8	1.5	7	ns
tPHL	LEBA to Ax, LEAB to Bx						
tPLH	Propagation Delay		1.5	8	1.5	6.7	ns
tPHL	CLKBA to Ax, CLKAB to Bx						
tPZH	Output Enable Time		1.5	8.2	1.5	7.2	ns
tPZL	$\overline{OEBA}$ to Ax, OEAB to Bx						
tPHZ	Output Disable Time		1.5	8	1.5	7	ns
tPLZ	$\overline{OEBA}$ to Ax, OEAB to Bx						
tSU	Set-up Time, HIGH or LOW		2.5	—	2.5	—	ns
	Ax to CLKAB, Bx to CLKBA						
tH	Hold Time, HIGH or LOW		0	—	0	—	ns
	Ax to CLKAB, Bx to CLKBA						
tSU	Set-up Time, HIGH or LOW	CLK LOW	2.5	—	2.5	—	ns
	Ax to LEAB, Bx to LEBA	CLK HIGH	2.5	—	2.5	—	
tH	Hold Time, HIGH or LOW		1.5	—	1.5	—	ns
	Ax to LEAB, Bx to LEBA						
tW	Pulse Width HIGH, LEAB or LEBA		3	—	3	—	ns
tW	Pulse Width HIGH or LOW, CLKAB or CLKBA		3	—	3	—	ns
tSK(o)	Output Skew[2]		—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. TA = – 40°C to + 85°C.
2 Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$ = 3.3V±0.3V	$V_{CC}^{(1)}$ = 2.7V	$V_{CC}^{(2)}$ = 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x V_{CC}	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	V_{CC} / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

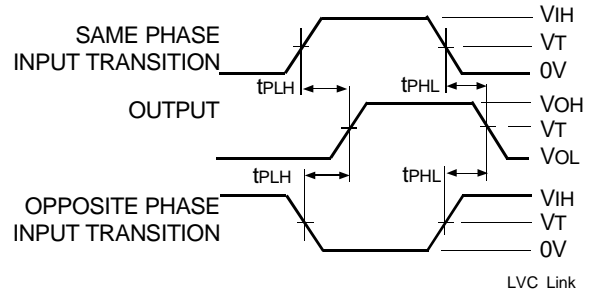| Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open
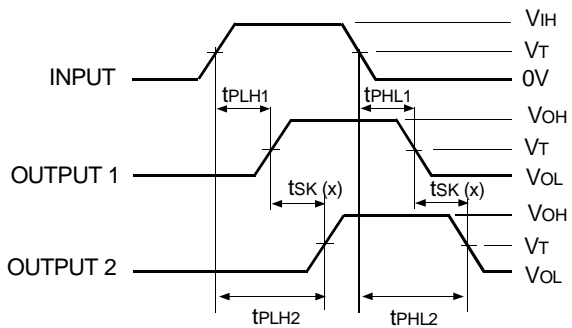
$t_{SK}(x) = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$
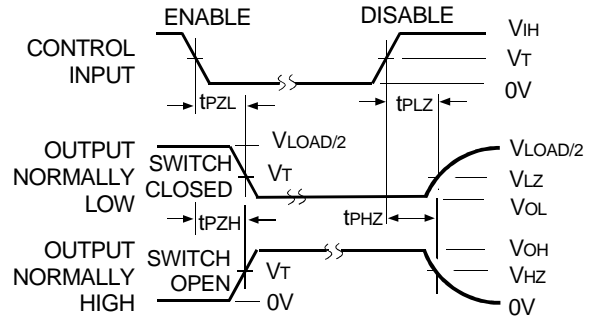
Output Skew - $t_{SK}(x)$

NOTES:
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.
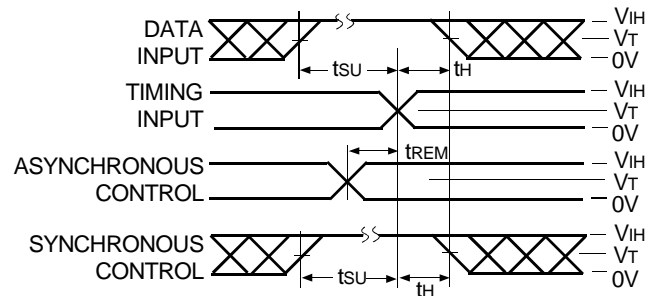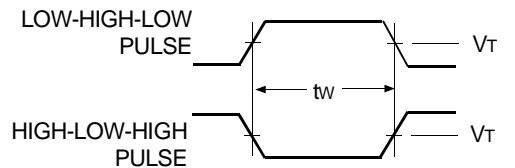

Propagation Delay

Enable and Disable Times

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Set-up, Hold, and Release Times

Pulse Width

ORDERING INFORMATION

IDT   XX   LVC   X   XX   XXXX   XX

Temp. Range   Bus-Hold   Family   Device Type   Package

PV	Shrink Small Outline Package
PA	Thin Shrink Small Outline Package
PF	Thin Very Small Outline Package
501A	18-bit Registered Transceiver
R16	Double-Density, ±12mA
H	Bus-hold
74	-40°C to +85°C