L6562

TRANSITION-MODE PFC CONTROLLER

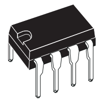
- TRANSITION-MODE CONTROL OF PFC PRE-REGULATORS
- PROPRIETARY MULTIPLIER DESIGN FOR MINIMUM THD OF AC INPUT CURRENT
- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- ULTRA-LOW (≤70µA) START-UP CURRENT
- LOW (≤4 mA) QUIESCENT CURRENT
- EXTENDED IC SUPPLY VOLTAGE RANGE
- ON-CHIP FILTER ON CURRENT SENSE
- DISABLE FUNCTION
- 1% (@ Tj = 25 °C) INTERNAL REFERENCE VOLTAGE
- -600/+800mA TOTEM POLE GATE DRIVER WITH UVLO PULL-DOWN AND VOLTAGE CLAMP
- MINIDIP/SO8 PACKAGES

APPLICATIONS

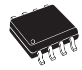
PFC PRE-REGULATORS FOR:

- IEC61000-3-2 COMPLIANT SMPS (TV, DESKTOP PC, MONITOR) UP TO 300W
- HI-END AC-DC ADAPTER/CHARGER
- ENTRY LEVEL SERVER & WEB SERVER

BCD TECHNOLOGY



Minidip (DIP-8)



SO8

ORDERING NUMBERS:

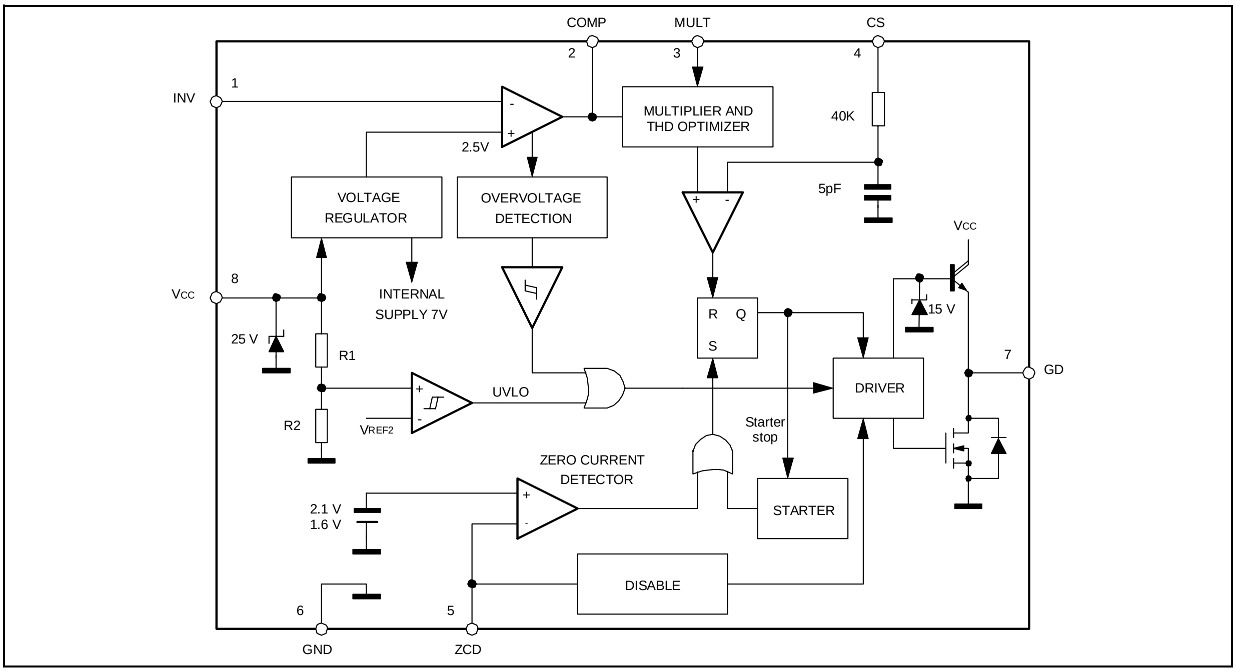
L6562N **L6562D**

DESCRIPTION

The L6562 is a current-mode PFC controller operating in Transition Mode (TM). Pin-to-pin compatible with the predecessor L6561, it offers improved performance.

The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

BLOCK DIAGRAM



The output voltage is controlled by means of a voltage-mode error amplifier and a precise (1% @Tj = 25°C) internal voltage reference.

The device features extremely low consumption (≤70 µA before start-up and <4 mA running) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.).

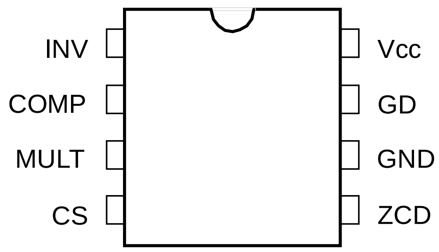
An effective two-step OVP enables to safely handle overvoltages either occurring at start-up or resulting from load disconnection.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOS-FET or IGBT drive which, combined with the other features, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS's up to 300W.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	IC Supply voltage (Icc = 20 mA)	self-limited	V
IGD	7	Output Totem Pole Peak Current	±0.8	A
---	1 to 4	Analog Inputs & Outputs	-0.3 to 8	V
IZCD	5	Zero Current Detector Max. Current	-50 (source) 10 (sink)	mA
P_{tot}		Power Dissipation @Tamb = 50°C (Minidip) (SO8)	1 0.65	W
T_j		Junction Temperature Operating range	-40 to 150	°C
T_{stg}		Storage Temperature	-55 to 150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	SO8	Minidip	Unit
$R_{th\ j\text{-}amb}$	Max. Thermal Resistance, Junction-to-ambient	150	100	°C/W

PIN DESCRIPTION

N°	Pin	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

ELECTRICAL CHARACTERISTICS

(T_j = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
V_{CC}	Operating range	After turn-on	10.3		22	V
V_{CCon}	Turn-on threshold	(1)	11	12	13	V
V_{CCOff}	Turn-off threshold	(1)	8.7	9.5	10.3	V
Hys	Hysteresis		2.2		2.8	V
V_Z	Zener Voltage	I_{CC} = 20 mA	22	25	28	V
SUPPLY CURRENT						
$I_{start-up}$	Start-up Current	Before turn-on, V_{CC} =11V		40	70	µA
I_q	Quiescent Current	After turn-on		2.5	3.75	mA
I_{CC}	Operating Supply Current	@ 70 kHz		3.5	5	mA
I_q	Quiescent Current	During OVP (either static or dynamic) or V_{ZCD} =150 mV			2.2	mA
MULTIPLIER INPUT						
I_{MULT}	Input Bias Current	V_{VFF} = 0 to 4 V			-1	µA
V_{MULT}	Linear Operation Range		0 to 3			V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output Max. Slope	V_{MULT} = 0 to 0.5V V_{COMP} = Upper clamp	1.65	1.9		V/V
K	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V	0.5	0.6	0.7	1/V

ELECTRICAL CHARACTERISTICS (continued)
(T_j = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER						
V_{INV}	Voltage Feedback Input Threshold	T_j = 25 °C	2.465	2.5	2.535	V
		10.3 V < Vcc < 22 V (1)	2.44		2.56	
	Line Regulation	Vcc = 10.3 V to 22V		2	5	mV
I_{INV}	Input Bias Current	V_{INV} = 0 to 3 V			-1	µA
G_v	Voltage Gain	Open loop	60	80		dB
GB	Gain-Bandwidth Product			1		MHz
I_{COMP}	Source Current	V_{COMP} = 4V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink Current	V_{COMP} = 4V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper Clamp Voltage	I_{SOURCE} = 0.5 mA	5.3	5.7	6	V
	Lower Clamp Voltage	I_{SINK} = 0.5 mA (1)	2.1	2.25	2.4	V
CURRENT SENSE COMPARATOR						
I_{CS}	Input Bias Current	V_{CS} = 0			-1	µA
$t_{d(H-L)}$	Delay to Output			200	350	ns
$V_{CS\ clamp}$	Current sense reference clamp	V_{COMP} = Upper clamp	1.6	1.7	1.8	V
$V_{CSoffset}$	Current sense offset	V_{MULT} = 0		30		mV
		V_{MULT} = 2.5V		5		
ZERO CURRENT DETECTOR						
V_{ZCDH}	Upper Clamp Voltage	I_{ZCD} = 2.5 mA	5.0	5.7	6.5	V
V_{ZCDL}	Lower Clamp Voltage	I_{ZCD} = -2.5 mA	0.3	0.65	1	V
V_{ZCDA}	Arming Voltage (positive-going edge)	(3)		2.1		V
V_{ZCDT}	Triggering Voltage (negative-going edge)	(3)		1.6		V
I_{ZCDb}	Input Bias Current	V_{ZCD} = 1 to 4.5 V		2		µA
I_{ZCDsrc}	Source Current Capability		-2.5		-5.5	mA
I_{ZCDsnk}	Sink Current Capability		2.5			mA
V_{ZCDdis}	Disable threshold		150	200	250	mV
V_{ZCDen}	Restart threshold				350	mV
I_{ZCDres}	Restart Current after Disable		30	75		µA
STARTER						
t_{START}	Start Timer period		75	130	300	µs
OUTPUT OVERVOLTAGE						
I_{OVP}	Dynamic OVP triggering current		35	40	45	µA
Hys	Hysteresis	(3)		30		µA
	Static OVP threshold	(1)	2.1	2.25	2.4	V
GATE DRIVER						
V_{OH}	Dropout Voltage	$I_{GDsource}$ = 20 mA		2	2.6	
		$I_{GDsource}$ = 200 mA		2.5	3	V
V_{OL}		I_{GDsink} = 200 mA		0.9	1.9	V

ELECTRICAL CHARACTERISTICS (continued)
(T_j = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_f	Voltage Fall Time			30	70	ns
t_r	Voltage Rise Time			40	80	ns
V_{Oclamp}	Output clamp voltage	$I_{GDsource}$ = 5mA; Vcc = 20V	10	12	15	V
	UVLO saturation	V_{CC} = 0 to V_{CCon}, I_{sink}=10mA			1.1	V

(1) All parameters are in tracking
(2) The multiplier output is given by: $V_{cs} = K \cdot V_{MULT} \cdot (V_{COMP} - 2.5)$
(3) Parameters guaranteed by design, functionality tested in production.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. Supply current vs. Supply voltage

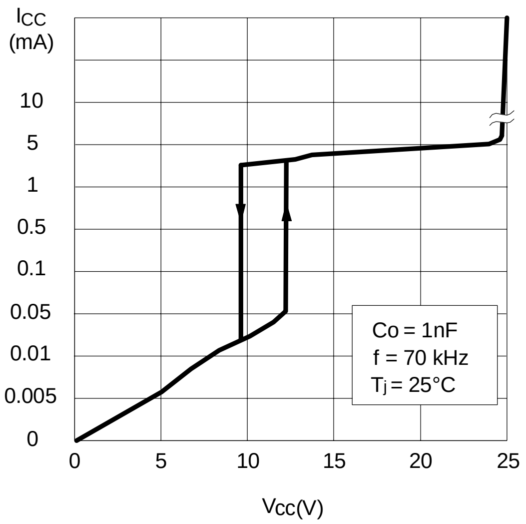


Figure 3. IC consumption vs. T_j

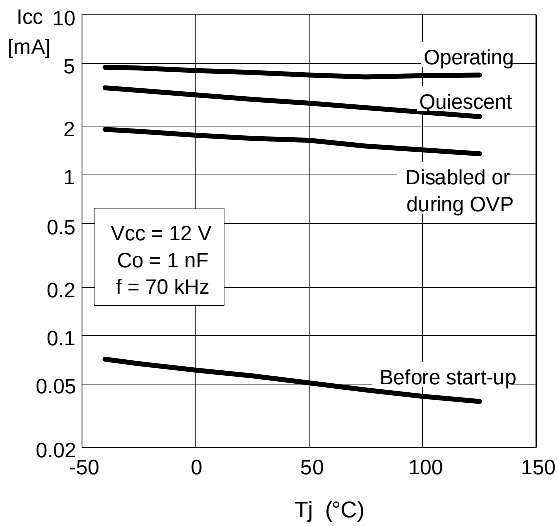


Figure 2. Start-up & UVLO vs. T_j

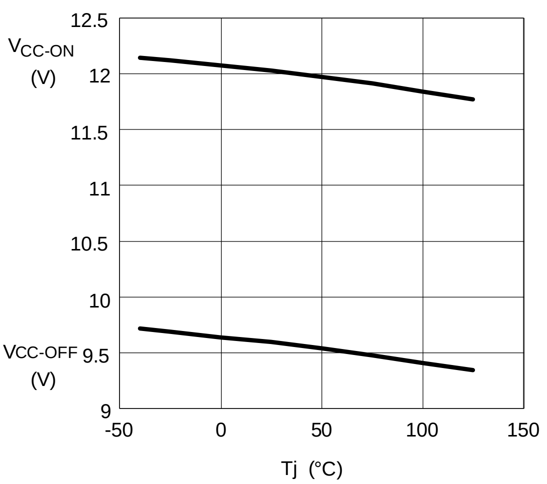


Figure 4. Vcc Zener voltage vs. T_j

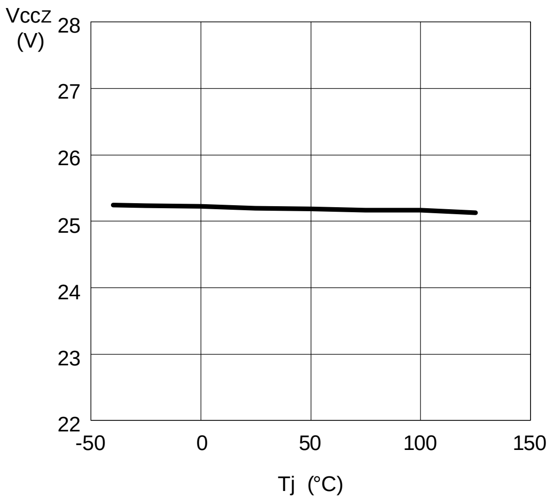


Figure 5. Feedback reference vs. T_j

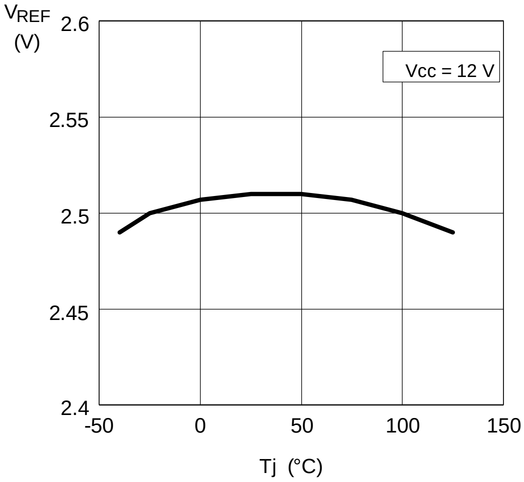


Figure 6. OVP current vs. T_j

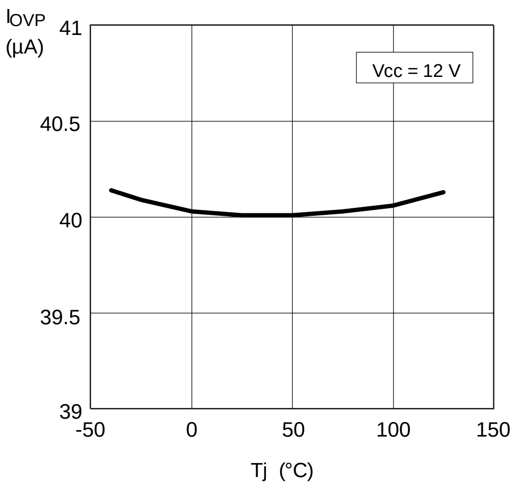


Figure 7. E/A output clamp levels vs. T_j

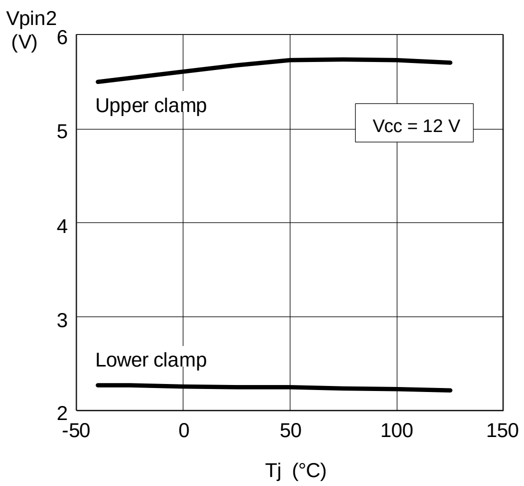


Figure 8. Delay-to-output vs. T_j

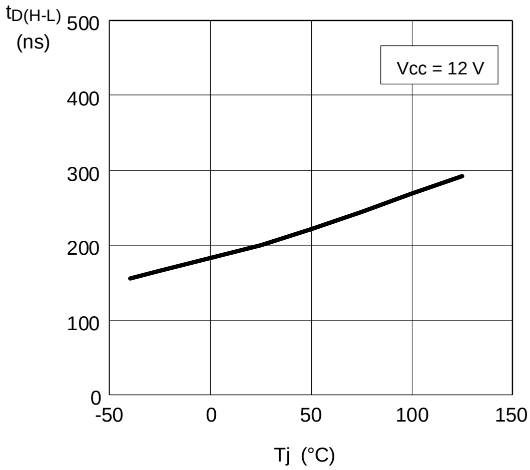


Figure 9. Multiplier characteristic

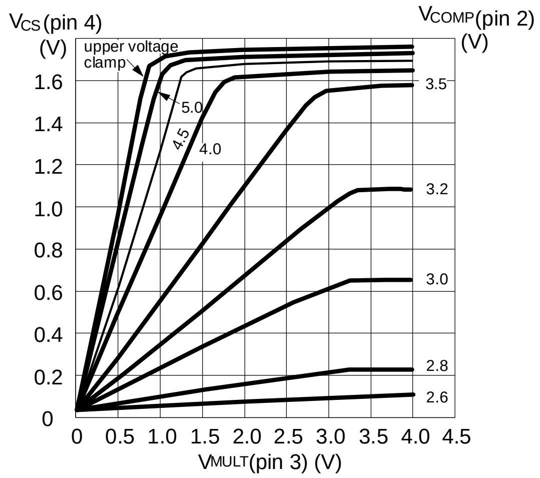


Figure 10. Multiplier gain vs. T_j

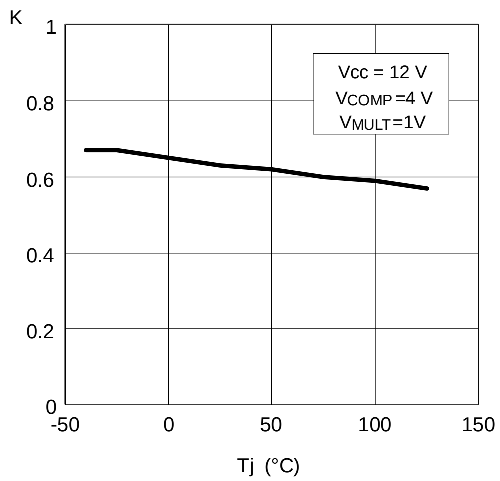


Figure 11. Vcs clamp vs. T_j

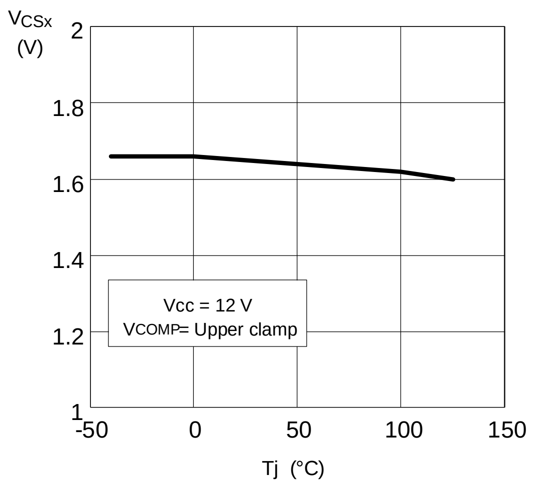


Figure 14. ZCD source capability vs. T_j

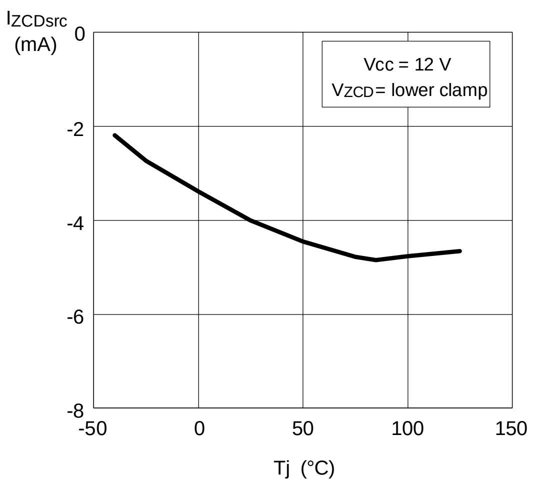


Figure 12. Start-up timer vs. T_j

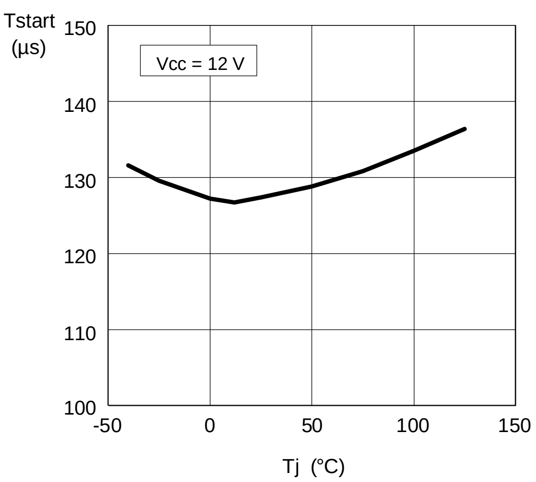


Figure 15. Gate-drive output low saturation

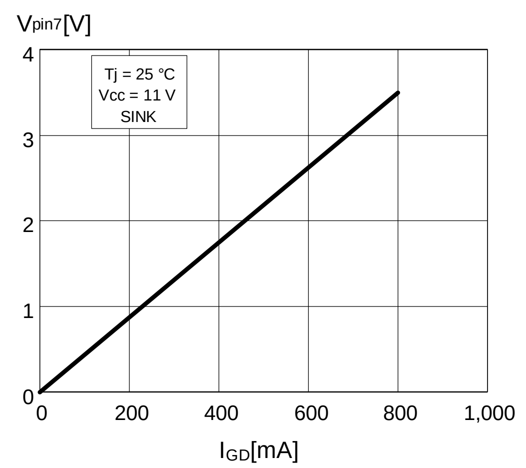


Figure 13. ZCD clamp levels vs. T_j

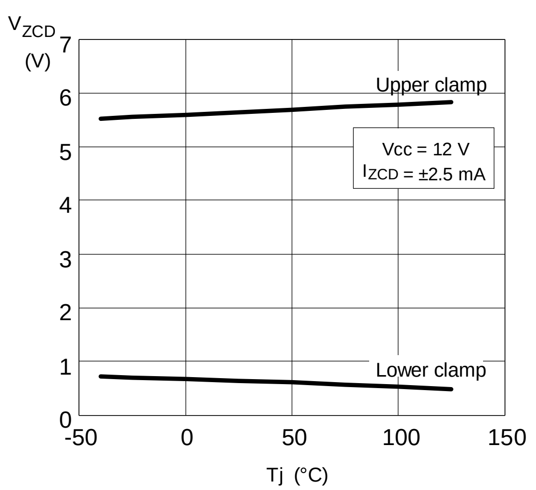


Figure 16. Gate-drive output high saturation

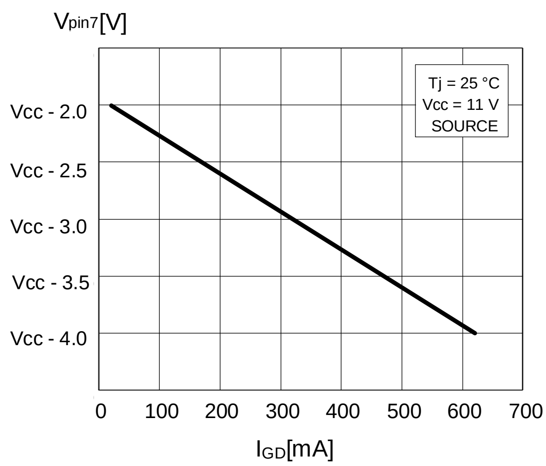


Figure 17. Gate-drive clamp vs. T_j

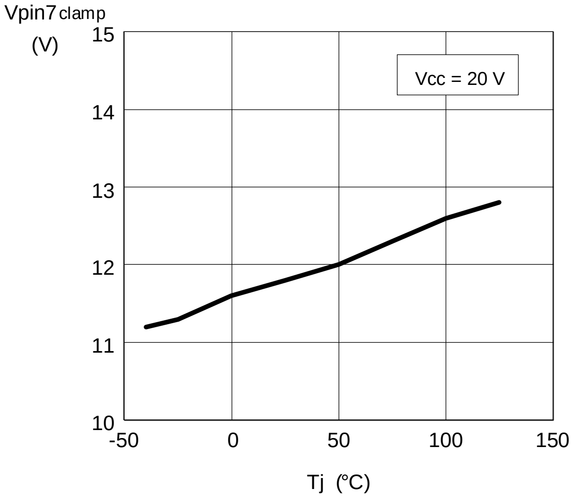
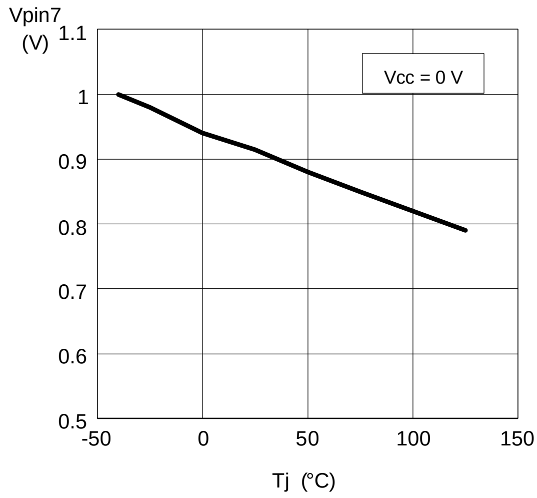


Figure 18. UVLO saturation vs. T_j



APPLICATION INFORMATION

Overvoltage protection

Under steady-state conditions, the voltage control loop keeps the output voltage Vo of a PFC pre-regulator close to its nominal value, set by the resistors R1 and R2 of the output divider. Neglecting ripple components, the current through R1, I_{R1}, equals that through R2, I_{R2}. Considering that the non-inverting input of the error amplifier is internally referenced at 2.5V, also the voltage at pin INV will be 2.5V, then:

$$I_{R2} = \frac{2.5}{R2} = I_{R1} = \frac{Vo - 2.5}{R1} .$$

If the output voltage experiences an abrupt change $\Delta Vo > 0$ due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant to achieve high PF (this is why ΔVo can be large). As a result, the current through R2 will remain equal to 2.5/R2 but that through R1 will become:

$$I'_{R1} = \frac{Vo - 2.5 + \Delta Vo}{R1} .$$

The difference current $\Delta I_{R1}=I'_{R1}-I_{R2}=I'_{R1}-I_{R1}=\Delta Vo/R1$ will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the L6562 and if it reaches about 37 µA the output voltage of the multiplier is forced to decrease, thus smoothly reducing the energy delivered to the output. As the current exceeds 40 µA, the OVP is triggered (Dynamic OVP): the gate-drive is forced low to switch off the external power transistor and the IC put in an idle state. This condition is maintained until the current falls below approximately 10 µA, which re-enables the internal starter and allows switching to restart. The output ΔVo that is able to trigger the Dynamic OVP function is then:

$$\Delta Vo = R1 \cdot 40 \cdot 10^{-6} .$$

An important advantage of this technique is that the OV level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 12%, that is 12% tolerance on ΔVo. Since $\Delta Vo << Vo$, the tolerance on the absolute value will be proportionally reduced.

Example: Vo = 400 V, ΔVo = 40 V. Then: R1=40V/40µA=1MΩ; R2=1MΩ·2.5/(400-2.5)=6.289kΩ. The tolerance on the OVP level due to the L6562 will be 40·0.12=4.8V, that is 1.2% of the regulated value.

When the load of a PFC pre-regulator is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low; hence, when this is detected, the external power transistor is switched off and the IC put in an idle state (Static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the L6562 will work in burst-mode, with a repetition rate that can be very low.

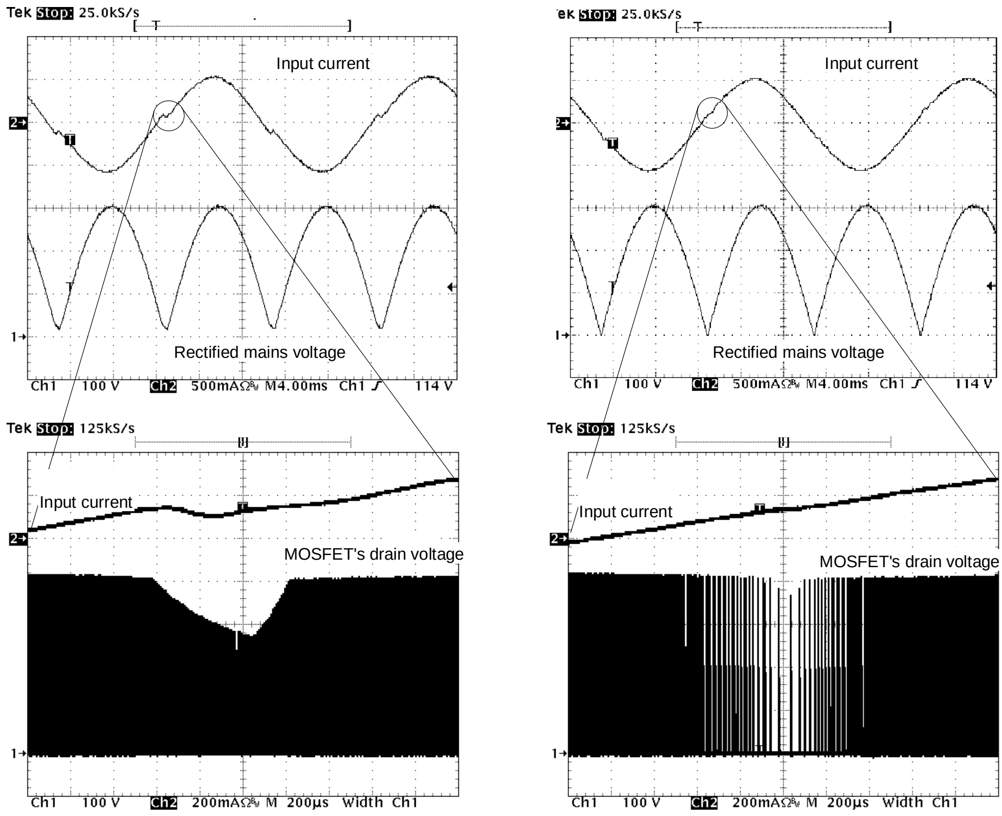
When either OVP is activated the quiescent consumption of the IC is reduced to minimize the discharge of the Vcc capacitor and increase the hold-up capability of the IC supply system.

THD optimizer circuit

The L6562 is equipped with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (Total Harmonic Distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

Figure 19. THD optimization: standard TM PFC controller (left side) and L6562 (right side)



To overcome this issue the circuit embedded in the L6562 forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. The effect of the circuit is shown in figure 19, where the key waveforms of a standard TM PFC controller are compared to those of the L6562.

Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid.

To maximally benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus making the action of the optimizer circuit little effective.

Figure 20. Typical application circuit (250W, Wide-range mains)

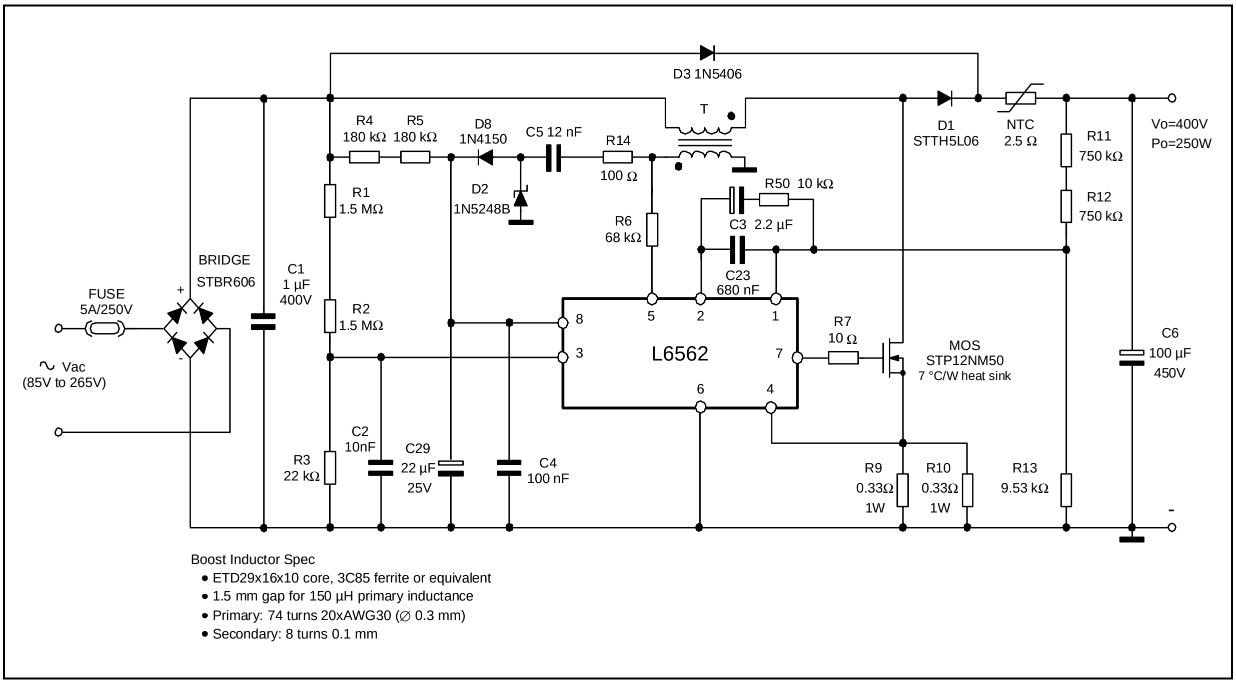


Figure 21. Demo board (EVAL6562N, 80W, Wide-range mains): Electrical schematic

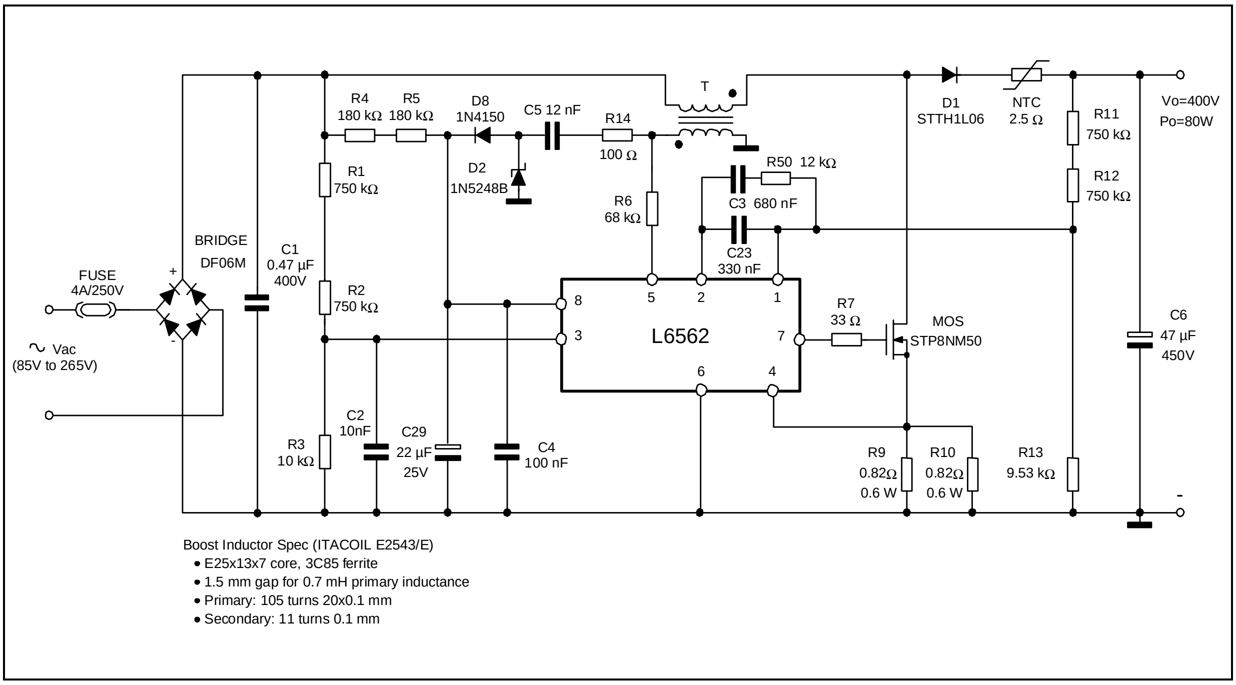


Figure 22. EVAL6562N: PCB and component layout (Top view, real size: 57 x 108 mm)

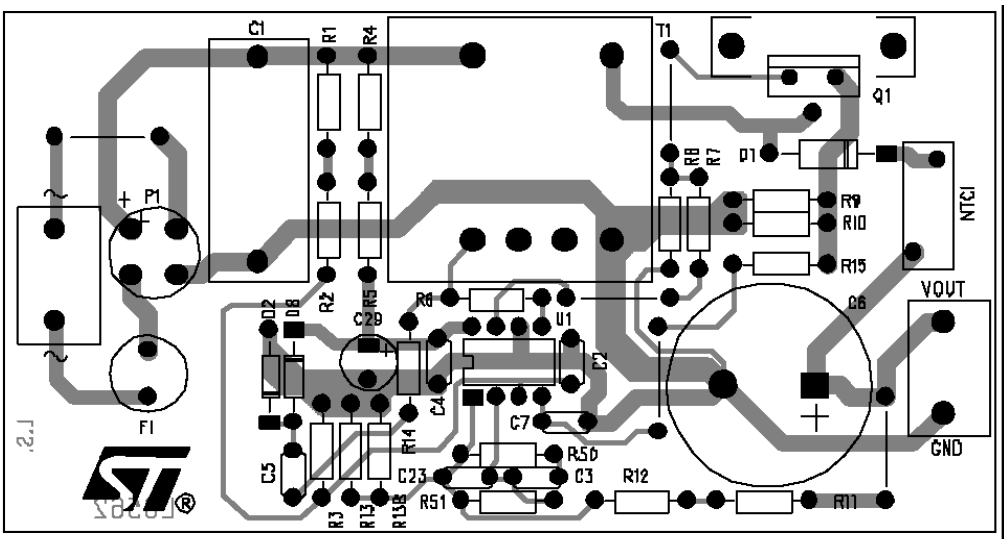


Table 1. EVAL6562N: Evaluation results at full load

Vin (V_{AC})	Pin (W)	Vo (V_{DC})	$\Delta Vo(V_{pk-pk})$	Po (W)	η (%)	PF	THD (%)
85	86.4	394.79	12.8	80.16	92.8	0.998	3.6
110	84.6	394.86	12.8	80.20	94.8	0.996	4.2
135	83.8	394.86	12.8	80.20	95.7	0.991	4.9
175	83.2	394.87	15.5	80.20	96.4	0.981	6.5
220	82.9	394.87	15.7	80.20	96.7	0.956	7.8
265	82.7	394.87	15.9	80.20	97.0	0.915	9.2

Note: measurements done with the line filter shown in figure 23

Table 2. EVAL6562N: Evaluation results at half load

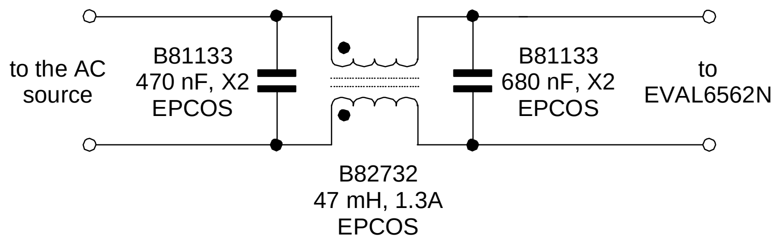
Vin (V_{AC})	Pin (W)	Vo (V_{DC})	$\Delta Vo(V_{pk-pk})$	Po (W)	η (%)	PF	THD (%)
85	42.8	394.86	6.6	40.20	93.9	0.994	5.5
110	42.5	394.90	6.6	40.20	94.6	0.985	6.2
135	42.5	394.91	6.7	40.20	94.6	0.967	7.1
175	42.5	394.93	8.0	40.19	94.6	0.939	8.3
220	42.6	394.94	8.2	40.19	94.3	0.869	9.8
265	42.6	394.94	8.3	40.19	94.3	0.776	11.4

Note: measurements done with the line filter shown in figure 23

Table 3. EVAL6562N: No-load measurements

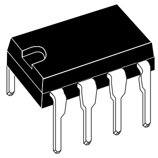
Vin (V_{AC})	Pin (W)	Vo (V_{DC})	ΔVo(V_{pk-pk})	Po (W)
85	0.4	396.77	0.45	0
110	0.3	396.82	0.55	0
135	0.3	396.83	0.60	0
175 (*)	0.4	396.90	1.00	0
220 (*)	0.4	396.95	1.40	0
265 (*)	0.5	396.98	1.65	0
(*) Vcc = 12V supplied externally				

Figure 23. Line filter (not tested for EMI compliance) used for EVAL6562N evaluation

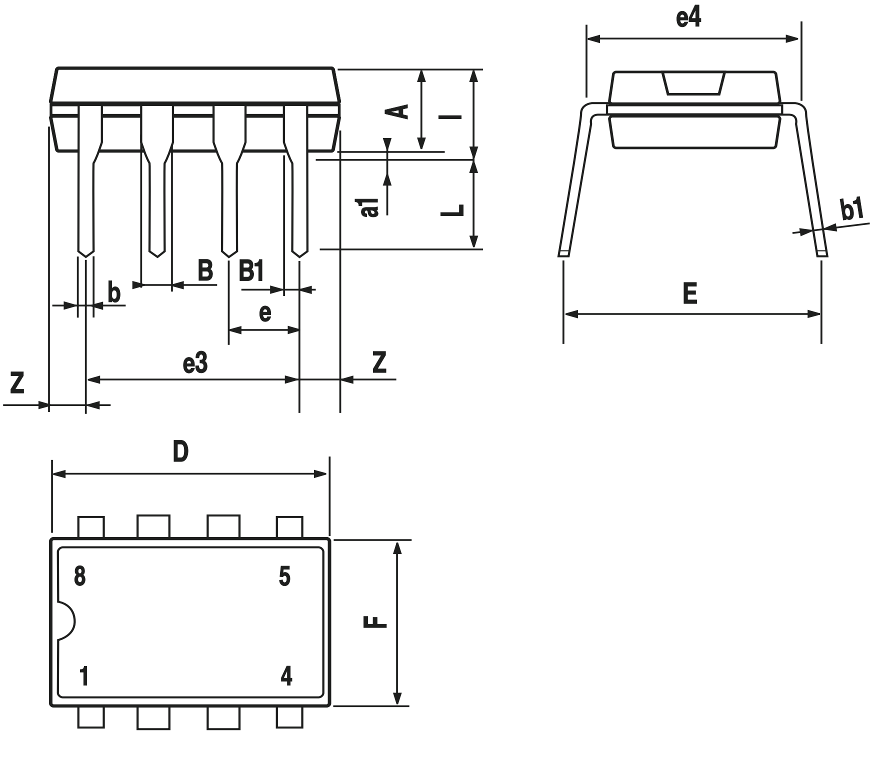


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



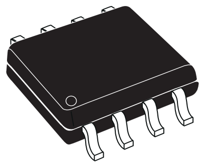
Minidip



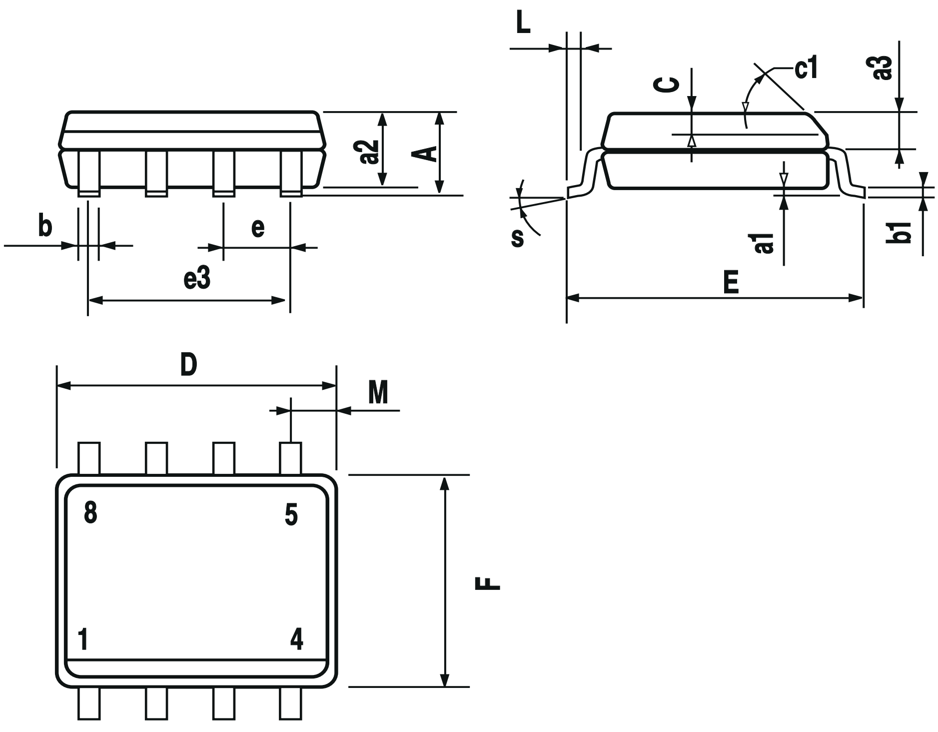
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



SO8



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