

**GENERAL DESCRIPTION**

The N1164 is a 5 bit TTL-compatible input, digital-to-analog (DAC) programmable, synchronous buck converter with dual LDOs controller designed specifically to power the Pentium® II as well as the next generation of P6 family or other high performance core logic in desktop personal computer and file servers CPU applications.

The N1164 switching section provides programmability of output voltage from 1.3V to 2.05V in 50mV steps and 2.0V to 3.5V in 100 mV increments and the linear sections use external N-Channel power MOSFETs to provide fixed output voltages of 1.5V for GTL bus and 2.5V for clock.

The N1164 monitors all the output voltages. A signal Power-Good signal is issued when the core is within ±15% of the DAC setting. Additional features are built-in over-voltage, over-current protections for the core output and logic compatible shutdown.

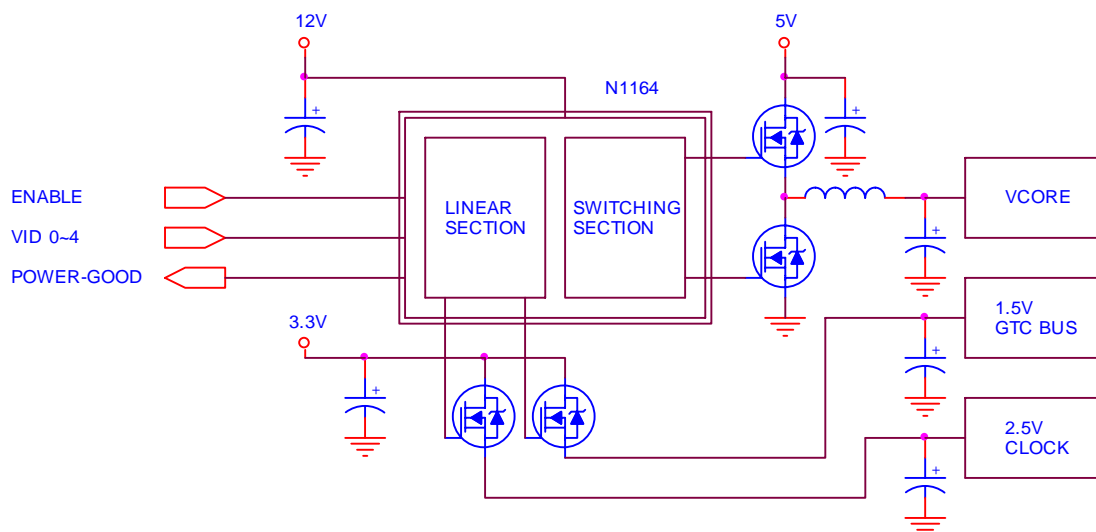
**FEATURES**

- Synchronous operation with high efficiency
- TTL-compatible 5 bit DAC, output voltage selection from 1.3V to 3.5V programmable
- High current totem pole output, up to 2 A for direct driving of the external N-Channel power MOSFETs.
- 200 KHz fixed frequency internal oscillator
- Fast transient response
- Provides 2 regulated voltages, 1.5V and 2.5V for linear section
- Power-Good output voltage monitor
- Over-Voltage and Over-Current protection
- Logic level enable input
- High performance and low cost solution

**APPLICATIONS**

- Powering Pentium® II, III or Deschutes, K6 and other advanced processor
- High power DC to DC controller with triple output supplies

**TYPICAL APPLICATION**



**N1164, Motherboard Power Regulation for Computers**

**ABSOLUTE MAXIMUM RATINGS**

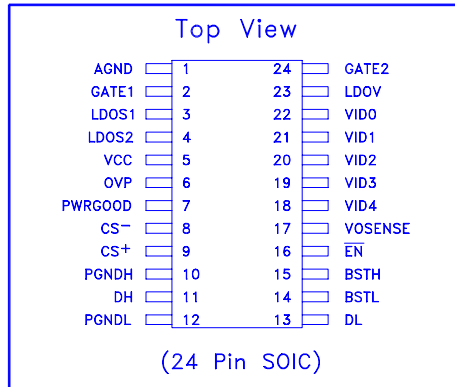
● $V_{CC}$ to GND	- 0.3V to 7V	● Operating Temperature Range, $T_A$	0 to 70 °C
● BST to GND	-0.3V to 15V	● Operating Junction Temperature Range, $T_J$	0 to 125 °C
● Thermal Resistance Junction to Case, $\theta_{JC}$	25 °C/W	● Storage Temperature Range, $T_{STG}$	-65 to 150 °C
● Thermal Resistance Junction to Ambient, $\theta_{JA}$	80 °C/W	● Lead Temperature, $T_{LEAD}$ (Soldering, 10 Seconds)	300 °C

**ELECTRICAL SPECIFICATIONS**

<Unless specified:  $V_{CC} = 4.75V \sim 5.25V$ ,  $GND = PGND = 0V$ ,  $V_{OSENSE} = V_O$ ,  $0mV < (CS^+ - CS^-) < 60mV$ ,  $LDOV = 11.4V \sim 12.6V$ ,  $T_A = 25^\circ C$ >

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SWITCHING SECTION</b>					
Supply Voltage	$V_{CC}$	4.5		7	V
Supply Current	$V_{CC} = 5.0V$		8	15	mA
Output Voltage	$I_O = 2A$	See Table 1.			
Load Regulation	$I_O = 0.3A$ to 15A		1		%
Line Regulation	All VID Codes		0.5		%
Gain ( $A_{OL}$ )	$V_{OSENSE}$ to $V_O$		35		dB
Current Limit Voltage		55	70	85	mV
Oscillator Frequency		175	200	225	KHz
Oscillator Max Duty Cycle		90	95		%
Peak DH Sink/Source Current	BSTH - DH = 4.5V, DH - PGNDH = 2V	1			A
Peak DL Sink/Source Current	BSTL - DL = 4.5V, DL - PGNDL = 2V	1			A
OVP Threshold Voltage			120		%
OVP Source Current	$V_{OVP} = 3.0V$	10			mA
Power-Good Threshold Voltage		85		115	%
Dead Time		100	200		nS
<b>LINEAR SECTIONS</b>					
Quiescent Current	$LDOV = 12V$			5	mA
Output Voltage (LDO1)		2.45	2.500	2.55	V
Output Voltage (LDO2)		1.47	1.500	1.53	V
Load Regulation	$I_O = 0$ to 8A		1		%
Line Regulation			1		%
Output Impedance			1		K $\Omega$

**PIN CONFIGURATIONS**



**PIN DEFINITIONS**

Pin #	Pin Name	Pin Function Description
1	AGND	Small signal analog and digital ground
2	GATE1	Gate drive output LDO1
3	LDOS1	Sense input for LDO1
4	LDOS2	Sense input for LDO2
5	V <sub>CC</sub>	Input voltage
6	OVP	High signal out if V <sub>O</sub> >set point +20%
7	PWRGOOD*	Open collector logic output, high if V <sub>O</sub> within 10% of set point
8	CS <sup>-</sup>	Current sense input (Negative)
9	CS <sup>+</sup>	Current sense input (Positive)
10	PGNDL	Power ground for high side switch
11	DH	High side driver output
12	PGNDL	Power ground for low side switch
13	DL	Low side driver output
14	BSTL	Supply for low side driver
15	BSTH	Supply for high side driver
16	EN*	Logic low shuts down the converter; high or open for normal operation.
17	VOSENSE	Top end of internal feedback chain
18	VID4*	Programming input (MSB)
19	VID3*	Programming input
20	VID2*	Programming input
21	VID1*	Programming input
22	VID0*	Programming input (LSB)
23	LDOV	+12V for LDO section
24	GATE2	Gate drive output LDO2

\* : All logic level inputs and outputs are open collector TTL compatible.

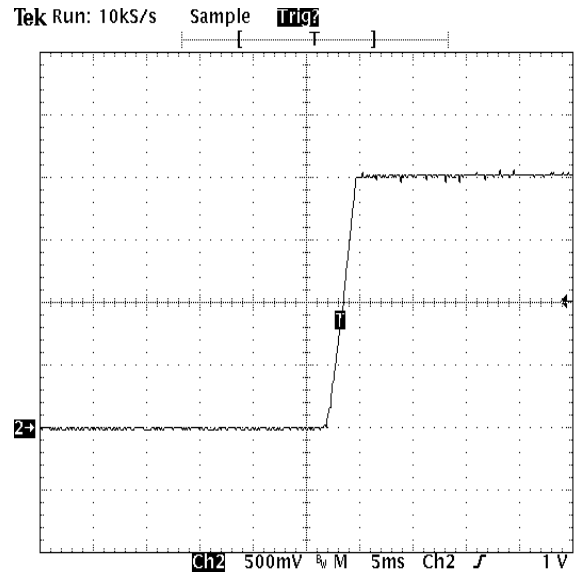
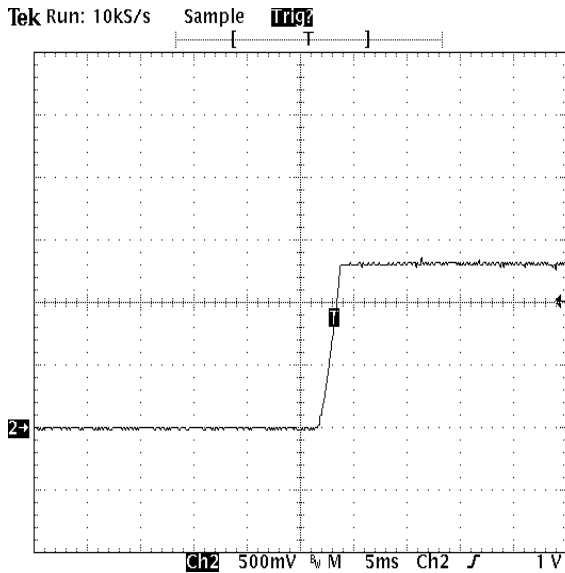
**OUTPUT VOLTAGE**

<Unless specified:  $V_{CC} = 4.75V \sim 5.25V$ ,  $GND = PGND = 0V$ ,  $V_{OSENSE} = V_O$ ,  $0mV < (CS^+ - CS^-) < 60mV$ ,  $LDOV = 11.4V \sim 12.6V$ ,  $T_A = 25^\circ C$ >

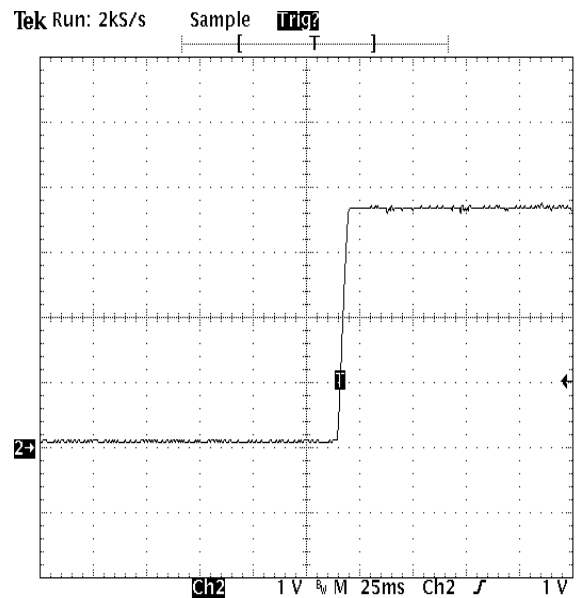
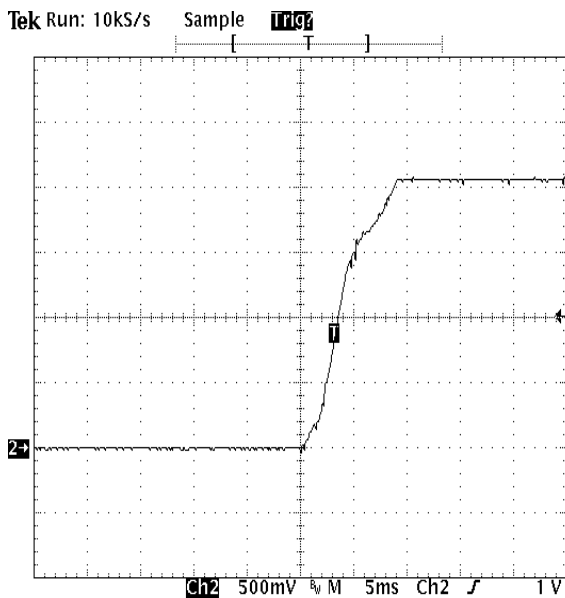
– Table 1 –

VID 4 3 2 1 0	Min. (V)	Typ. (V)	Max. (V)
0 1 1 1 1	1.274	1.300	1.326
0 1 1 1 0	1.323	1.350	1.377
0 1 1 0 1	1.372	1.400	1.428
0 1 1 0 0	1.421	1.450	1.479
0 1 0 1 1	1.470	1.500	1.530
0 1 0 1 0	1.527	1.550	1.573
0 1 0 0 1	1.576	1.600	1.624
0 1 0 0 0	1.625	1.650	1.675
0 0 1 1 1	1.675	1.700	1.726
0 0 1 1 0	1.724	1.750	1.776
0 0 1 0 1	1.773	1.800	1.827
0 0 1 0 0	1.822	1.850	1.878
0 0 0 1 1	1.871	1.900	1.929
0 0 0 1 0	1.921	1.950	1.979
0 0 0 0 1	1.970	2.000	2.030
0 0 0 0 0	2.019	2.050	2.081
1 1 1 1 1	1.940	2.000	2.060
1 1 1 1 0	2.058	2.100	2.142
1 1 1 0 1	2.156	2.200	2.244
1 1 1 0 0	2.254	2.300	2.346
1 1 0 1 1	2.352	2.400	2.448
1 1 0 1 0	2.450	2.500	2.550
1 1 0 0 1	2.548	2.600	2.652
1 1 0 0 0	2.646	2.700	2.754
1 0 1 1 1	2.744	2.800	2.856
1 0 1 1 0	2.842	2.900	2.958
1 0 1 0 1	2.940	3.000	3.060
1 0 1 0 0	3.038	3.100	3.162
1 0 0 1 1	3.136	3.200	3.264
1 0 0 1 0	3.234	3.300	3.366
1 0 0 0 1	3.332	3.400	3.468
1 0 0 0 0	3.430	3.500	3.570

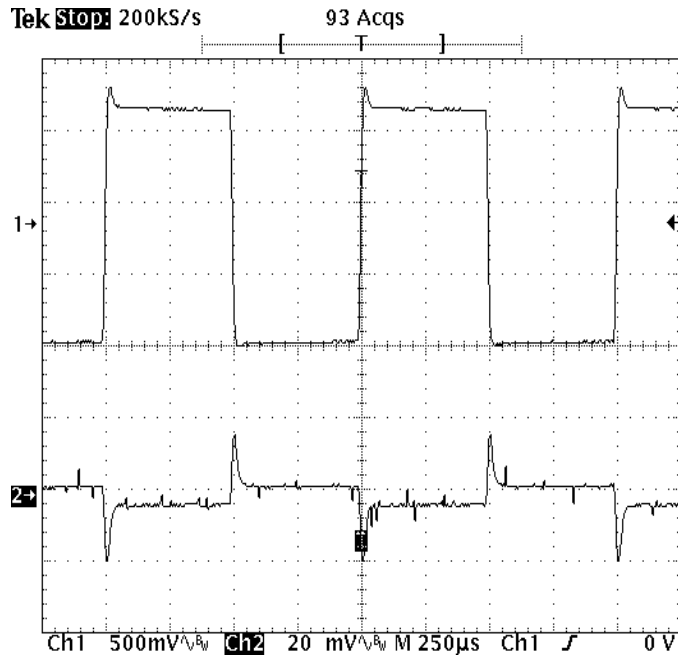
Note:  $I_O = 2.0A$  in Application Circuit



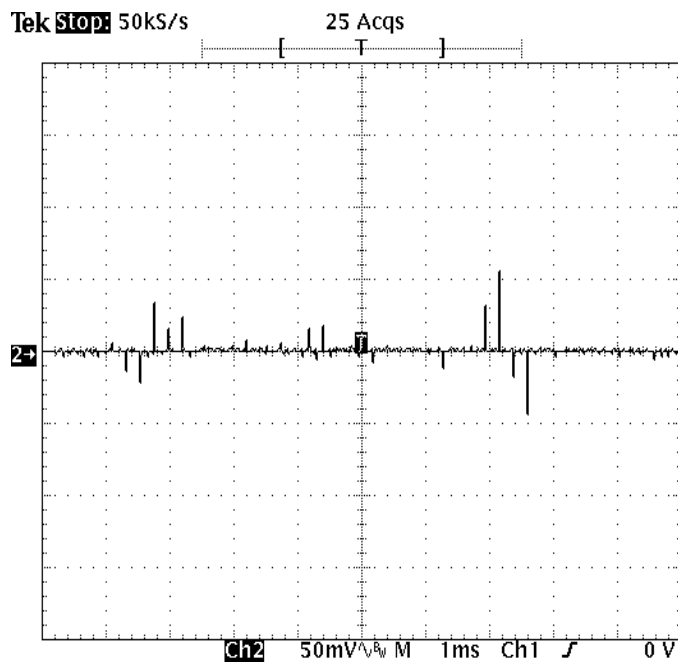
1.3V (VID=01111) - Turn On Overshoot - 2.0V (VID=11111)



2.05V (VID=00000) - Turn On Overshoot - 3.5V (VID=10000)

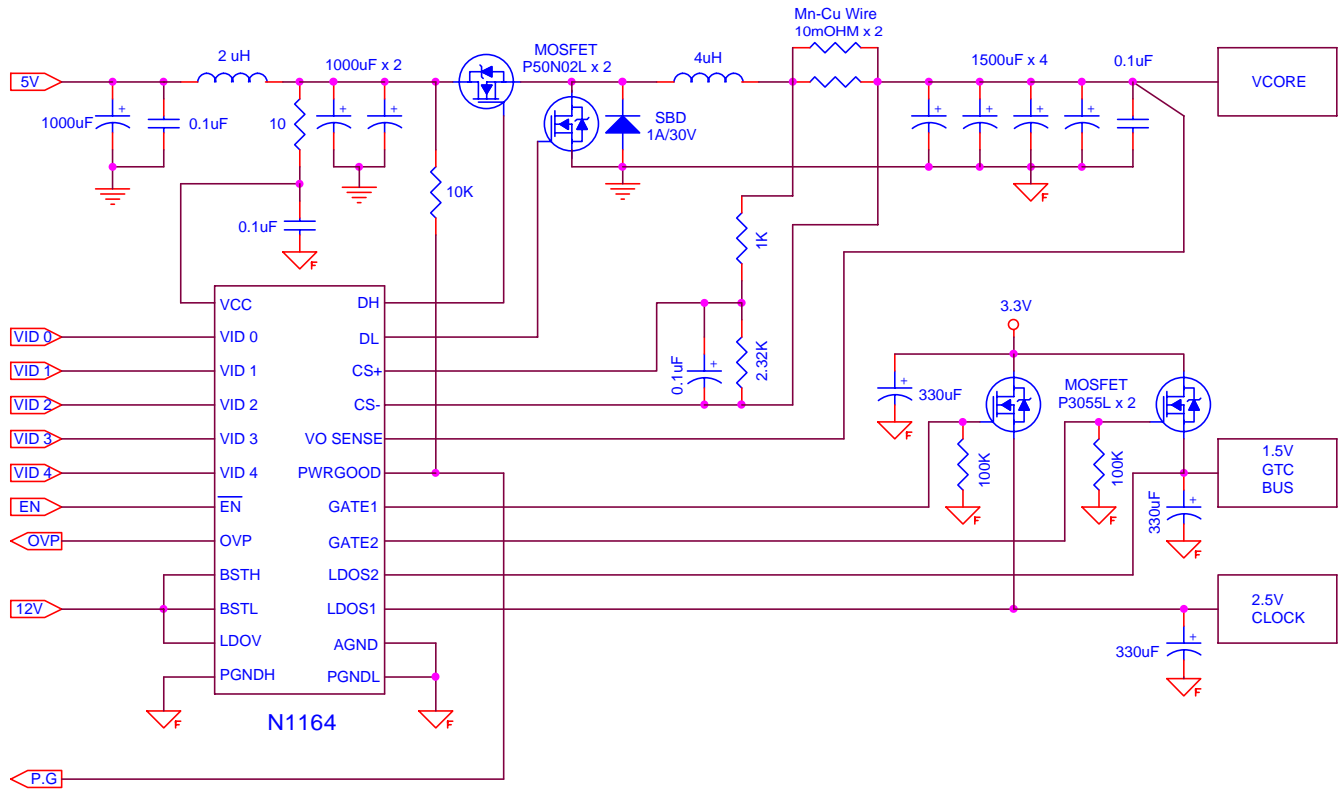


Transient Response,  $V_O=2.8V$ ,  $I_O=0.3A$  to  $10A$



Typical Ripple & Noise,  $V_O=2.8V$ ,  $I_O=10A$

**APPLICATION CIRCUIT**



**SOIC-24 (DW) MECHANICAL DATA**

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	15.2		15.6	H	0.4		1.27
B	7.3		7.7	I	0.23		0.32
C	10		10.65	J	0.25		0.74
D	0.33		0.51	K	0°		8°
E		1.27		L			
F	2.1	2.3	2.5	M			
G	0.1		0.3	N			

