

Complementary Silicon Plastic Power Transistors

... designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
 $V_{CE(sat)} = 1.5 \text{ Vdc (Max) @ } I_C = 6.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage —
 $V_{CEO(sus)} = 60 \text{ Vdc (Min) — TIP41A, TIP42A}$
 $= 80 \text{ Vdc (Min) — TIP41B, TIP42B}$
 $= 100 \text{ Vdc (Min) — TIP41C, TIP42C}$
- High Current Gain — Bandwidth Product
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mAdc}$
- Compact TO–220 AB Package

*MAXIMUM RATINGS

Rating	Symbol	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	6 10			Adc
Base Current	I_B	2.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	65 0.52			Watts W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016			Watts W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	62.5			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

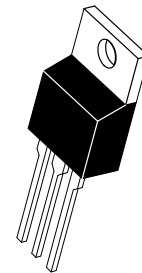
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$

(1) $I_C = 2.5 \text{ A}$, $L = 20 \text{ mH}$, P.R.F. = 10 Hz, $V_{CC} = 10 \text{ V}$, $R_{BE} = 100 \Omega$.

NPN
TIP41A
TIP41B*
TIP41C*
PNP
TIP42A
TIP42B*
TIP42C*

*Motorola Preferred Device

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80–100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

Preferred devices are Motorola recommended choices for future use and best overall value.

TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I _C = 30 mA, I _B = 0)	V _{CEO(sus)}	60 80 100	—	Vdc
Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 60 Vdc, I _B = 0)	I _{CEO}	— — —	0.7 0.7 0.7	mA
Collector Cutoff Current (V _{CE} = 60 Vdc, V _{EB} = 0) (V _{CE} = 80 Vdc, V _{EB} = 0) (V _{CE} = 100 Vdc, V _{EB} = 0)	I _{CES}	— — —	400 400 400	μA
Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0)	I _{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I _C = 0.3 A, V _{CE} = 4.0 Vdc) (I _C = 3.0 A, V _{CE} = 4.0 Vdc)	h _{FE}	30 15	— 75	—
Collector–Emitter Saturation Voltage (I _C = 6.0 A, I _B = 600 mA)	V _{CE(sat)}	—	1.5	Vdc
Base–Emitter On Voltage (I _C = 6.0 A, V _{CE} = 4.0 Vdc)	V _{BE(on)}	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I _C = 500 mA, V _{CE} = 10 Vdc, f _{test} = 1.0 MHz)	f _T	3.0	—	MHz
Small–Signal Current Gain (I _C = 0.5 A, V _{CE} = 10 Vdc, f = 1.0 kHz)	h _{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

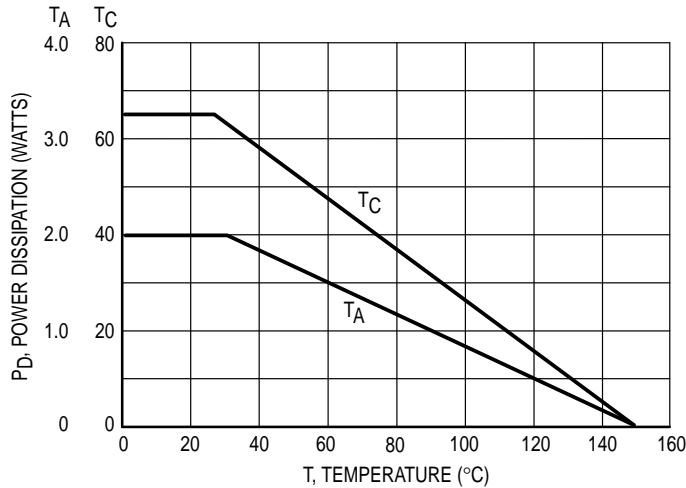


Figure 1. Power Derating

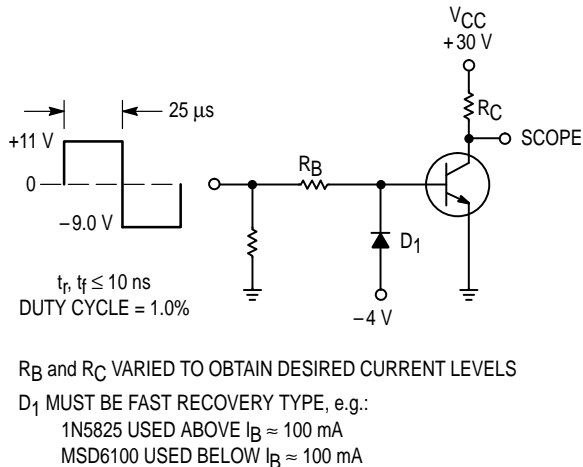


Figure 2. Switching Time Test Circuit

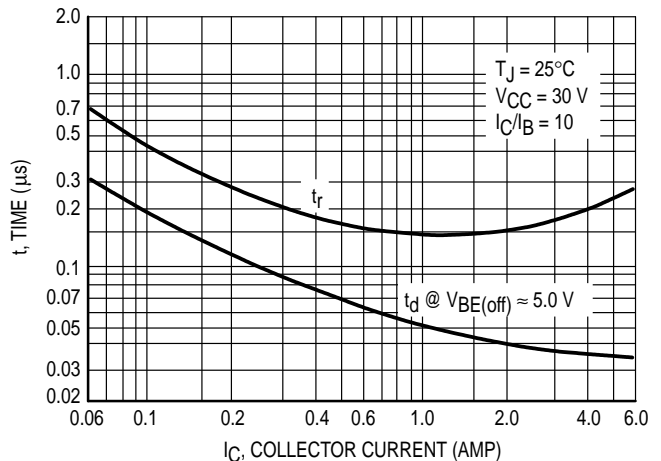


Figure 3. Turn-On Time

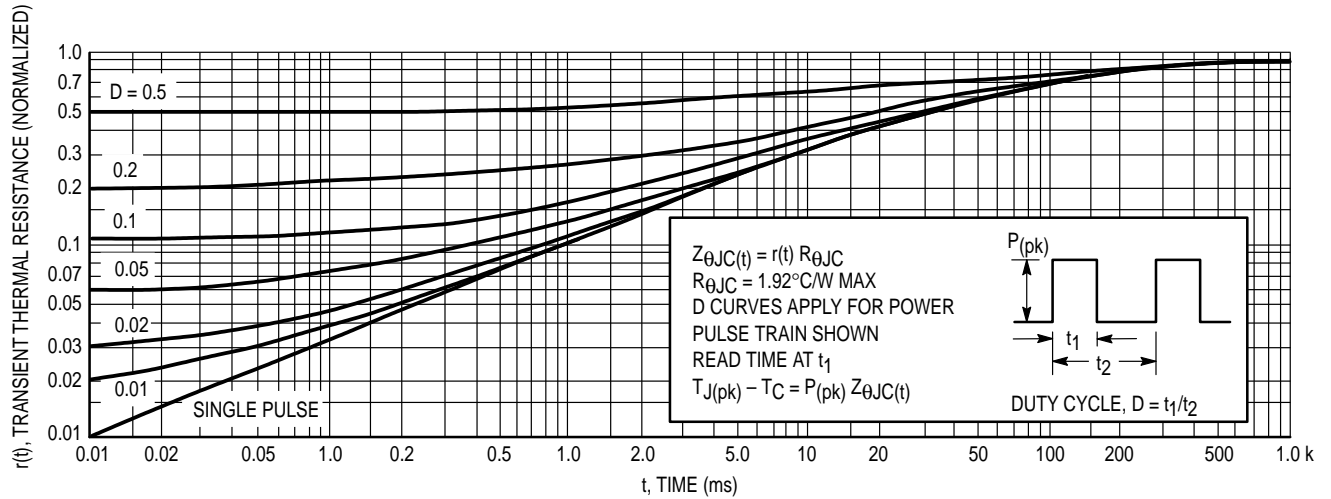


Figure 4. Thermal Response

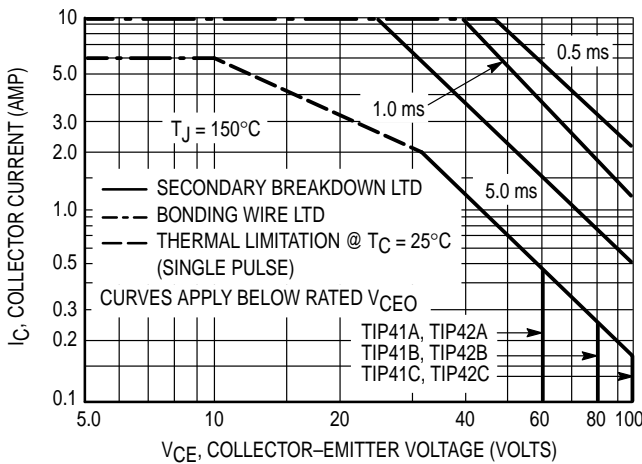


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_J(p_k) = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(p_k) \leq 150^{\circ}\text{C}$. $T_J(p_k)$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

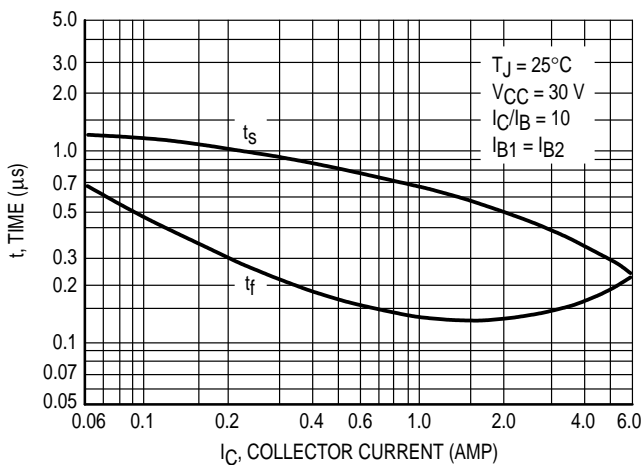


Figure 6. Turn-Off Time

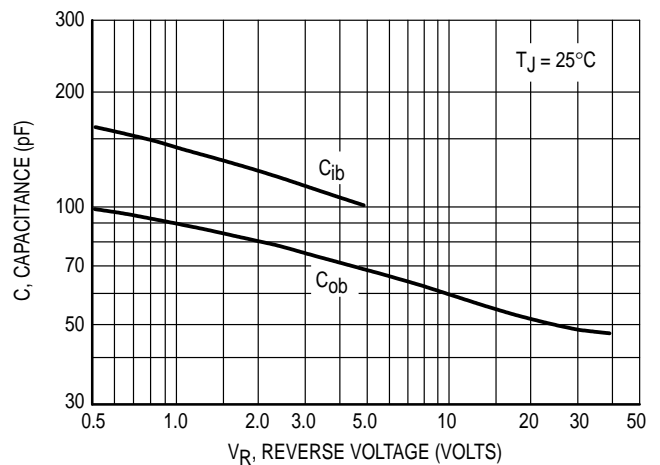


Figure 7. Capacitance

TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

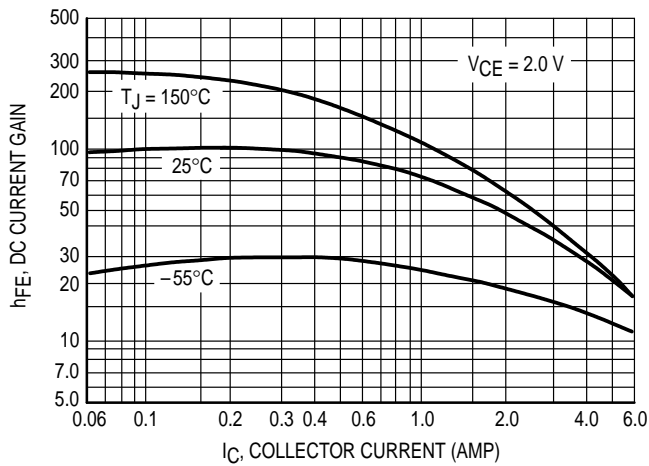


Figure 8. DC Current Gain

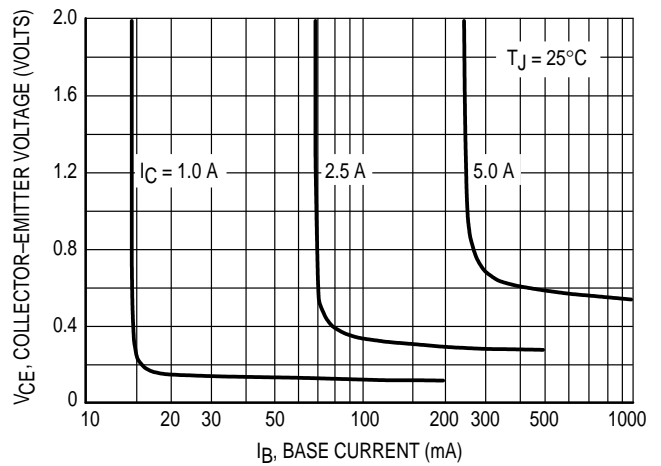


Figure 9. Collector Saturation Region

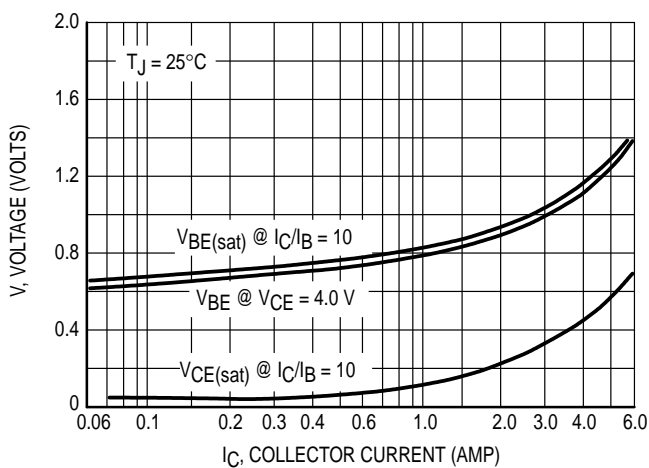


Figure 10. "On" Voltages

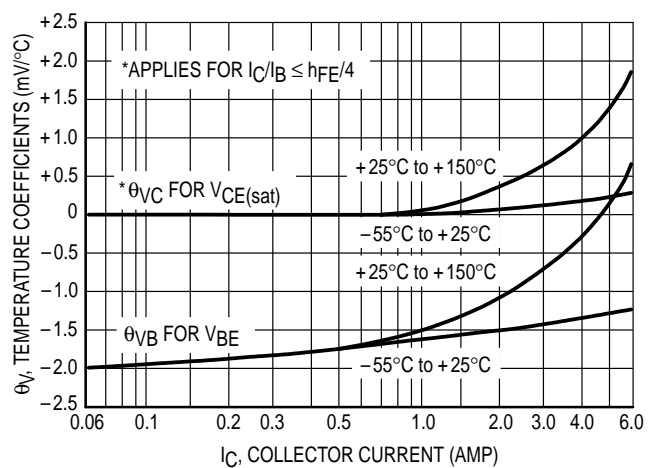


Figure 11. Temperature Coefficients

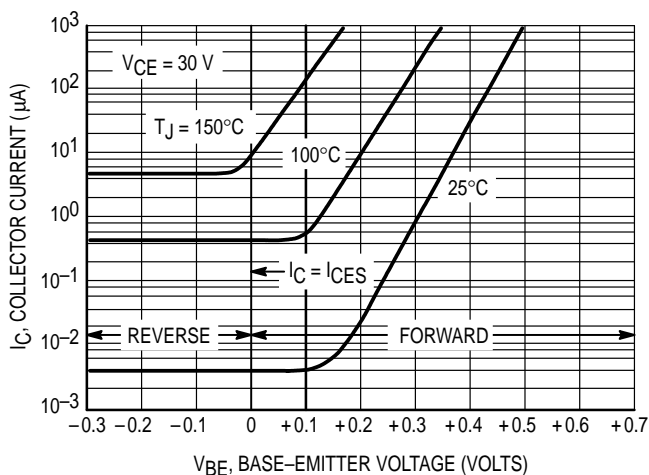


Figure 12. Collector Cut-Off Region

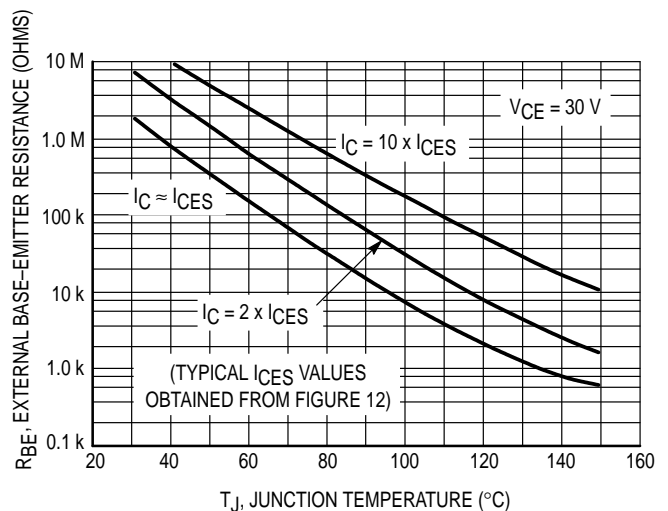
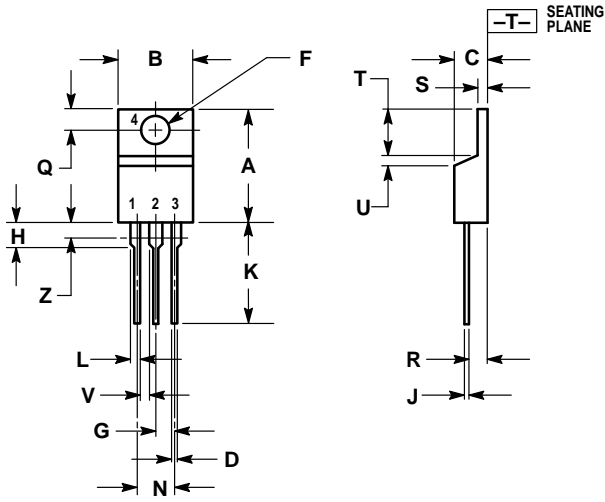


Figure 13. Effects of Base-Emitter Resistance

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 221A-06
 TO-220AB
 ISSUE Y

TIP41A TIP41B TIP41C TIP42A TIP42B TIP42C

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TIP41A/D

