FAIRCHILD
SEMICONDUCTOR®

FDJ1027P

## P-Channel 1.8V Specified PowerTrench® MOSFET

General Description

This dual P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. Packaged in FLMP SC75, the $R_{DS(ON)}$ and thermal properties of the device are optimized for battery power management applications.

Applications

• Battery management/Charger Application
• Load switch

Features

• −2.8 A, −20 V $R_{DS(ON)}$ = 160 mΩ @ V_{GS} = −4.5 V
  $R_{DS(ON)}$ = 230 mΩ @ V_{GS} = −2.5 V
  $R_{DS(ON)}$ = 390 mΩ @ V_{GS} = −1.8 V

• Low gate charge, High Power and Current handling capability

• High performance trench technology for extremely low $R_{DS(ON)}$

• FLMP SC75 package: Enhanced thermal performance in industry-standard package size

Bottom Drain Contact
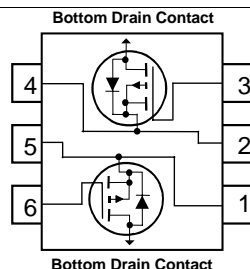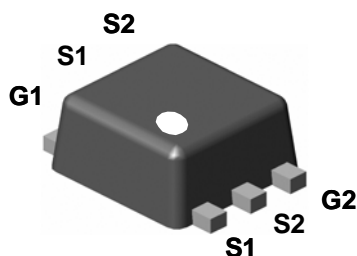
MOSFET Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current – Continuous	(Note 1a)	−2.8	A
	– Pulsed		−12	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.5	
		(Note 1b)	0.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{θJA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	80	°C/W
$R_{θJC}$	Thermal Resistance, Junction-to-Case		5	

Package Marking and Ordering Information

.G	FDJ1027P	7"	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source BreakdownVoltage	V_{GS} = 0 V, I_D = −250 μA	−20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = − 250 μA, Referenced to 25°C		−13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V			−1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−0.4	−0.8	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = −4.5 V, I_D = −2.8 A V_{GS} = −2.5 V, I_D = −2.2 A V_{GS} = −1.8 V, I_D = −1.7 A V_{GS} = −4.5 V,I_D = −2.8 A,T_J=125°C		108 163 283 150	160 230 390 238	mΩ
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −2.8 A		5		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz		290		pF
C_{oss}	Output Capacitance			55		pF
C_{rss}	Reverse Transfer Capacitance			29		pF
Rg	Gate Resistance	V_{GS} = 15 mV f = 1.0 MHz		18		mΩ
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = −10 V, I_D = −1 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			13	23	ns
t_f	Turn–Off Fall Time			18	32	ns
Q_g	Total Gate Charge	V_{DS} = −10 V, I_D = −2.8 A, V_{GS} = −4.5 V		3	4	nC
Q_{gs}	Gate–Source Charge			0.65		nC
Q_{gd}	Gate–Drain Charge			0.75		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				−1.25	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −1.25 A (Note 2)		−0.8	−1.2	V
trr	Diode Reverse Recovery Time	I_F = −2.8 A, d_{iF}/d_t = 100 A/μs		14		ns
Qrr	Diode Reverse Recovery Charge			4		nC

Electrical Characteristics

T_A = 25°C unless otherwise noted

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 80°C/W when mounted on a 1in^2 pad of 2 oz copper (Single Operation).

b) 140°C/W when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Dimensional Outline and Pad Layout

DRAIN

PKG ℄

(0.24)

(0.18)

1   3

0.30
0.20

PKG ℄

(0.73)

(0.46)

(0.50)

DRAIN 1   6   4   DRAIN 2

<u>BOTTOM VIEW</u>

1.70
1.50   [A]

PKG ℄

6   4   [B]

PKG ℄

1.75
1.55

1   3

(0.20)

0.275
0.125

[0.50]

⊕ 0.075Ⓜ A B

[1.00]

**Top
View**

PKG ℄

0.80
0.65

SEATING
PLANE

PKG

PKG ℄

0.225
0.075

1.075
0.925

2.15
1.85

PKG ℄

0.30 MIN

DRAIN 1
TERMINAL

6   4

0.20

0.84

PKG ℄

2.35 MIN

1.35

0.60

0.50 MIN

1   3   DRAIN 2
TERMINAL

0.50

1.00

LAND PATTERN RECOMMENDATION

Typical Characteristics
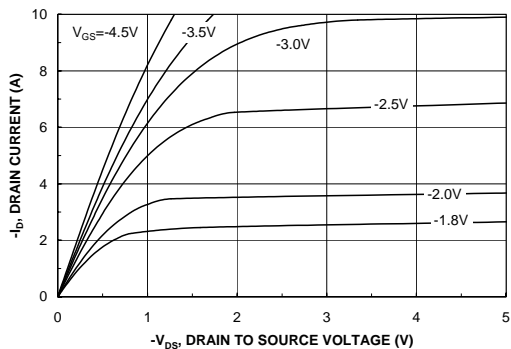
Figure 1. On-Region Characteristics.
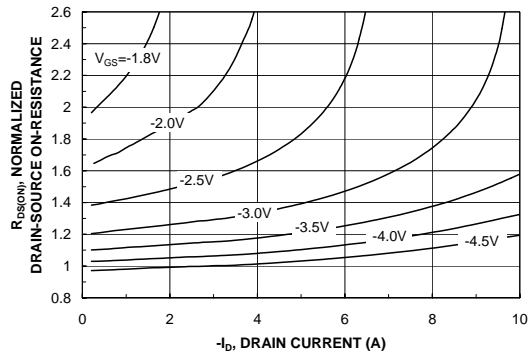
Figure 2. On-Resistance Variation with
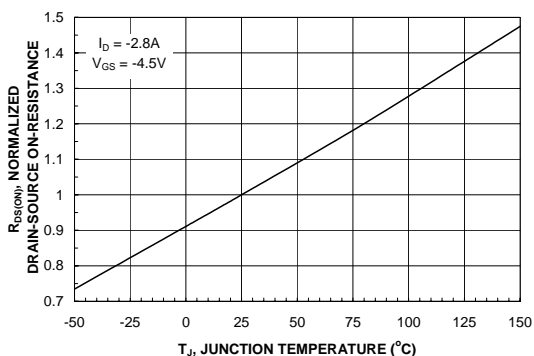Drain Current and Gate Voltage.

Figure 3. On-Resistance Variation with
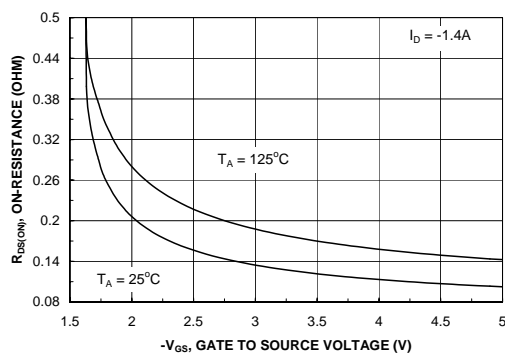Temperature.
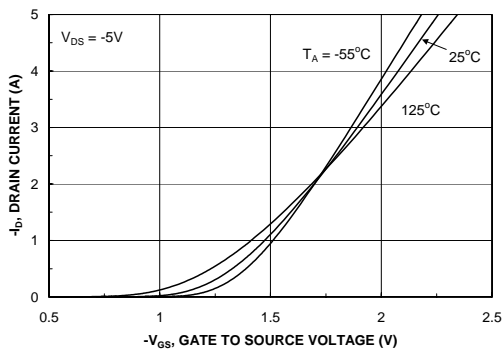

Figure 4. On-Resistance Variation with
Gate-to-Source Voltage.
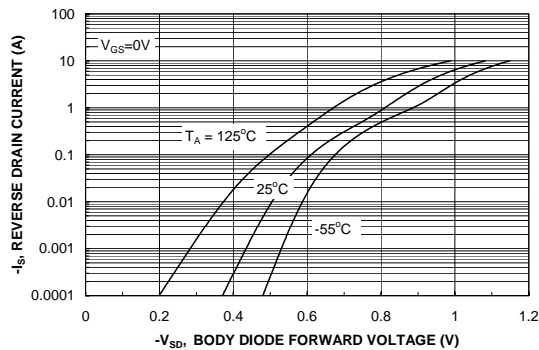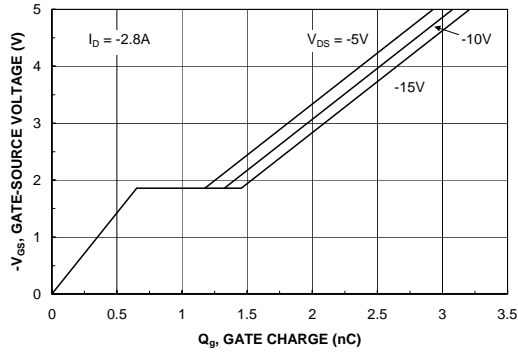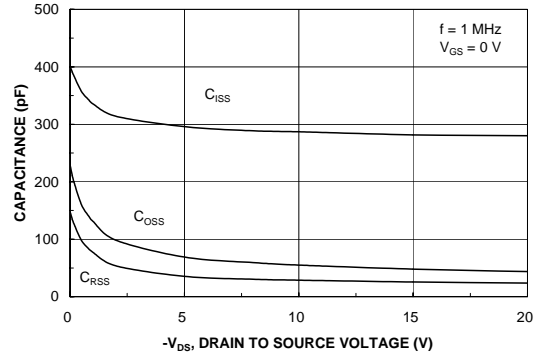

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation
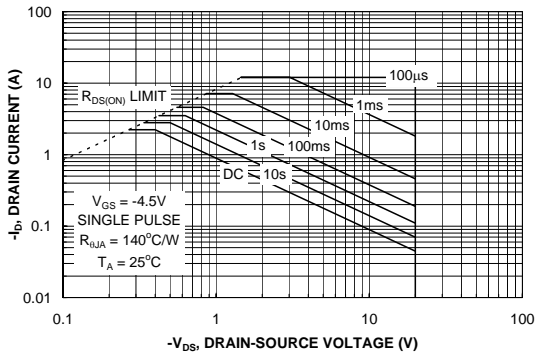with Source Current and Temperature.
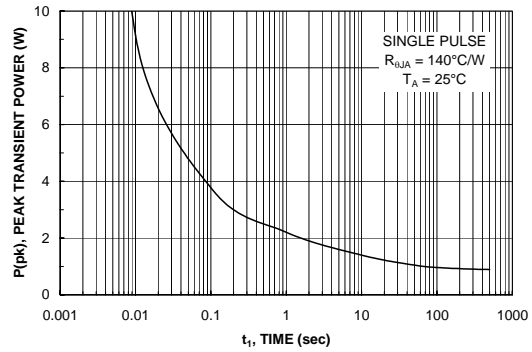
Typical Characteristics

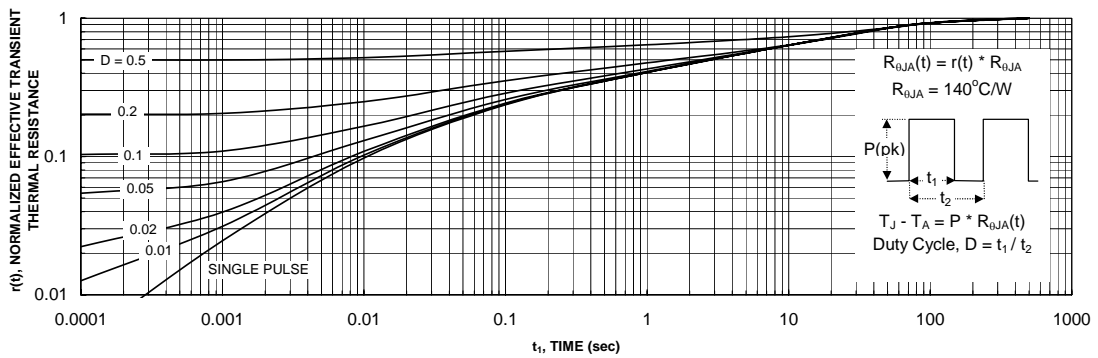**Figure 7. Gate Charge Characteristics.**

Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.

**Figure 10. Single Pulse Maximum
Power Dissipation.**

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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FACT Quiet Series™		OPTOLOGIC®	μSerDes™	UltraFET®
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