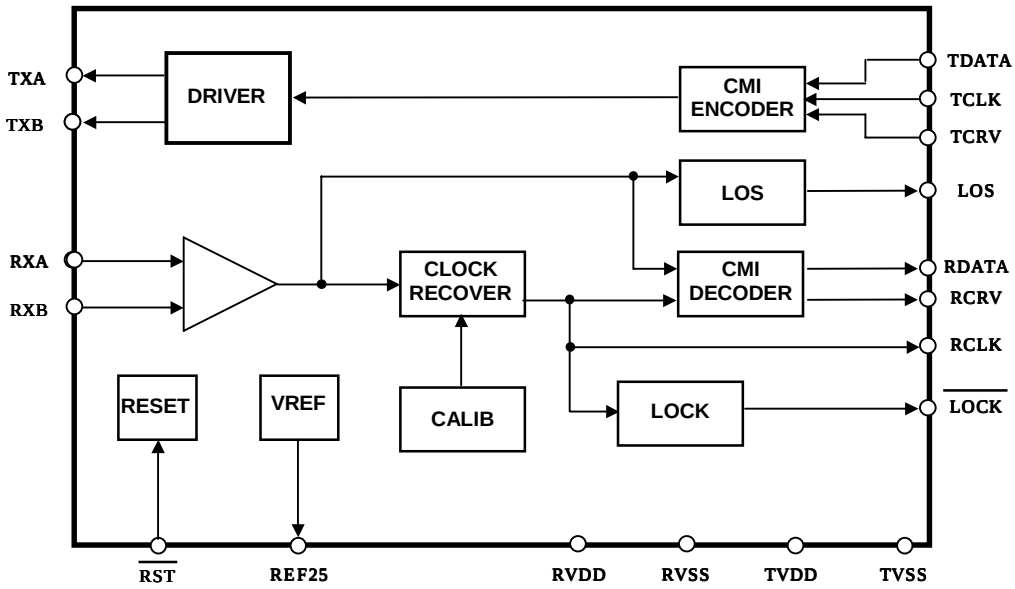
AK2048D

2M CMI Transceiver

FEATURES

- 2.048Mbps CMI Interface
- CLOCK & DATA Recovery function
- Loss of Lock Detection
- Loss of Signal Detection
- Transmitter Pulse Shape
- Single 5.0V±5% Operation
- Low Power Consumption: 400mW (TYP)
- Package: 44pin QFP

BLOCK DIAGRAM



2M CMI Transceiver Block Diagram

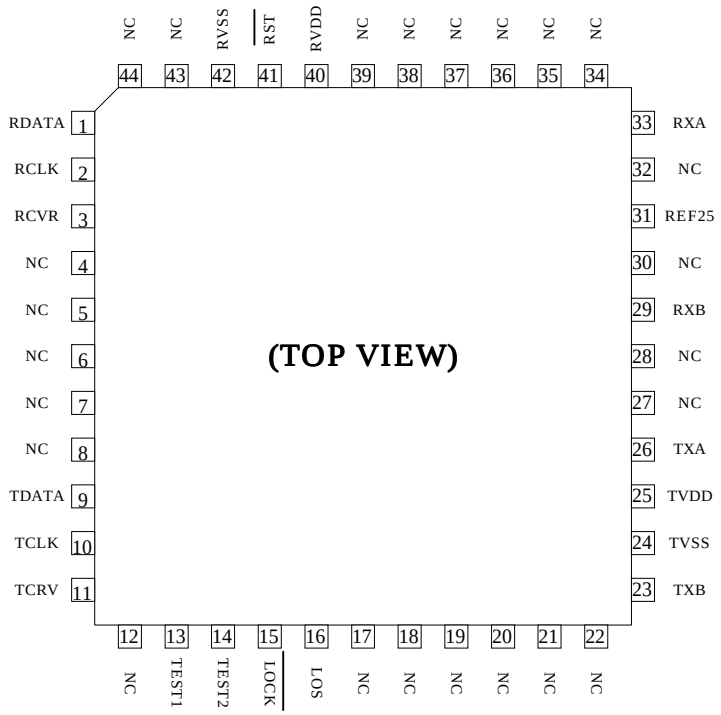
GENERAL DESCRIPTIONS

AK2048D is the 2.048Mbps CMI interface CMOS LSI for CMI interface card. It includes Clock and Data Recovery, Line Driver, LOS Detector, etc.

Build in PLL clock recovery circuit eliminates the correlation of the frequency deviation due to the uneven quality of the devices and a secular change.

PIN ASSIGNMENTS

44pin QFP



PIN ASSIGNMENTS

Pin No.	Pin Name	I/O	Type	AC Load (MAX)	DC Load (MIN)	Comment
1	RDATA	O	TTL	≤15pF	≥4kΩ	
2	RCLK	O	TTL	≤15pF	≥4kΩ	
3	RCRV	O	TTL	≤15pF	≥4kΩ	
9	TDATA	I	TTL			
10	TCLK	I	TTL			
11	TCRV	I	TTL			
13	TEST1	-				*2)
14	TEST2	-				*2)
15	$\overline{\text{LOCK}}$	O	TTL	≤15pF	≥4kΩ	
16	LOS	O	TTL	≤15pF	≥4kΩ	
23	TXB	O	Analog	≤15pF		*1)
24	TVSS	-				
25	TVDD	-				
26	TXA	O	Analog	≤15pF		*1)
29	RXB	I	Analog			
31	REF25	O	Analog	1μF(typ)		
33	RXA	I	Analog			
40	RVDD	-				
41	$\overline{\text{RST}}$	I	TTL			Pulled up to VDD by the internal register (50KΩmin)
42	RVSS	-				

The other pins (4-8,12,17-22,27,28,30,32,34-39,43,44) are NC pins.

NC pins are recommended to connect to VSS to avoid noise problem.

*1) TXA, TXB can drive 110Ω connected between these pins.

*2) Must be open.

PIN DESCRIPTIONS

Pin Name	I/O	Function
RDATA	O	Receive Data output recovered from the incoming data. Delay time from the incoming data to the RDATA is about 1.25bit. Output on the rising edge of RCLK.
RCLK	O	Receive Clock Output recovered from the incoming data.
RCRV	O	CRV (Code Rule Violation) output pin. When AK2048D detects the CRV of CMI codes from in the coming data, RCRV goes to "high" synchronized with the violation data. CRV is detected for both "0" data and "1" data. Refer to Fig.6, 11
TDATA	I	Transmit Data Input pin. Input on the falling edge of TCLK.
TCLK	I	Transmit Clock Input pin.
TCRV	I	If this input is "high", AK2048D generates CRV in the transmit data. CRV is generated for both "0"data and "1"data. "High" input TCRV is accepted until 5 clocks duration. If the duration of "High" input is longer than 6 clocks, TCRV input after 6th clock is ignored. Refer to Fig.4, 11
TEST1	NC	Test pin. Should be floated.
TEST2	NC	Test pin. Should be floated.
$\overline{\text{LOCK}}$	O	$\overline{\text{LOCK}}$ indicates the PLL status whether PLL is in the LOCK status or PLL is in the UNLOCK status. ***$\overline{\text{LOCK}}$ status*** $\overline{\text{LOCK}}$ becomes "Low" when the sampled RCLK are all "Low" during the consecutive 32 RXA-RXB sample clock duration. ***UN $\overline{\text{LOCK}}$ status*** $\overline{\text{LOCK}}$ becomes "High" when the following both conditions are satisfied. - The sampled RCLK are "High" more than 5 clocks in the frame of the consecutive 256 RXA-RXB clock duration. - And the above happens in the 5 consecutive frames. In another condition, $\overline{\text{LOCK}}$ keeps the current output status without change. The output timing of this signal is asynchronous with RCLK. When RST is "Low", $\overline{\text{LOCK}}$ is fixed to "High".

Pin Name	I/O	Function
LOS	O	LOS goes High within 12usec after AK2048D detects that the amplitude of the RXB input signal is lower than 135mVpp(typ). Output on the rising edge of RCLK.
TXB	O	Transmit CMI signal output. TXA is to CMI+, and TXB is corresponds to CMI-. Delay time from TDATA to TXB is about 1bit.
TVSS	-	Negative power supply 0V
TVDD	-	Positive power supply 5V
TXA	O	Transmit CMI signal output. TXA is to CMI+, and TXB is corresponds to CMI-. Delay time from TDATA to TXA is about 1bit.
RXB	I	Receive CMI signal input. RXA is to CMI+, and RXB is corresponds to CMI-.
REF25	O	Output reference voltage (about 2.5V) in order to decide middle point of input signal (RXA-RXB). Connected to middle point of the external equalizer.
RXA	I	Receive CMI signal input. RXA is to CMI+, and RXB is corresponds to CMI-.
RVDD	-	Positive power supply. 5V
$\overline{\text{RST}}$	O	"Low" input reset the calibration circuit and forces $\overline{\text{LOCK}}$ output "High" and TXA-TXB output "High-Z". When this input rise, PLL calibration restarts. Please set open or connect to VDD when not using.
RVSS	-	Negative power supply 0V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Units	Conditions
DC Supply	DVDD TVDD	-0.3		6.0	V	
Input Voltage	V_{IN}	RVSS-0.3		RVDD+0.3	V	
Input Current 1	I_{IN1}			10	mA	*1)
Input Current 2 (TXA, TXB, RXA, RXB)	I_{IN2}			200	mA	
Storage Temperature	Tstg	-65		150	°C	

*1) Except for TXA, TXB, RXA, RXB

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Unit	Conditions
DC Supply	RVDD TVDD	4.75	5.0	5.25	V	TVDD<RVDD+0.3V
Ambient Operating Temperature	Ta	0	25	+80	°C	
Power Consumption	PD1(RVDD)		150	300	mW	
	PD2(TVDD)		250	300	mW	110Ω LOAD

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Condition: VDD=5.0V±5%, VSS=0V,Ta=0~80°C

Parameter	Symbol	min	typ	max	Unit	Conditions
Digital High-level input voltage	V_{IH}	2.4			V	
Digital Low-level input voltage	V_{IL}			0.8	V	
Digital High-Level output voltage	V_{OH}	2.4			V	I_{OUT}=-40μA *1)
Digital Low-level output voltage	V_{OL}			0.5	V	I_{OUT}=1.6mA *1)
Input leak current 1				10	μA	Without $\overline{RST}$, TEST1
Input leak current 2				100	μA	$\overline{RST}$, TEST1

*1) When CMOS load is connected, output CMOS logic level.

TRANSMITTER

Parameter	Symbol	min	typ	max	Unit	Comments
Output signal level	Va	2.55	3.3	3.90	Vp-p	Refer to Fig.1, 2
	VpeakH			4.05		
	VpeakL	2.55				
Rise/Fall Time	Tr, Tf		20	50	ns	Refer to Fig.1, 2
Pulse duty of transmit output		43	50	57	%	*1), *2) Refer to Fig.3
Delay time from TDATA to TXA,TXB	Ttd		1		Bit	*3)Refer to Fig.4

*1) The duty cycle of TCLK 50%±4%.

*2) Duty cycle = Tpwh / (Tpwh + Tpwl) × 100%

*3) Signal output delay = (1bit logical delay) + (internal propagation delay)

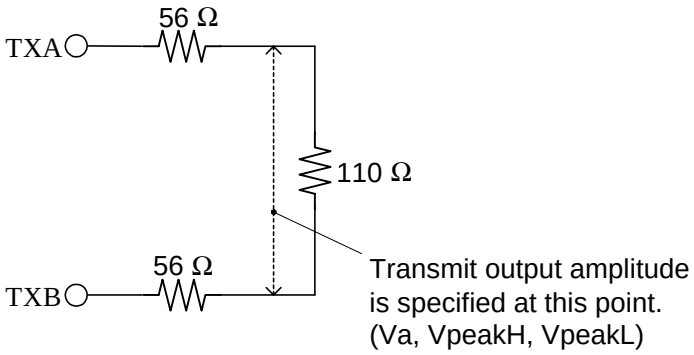


Fig.1 Measurement circuit

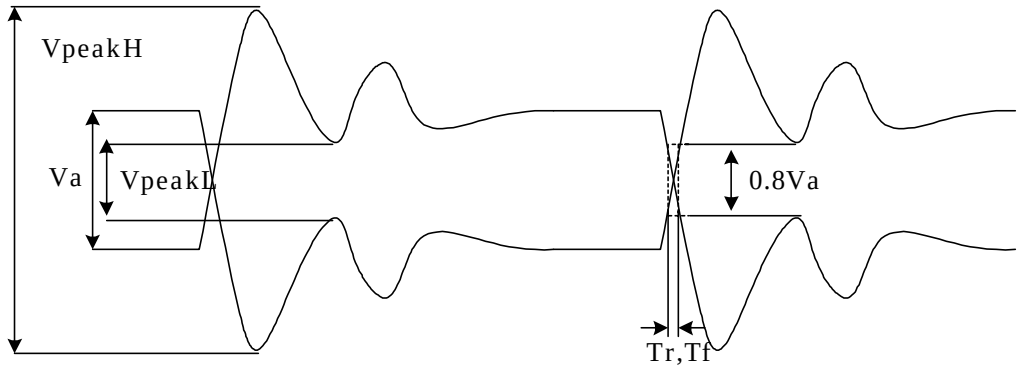


Fig.2 Rise and fall times

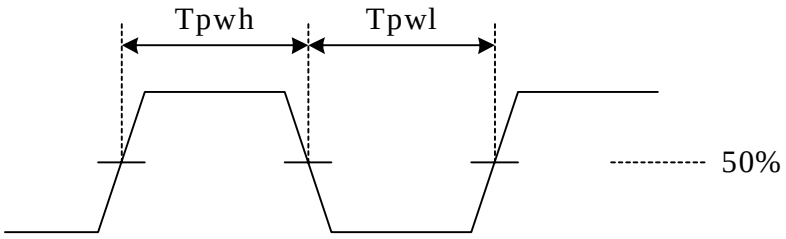


Fig.3 Transmit output pulse duty

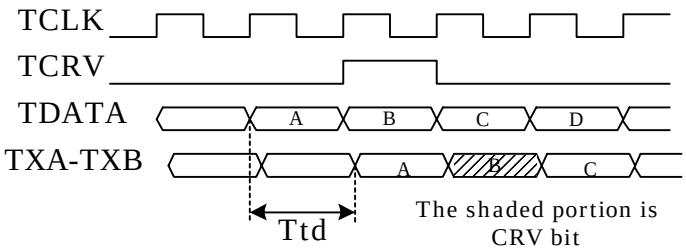


Fig.4 Data input to signal output delay time

RECEIVER

Parameter	Symbol	min	typ	max	Unit	Comments
REF25 output	VREF	2.0	2.5	3.0	V	Iout<IuA *1)
Signal loss threshold level	Vth	85	135	185	mVp-p	RXB terminal
Signal loss detection time	TALM		10	12	usec	Fig.5
Sensitivity		0.2		4.0	Vp-p	
Input jitter tolerance				0.15	UIp-p	Jitter frequency 20KHz~100KHz
PSRR (Line Length 400m)				400	mVp-p	*2)
S/X tolerance Line Length 400m 0m		 2 12			 dB dB	*2) frequency 1.9MHz
Signal input to Data output delay time	Trd		1.25		bit	Fig.6 *3)
RCLK Output Jitter			3		nsp-p	*4)

*1) Reference output of fixed equalizer.

*2) The amplitude of input data is 3.0±0.75Vp-p and the data pattern is 2^{15}-1.

*3) Data output delay = (1.25bit logical delay) + (internal propagation delay)

*4) Data pattern is “all space” with CRV every 8kHz cycle.

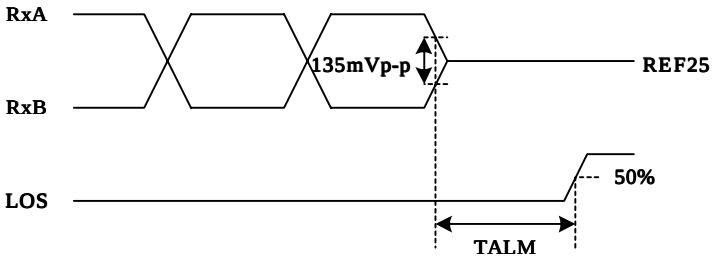


Fig.5 LOS output signal

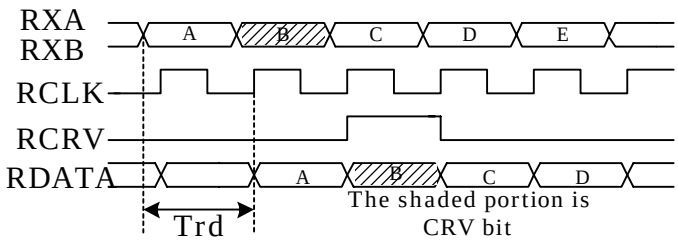


Fig.6 Delay time from RXA,RXB to RDATA

AC CHARACTERISTICS

Parameter	Pin Name	Symbol	min	typ	max	Unit	Conditions
Input Clock Frequency	TCLK	fin		2.048		MHz	
Duty Cycle	TCLK		46	50	54	%	*1) Refer to Fig.7
Delay time from TCLK rising to TDATA, TCRV.	TDATA TCRV	Tpd	-58		58	ns	Refer to Fig.8
Output Clock Frequency	RCLK	fout		2.048		MHz	The bit rate of received signal is 2.048Mbps
Output Clock Duty	RCLK		43	50	57	%	*1) Refer to Fig.7
Delay time from RCLK rising to RDATA, RCRV.	RDATA RCRV	Tpd	-48		48	ns	Refer to Fig.8
Rise/Fall Time	LOS LOCK	Tr, Tf		15	30	ns	Refer to Fig.9
	RDATA RCLK RCRV				15	ns	
Delay time from RCLK rising to LOS	LOS	Tpd	-48		48	ns	Refer to Fig.8

*1) Duty: Tpwh/(Tpwh+Tpwl) × 100%

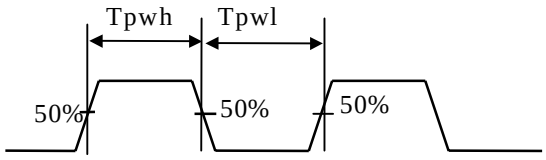


Fig.7 Clock timing

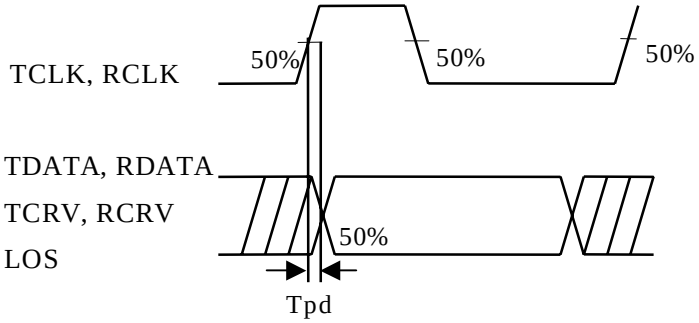


Fig.8 Transmitter Timing

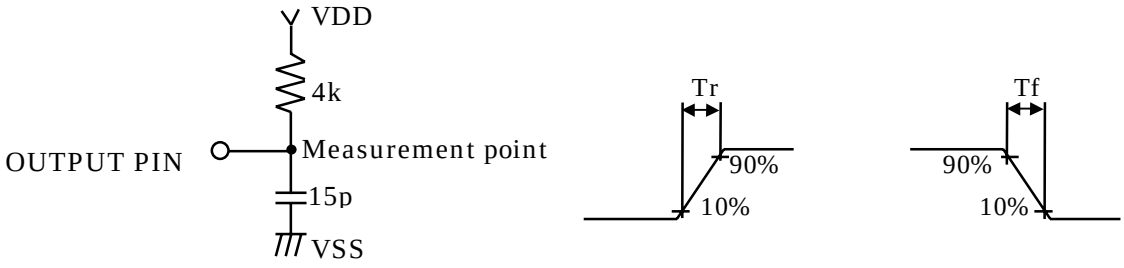


Fig.9 Rise and fall times and a condition of measurement.

FUNCTIONAL DESCRIPTION

PLL calibration function

The calibration of PLL is caused in case of the following 3cases.

(1) Power on

(2) $\overline{\text{RST}}$ rising

(3) $\overline{\text{LOCK}}$ rising

(1) Power on

After the power is on, the calibration is complete and $\overline{\text{LOCK}}$ goes to “Low” in less than 63ms from whichever the later happens, the input of signal (RXA-RXB) or the rising edge of $\overline{\text{RST}}$.

(2) $\overline{\text{RST}}$ rising

The calibration is complete and $\overline{\text{LOCK}}$ goes to “Low” in less than 38ms from whichever the later happens, the input of signal (RXA-RXB) or the rising edge of $\overline{\text{RST}}$.

(3) $\overline{\text{LOCK}}$ rising

When the device falls into unlock by some reasons and $\overline{\text{LOCK}}$ goes to “high”, calibration restarts.
The calibration is complete and $\overline{\text{LOCK}}$ goes to “Low” in less than 38ms from the rising edge of $\overline{\text{LOCK}}$.

PLL pull in time after loss of signal

When LOS goes to “high” by loss of signal after the calibration, the pull in of the PLL restarts by signal input. If the device can pull in without calibration, pull-in completes less than 200us.
In other case, $\overline{\text{LOCK}}$ goes to “high” and calibration restarts less than 2ms.

LOS signal

LOS goes to ”high”, when the amplitude of RXB is less than 135mVpp(typ) during 16 bits (about 8us).
LOS signal goes to “Low”, when amplitude of RXB is more than 135mVpp(typ).

When the signal is lost during the calibration, LOS signal goes to “high” and the calibration circuit is reset. The calibration restarts after LOS signal goes to “Low”.

CRV (Code Rule Violation)

CMI code with violation is called as MD (Modified Dipulse) code. MD is refer to Fig.10. Generally speaking, CRV (Code Rule Violation) is generated at code “1”. But AK2048D generates the violation for not only code “1”, but also code “0”. Violation of code “0” is refer to Fig.11.

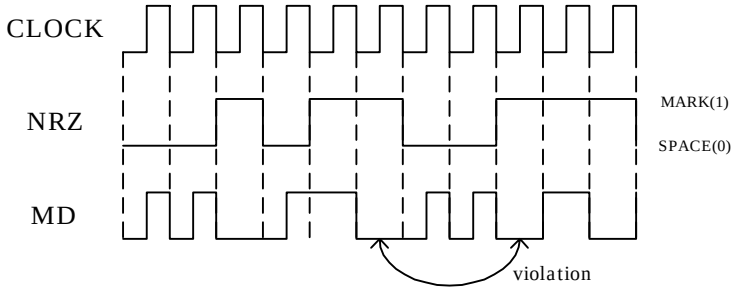


Fig.10 MD code

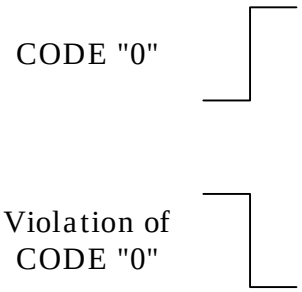


Fig.11 Violation of CODE “0”

RECOMMENDED EXTERNAL CIRCUITS

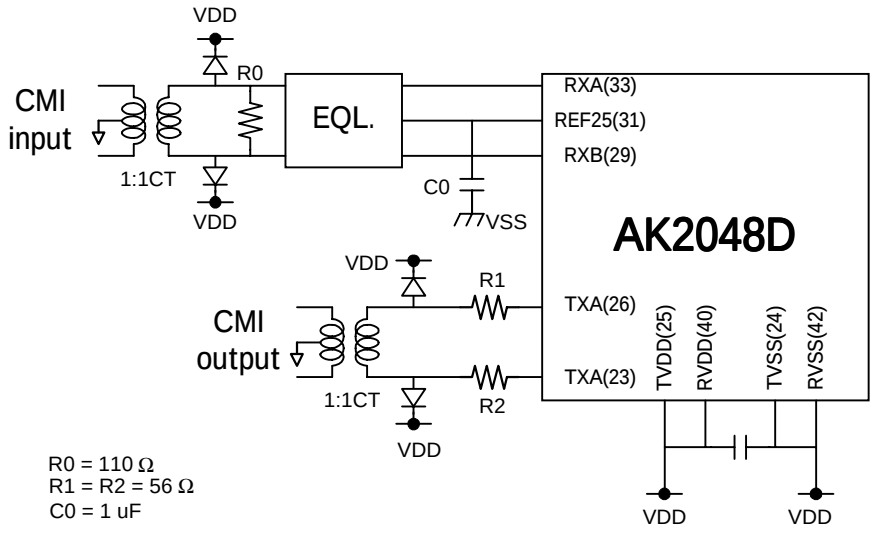
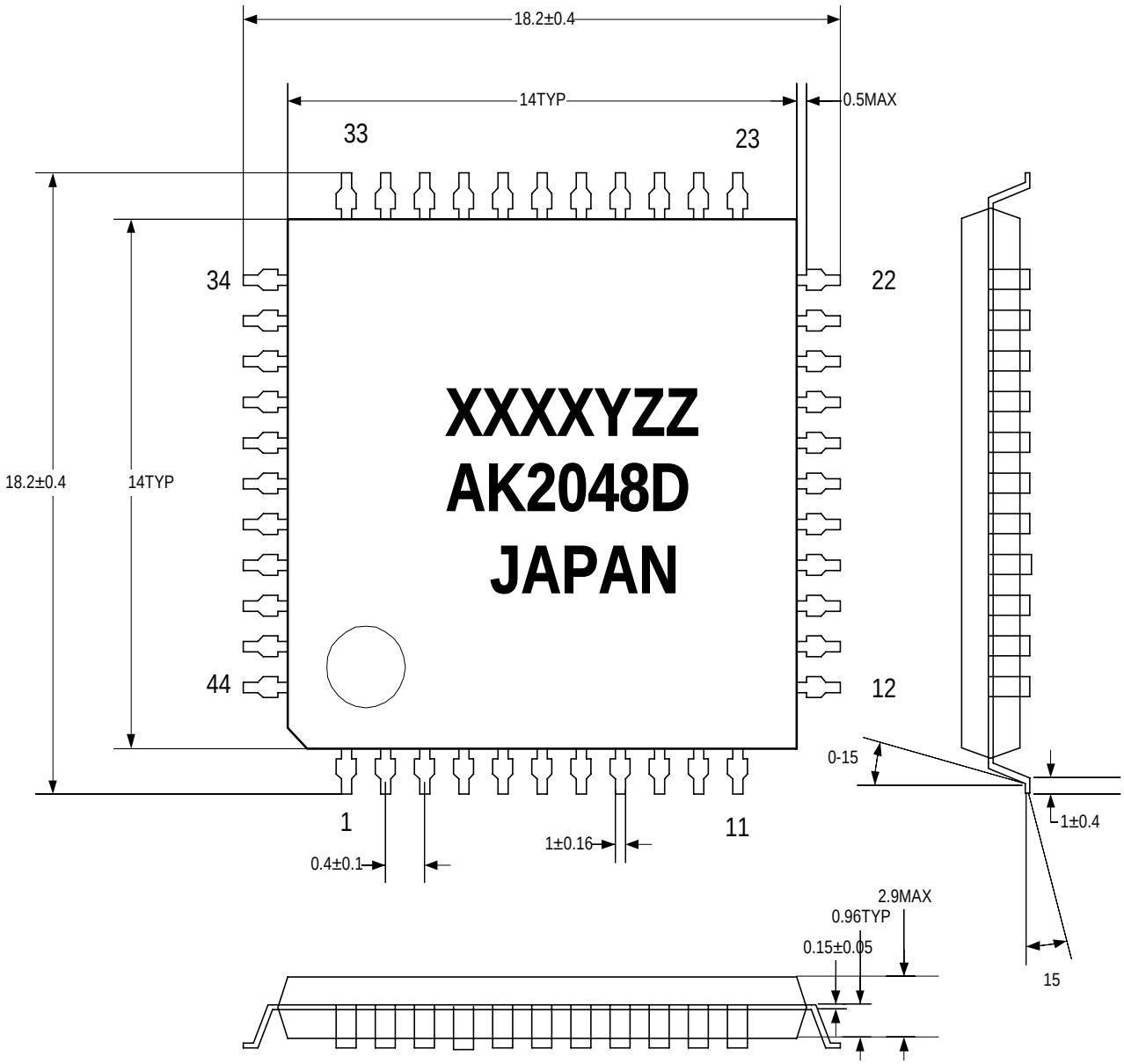


Fig.12 The example of the external circuits

It is recommended that Shott key diode in Fig 12 is connected for protection of latch-up.

PACKAGE


18.2±0.4
14TYP
0.5MAX
33
23
34
22
XXXXYZZ
AK2048D
JAPAN
18.2±0.4
14TYP
44
12
1
11
0.4±0.1
1±0.16
0-15
1±0.4
2.9MAX
0.96TYP
0.15±0.05
15

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