NEC

MOS INTEGRATED CIRCUIT

μPD17P207

4-BIT SINGLE-CHIP MICROCONTROLLER WITH LCD CONTROLLER/DRIVER AND A/D CONVERTER FOR INFRARED REMOTE CONTROL TRANSMITTER

DESCRIPTION

μPD17P207 is a variation of μPD17207 and is equipped with a one-time PROM instead of an internal mask ROM.

μPD17P207 is suitable for evaluating program when developing a μPD17201A and 17207 systems because program can be written by the user.

When reading this document, also refer to the μPD17201A, 17207 documents.

FEATURES

- 17K architecture:
  General-purpose register format
- Pin-compatible with μPD17201A, 17207
  except PROM programming functiom
- Internal one-time PROM: 4096 × 16 bits
- Supply voltage:
  2.5 to 5.5 V (at f_X = 4 MHz, T_A = –20 to +75°C)
  2.4 to 5.5 V (at f_X = 4 MHz, T_A = –20 to +60°C)
  2.0 to 5.5 V (at f_{XT} = 32.768 kHz, T_A = –20 to +75°C)

ORDERING INFORMATION

Part Number	Package
μPD17P207GF-001-3B9	80-pin plastic QFP (14 × 20 mm)
μPD17P207GF-002-3B9	80-pin plastic QFP (14 × 20 mm)
μPD17P207GF-003-3B9	80-pin plastic QFP (14 × 20 mm)

The features of each product is shown in the following table:

When using μPD17P207-001, be sure to connect the resonator to the main clock oscllator circuit and subclock oscillator circuit.

Item	μPD17P207-001	μPD17P207-002	μPD17P207-003	μPD17201A, 17207
Pull-up resistor of $\overline{\text{RESET}}$ pin	Provided	Not provided	Not provided	On request (mask option)
Main clock oscillator circuit		Provided		
Subclock oscillator circuit		Not provided	Provided	

μPD17P207 is different from μPD17201A, 17207 in some of the electrical characteristics, such as supply voltage, the operating ambient temperature, and supply current. Therefore, use μPD17P207 only for the system evaluation.

The information in this document is subject to change without notice.

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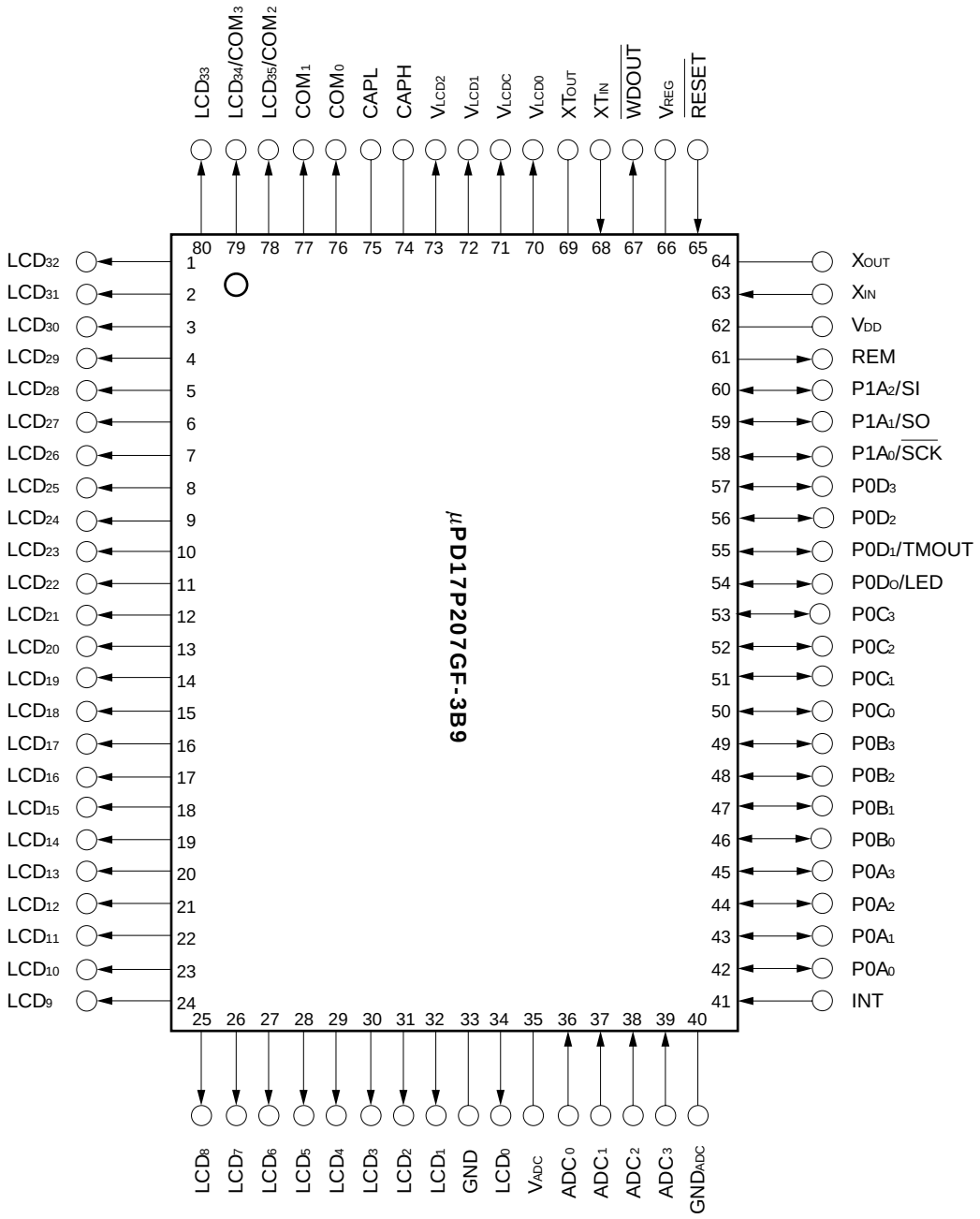
Date Published November 1996 P
Printed in Japan

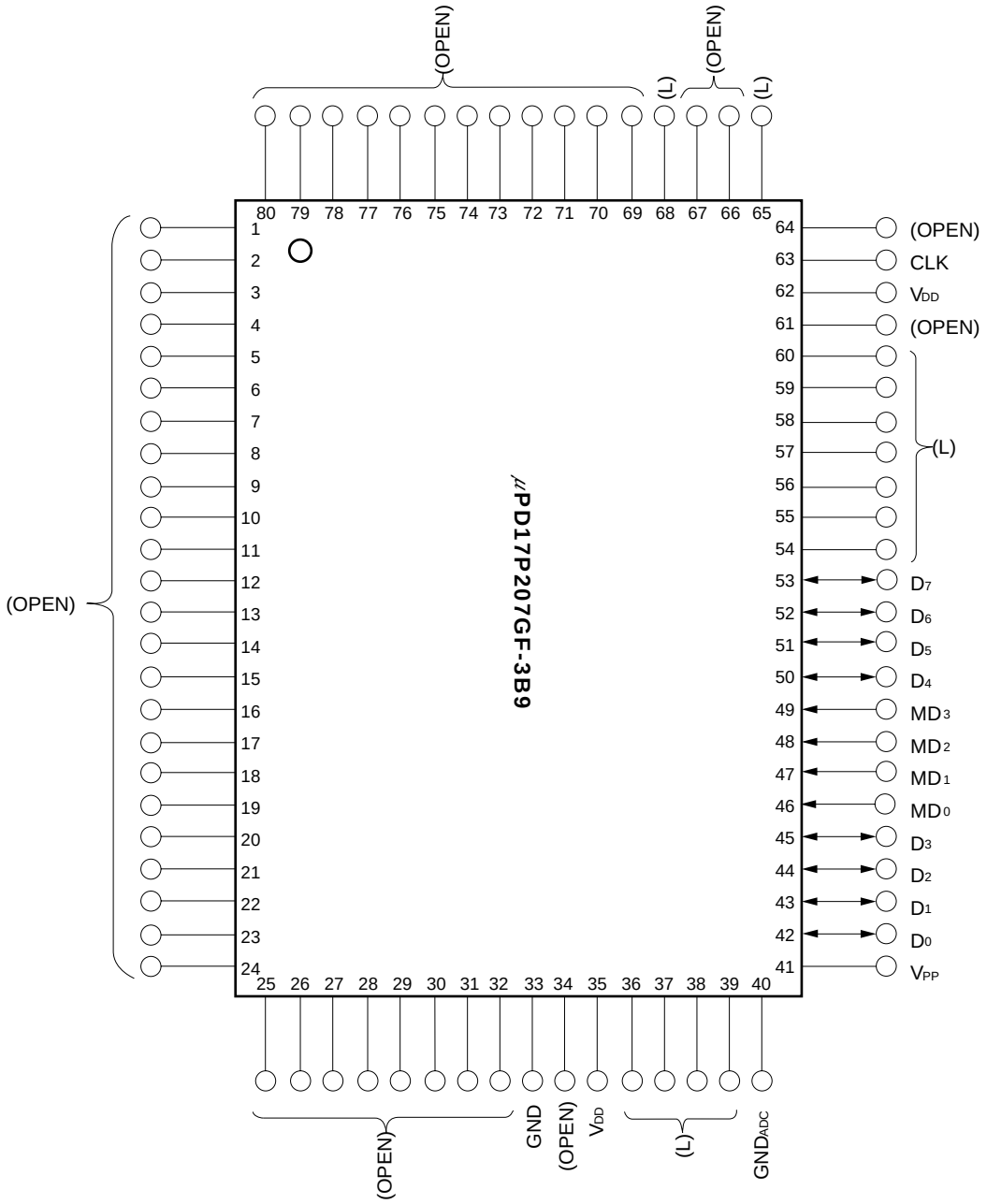
The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

(1) Ordinary operation mode



(2) PROM programming mode



Caution: Those enclosed in parentheses indicate the processing of the pins not used in PROM programming mode.

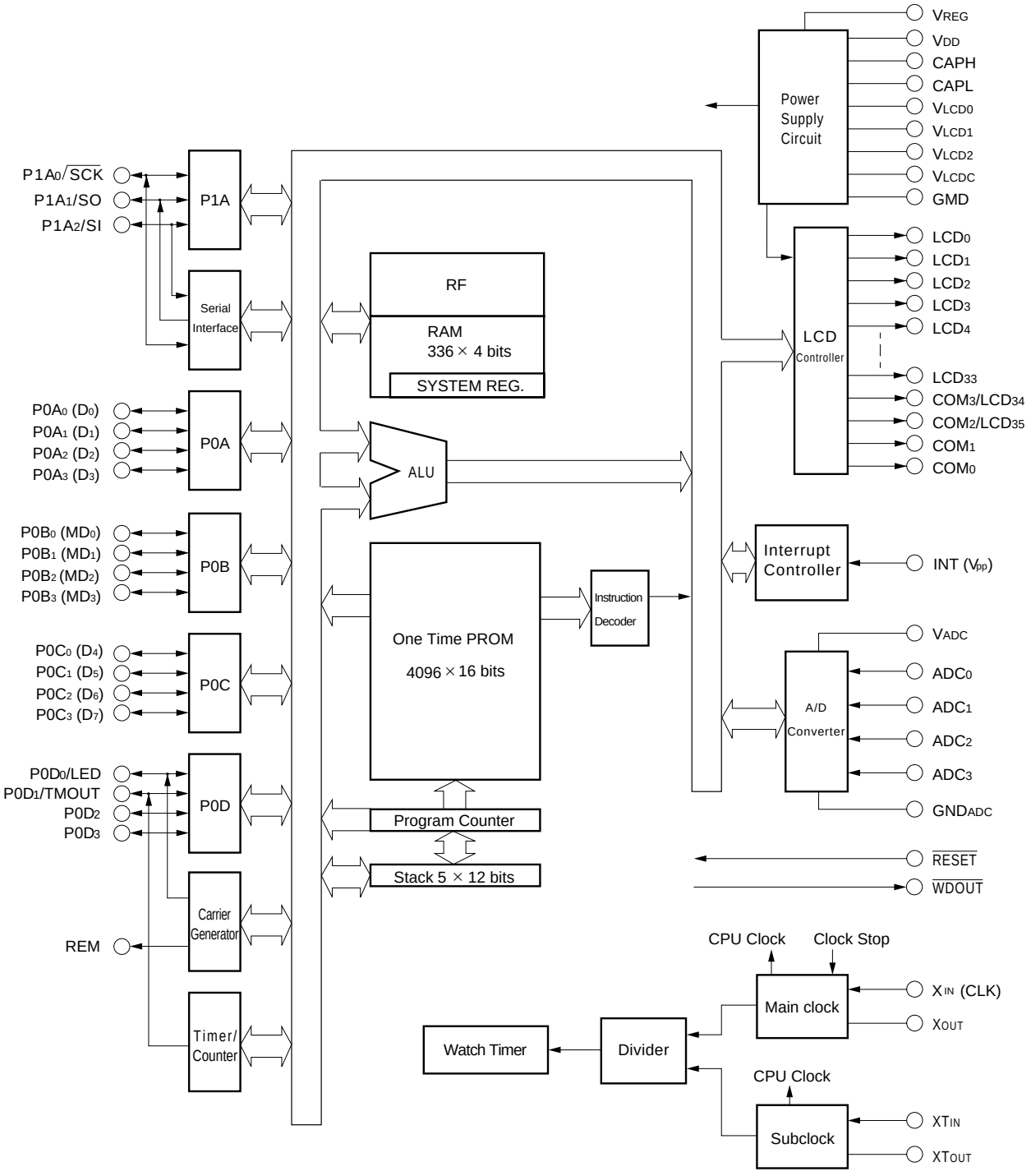
L : Ground these pins through a resistor (470 Ω).

Open : Do not connect anything to these pins.

Pin Name

ADC_0-ADC_3	:	A/D converter input
CAPH, CAPL	:	Booster capacitor connection
CLK	:	PROM clock input
COM_0-COM_3	:	LCD common signal output
D_0-D_7	:	PROM data I/O
GND, GND_{ADC}	:	Ground
INT	:	External interrupt request signal input
LCD_0-LCD_{35}	:	LCD segment signal output
LED	:	Remote controller transfer display output
MD_0-MD_3	:	PROM mode selection input
$P0A_0$-$P0A_3$	:	I/O port
$P0B_0$-$P0B_3$	:	I/O port
$P0C_0$-$P0C_3$	:	I/O port
$P0D_0$-$P0D_3$	:	I/O port
REM	:	Remote controller transfer output
$\overline{RESET}$	:	Reset signal input
$\overline{SCK}$	:	Serial clock I/O
SI	:	Serial data input
SO	:	Serial data output
TMOUT	:	Timer output
V_{ADC}	:	A/D converter power supply
V_{DD}	:	Power supply
V_{LCD0}-V_{LCD2}	:	LCD drive voltage output
V_{LCDC}	:	LCD drive reference voltage adjustment
V_{PP}	:	PROM writing power supply
V_{REG}	:	Voltage regulator output
$\overline{WDOUT}$	:	Overrun detection output
X_{IN}, X_{OUT}	:	Main clock oscillator circuit
XT_{IN}, XT_{OUT}	:	Subclock oscillator circuit

BLOCK DIAGRAM



Remark Inside the parenthesis indicates pin names in the PROM programming mode.

CONTENTS

1. PIN FUNCTIONS

1.1 ORDINARY OPERATION MODE

Pin No.	Symbol	Function	Output Type	On Reset
76 77 78 79 80 1 | 32 34	COM_0 COM_1 LCD_{35}/COM_2 LCD_{34}/COM_3 LCD_{33} LCD_{32} | LCD_1 LCD_0	Common/segment signal outputs of the LCD driver. These common and segment signal outputs are selected by LCDMD3 to LCDMD0 of the register file. • COM_0 to COM_3 · Common signal outputs of the LCD driver • LCD_{35} to LCD_0 · Segment signal outputs of the LCD driver	CMOS, push-pull	–
33	GND	Device ground	–	–
35	V_{ADC}	Positive power supply of the A/D converter (V_{ADC} should be equal to V_{DD}.)	–	–
36 | 39	ADC_0 | ADC_3	Analog inputs of the A/D converter (8-bit resolution)	–	–
40	GND_{ADC}	Ground of the A/D converter	–	–
41	INT	External interrupt request signal (Input). The interrupt request is generated at the rising edge of this signal.	–	Input
42 | 45	$P0A_0$ | $P0A_3$	4-bit I/O port (enabling setting of inputs or outputs in 4-bit units) (Grouped I/O). Each of these pins has a pull-up resistor.	CMOS, push-pull	Input
46 | 49	$P0B_0$ | $P0B_3$	4-bit I/O port (enabling setting of inputs or outputs in 4-bit units) (Grouped I/O).	N-channel, open-drain	Input
50 | 53	$P0C_0$ | $P0C_3$	4-bit I/O port (enabling setting of inputs or outputs in 4-bit units) (Grouped I/O).	N-channel, open-drain	Input
54 55 56 57	$P0D_0$/LED $P0D_1$/TMOUT $P0D_2$ $P0D_3$	Port 0D/LED output or 8-bit timer output. $P0D_0$ and LED outputs are switched by NRZEN of the register file. $P0D_1$ and 8-bit timer outputs are switched by TMOE of the register file. • $P0D_0$ to $P0D_3$ · 4-bit I/O port · Enabling setting of inputs or outputs of each bit (Bitwise I/O) • LED · Outputs NRZ signal in synchronization with infrared remote controller signal (REM) · Outputs high level while remote controller carrier is output from REM pin • TMOUT · Output of the 8-bit timer	CMOS, push-pull	Input

(to be cont'd)

(cont'd)

Pin No.	Symbol	Function	Output Type	On Reset
58 59 60	P1A0/$\overline{SCK}$ P1A1/SO P1A2/SI	Port 1A or serial interface. Port 1A and serial interface are switched by SIOEN of the register file. • P1A0 to P1A2 · 3-bit I/O port · Enabling setting of inputs or outputs of 3 bits (Grouped I/O) • $\overline{SCK}$, SO, SI · $\overline{SCK}$: Serial clock I/O · SO: Serial data output · SI: Serial data input	CMOS, push-pull	Input
61	REM	Signal output to an infrared remote controller. Active-high output	CMOS, push-pull	Low-level output
62	V_{DD}	Positive power supply.	–	–
63 64	X_{IN} X_{OUT}	These pins are connected to a 4-MHz ceramic or crystal resonator for main clock oscillation.		(Oscillation stops.)
65	$\overline{RESET}$	System reset input System is reset when low level is input to this pin. While this pin is low, oscillation of main clock is stopped. Only μPD17P207-001 has internal pull-up resistor.	–	Input
66	V_{REG}	Output of the voltage regulator for the subclock oscillation circuit. Connect external 0.1-μF capacitor to this pin.	–	–
67	$\overline{WDOUT}$	Output for detection of a program overrun. Outputs low level when the watchdog timer overflows or the stack overflows/underflows. Use this pin after connecting to the $\overline{RESET}$ pin.	N-channel, open drain	High-impedance
68 69	XT_{IN} XT_{OUT}	These pins are connected to a 32.768-kHz crystal oscillator for subclock oscillation.	–	(Oscillates.)
71	V_{LCDC}	Input to regulate the reference voltage to drive LCD.	–	–
70 72 73	V_{LCD0} V_{LCD1} V_{LCD2}	Reference voltage outputs to drive LCD. • V_{LCD0}: Reference voltage output • V_{LCD1}: Doubler output (Two times the reference voltage) • V_{LCD2}: Tripler output (Three times the reference voltage)	–	–
74 75	CAPH CAPL	These pins are connected to a capacitor to boost the LCD drive voltage.	–	–

1.2 PROM PROGRAMMING MODE

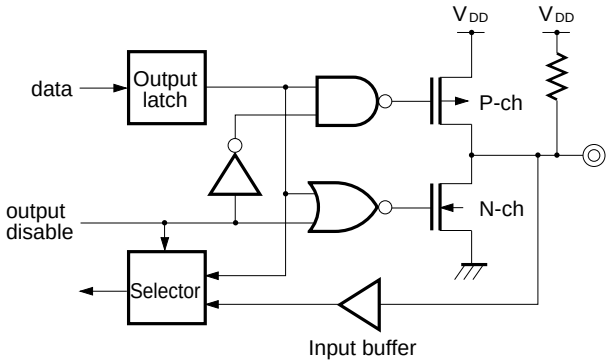
Pin No.	Symbol	Function	Output Type	On Reset
33	GND	Ground	–	–
35	V_{DD}	Positive power supply	–	–
40	GND_{ADC}	Ground for A/D converter Performs PROM programming with GND_{ADC} = GND.	–	–
41	V_{PP}	Positive power supply for PROM programming. Applies 12.5V as the program voltage when writing, reading, and verifying the program memory.	–	–
42 to 45 50 to 53	D_0 to D_3 D_4 to D_7	8-bit data I/O for PROM programming.	CMOS, push-pull	Input
46 to 49	MD_0 to MD_3	Select operation mode for PROM programming.	–	Input
62	V_{DD}	Positive power supply	–	–
63	CLK	Address update clock input	–	Input

Remark Pins other than the above are not used in the PROM programming mode. For the processing of unused pins, refer to **(2) PROM programming mode** in **PIN CONFIGURATION**.

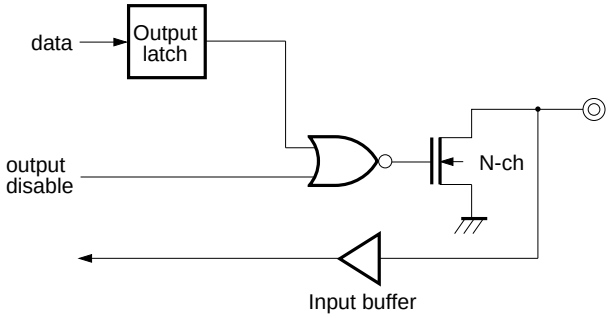
1.3 EQUIVALENT CIRCUITS OF PINS

The followings are equivalent circuits (partially simplified) of the respective pins of the μPD17P207.

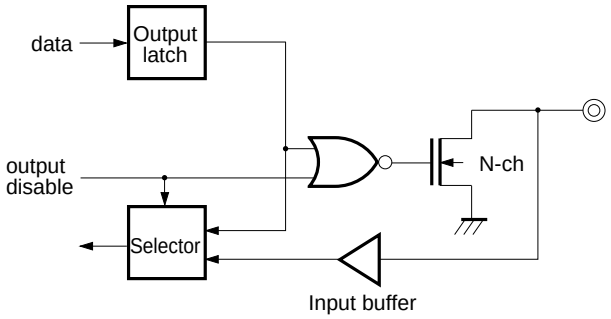
(1) P0A



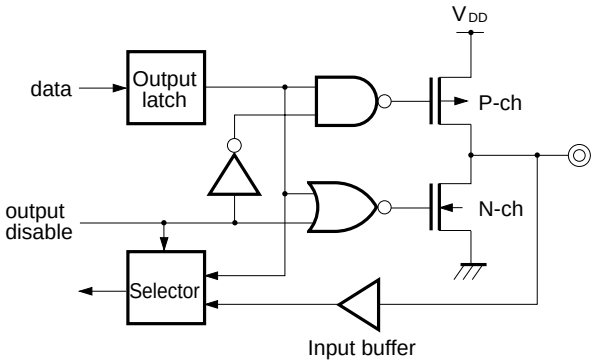
(2) P0B



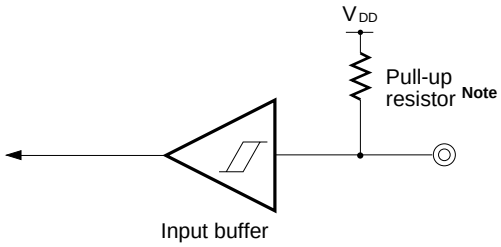
(3) P0C



(4) P0D, P1A



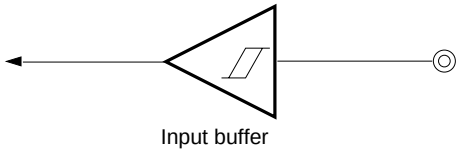
(5) $\overline{\text{RESET}}$



Schmitt trigger input with hysteresis characteristics

Note Only μPD17P207-001 has the internal pull-up resistor.

(6) INT



Schmitt trigger input with hysteresis characteristics

1.4 PROCESSING OF UNUSED PINS

In ordinay operation mode, process unused pins as follows:

Table 1-1. Processing of Unused Pins ★

(a) Port pins

Pin Name		Recommended Processing of Unused Pins	
		Internally	Externally
Input Mode	P0A	(Connect pull-up resistor.)	Open
	P0C	–	Directly connect to GND.
	P0D, P1A	–	Connect each pin to V_{DD} or GND via resistor[Note].
Output Mode	P0A (CMOS port)	Outputs high level	Open
	P0D, P1A (CMOS port)	–	
	P0B, P0C (N-ch open-drain port)	Outputs low level	

Note When externally pulling a pin up (connecting the pin to V_{DD} via resistor) and down (connecting the pin to GND via resistor), give adequate consideration to the drive capability and current consumption of the port. To pull a pin up or down at a high resistance, make sure that no noise is superimposed on the pin.

(b) Pins other than port pins

Pn Name	I/O Mode	Recommended Processing of Unused Pin
ADC_0-ADC_3	Input	Directly connect to GND
CAPH, CAPL	Output	Open
COM_0, COM_1, COM_2/LCD_{35}, COM_3/LCD_{34}	Output	Open
INT[Note]	Input	Directly connect to GND
LCD_0-LCD_{33}	Output	Open
REM	Output	Open
V_{ADC}	–	Directly connect to V_{DD}
V_{LCD0}-V_{LCD2}	Output	Open
V_{LCDC}	–	Directly connect to V_{DD} or V_{LCD0}
$\overline{WDOUT}$	Output	Directly connect to GND
X_{IN}, XT_{IN}	Input	Directly connect to GND
X_{OUT}	–	Directly connect to V_{DD}
XT_{OUT}	–	Directly connect to V_{REG}

Note The INT pin is also used as a test mode setting pin. Directly connect this pin to GND when it is not used.

Cautions 1. It is recommended that the input/output mode and output level of a pin be fixed by repeatedly setting in each loop of the program.

2. When the LCD controller/driver is not used, stop the voltage regulator by using the display mode register.

1.5 NOTES ON USING $\overline{\text{RESET}}$ AND INT PINS (ONLY IN ORDINARY OPERATION MODE)

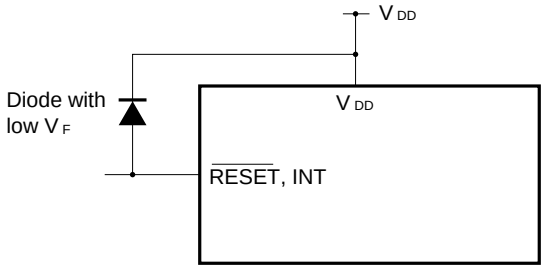
In addition to the functions shown in 1. PIN FUNCTIONS, the $\overline{\text{RESET}}$ and INT pins also have a function to set a test mode (for IC testing) in which the internal operations of the μPD17P207are tested.

When a voltage higher than V_{DD} is applied to either of these pins, the test mode is set. This means that, even during ordinary operation, the μPD17P207 may be set in the test mode if a noise exceeding V_{DD} is applied.

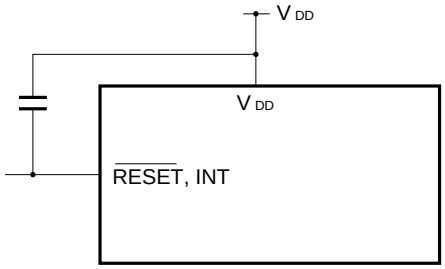
For example, if the wiring length of the $\overline{\text{RESET}}$ or INT pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- Connect diode with low V_F between V_{DD} and $\overline{\text{RESET}}$/INT pin



- Connect capacitor between V_{DD} and $\overline{\text{RESET}}$/INT pin



2. ONE-TIME PROM (PROGRAM MEMORY) WRITING, READING, AND VERIFICATION

μPD17P207 sets the PROM mode when PROM writing, reading or verification as shown in Table 2-1.

In PROM mode, no address input pin is used. Instead, the address is updated by the clock for input from the CLK pin.

Table 2-1. Pins Used for Program Memory Writing, Reading, or Verification

Pin Name	Function
V_{PP}	Applies program voltage (12.5 V).
CLK	Inputs address update clock.
MD_0-MD_3	Selects operation mode.
D_0-D_7	Inputs and outputs 8-bit data.
V_{DD}	Applies supply voltage (6 V).

2.1 OPERATION MODE FOR WRITING, READING, AND VERIFICATION OF PROGRAM MEMORY

If +6 V is applied to the V_{DD} and +12.5 V to the V_{PP} pin after μPD17P207 has been placed in the reset status for a fixed time (V_{DD} = 5V, $\overline{RESET}$ = Low level), μPD17P207 enters program memory write, read, or verify mode.

The MD_0 to MD_3 pins are used to set the operation modes listed in Table 2-2.

Leave the pins not used for program memory writing, reading, or verification open or ground through pull-down resistors (470 Ω). (Refer to **(2) PROM programming mode** in **PIN CONFIGURATION**.)

Table 2-2. Operating Mode for Program Memory Writing, Reading or Verification

Operating Mode Specification						Operating Mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	x	H	H	Program inhibit mode

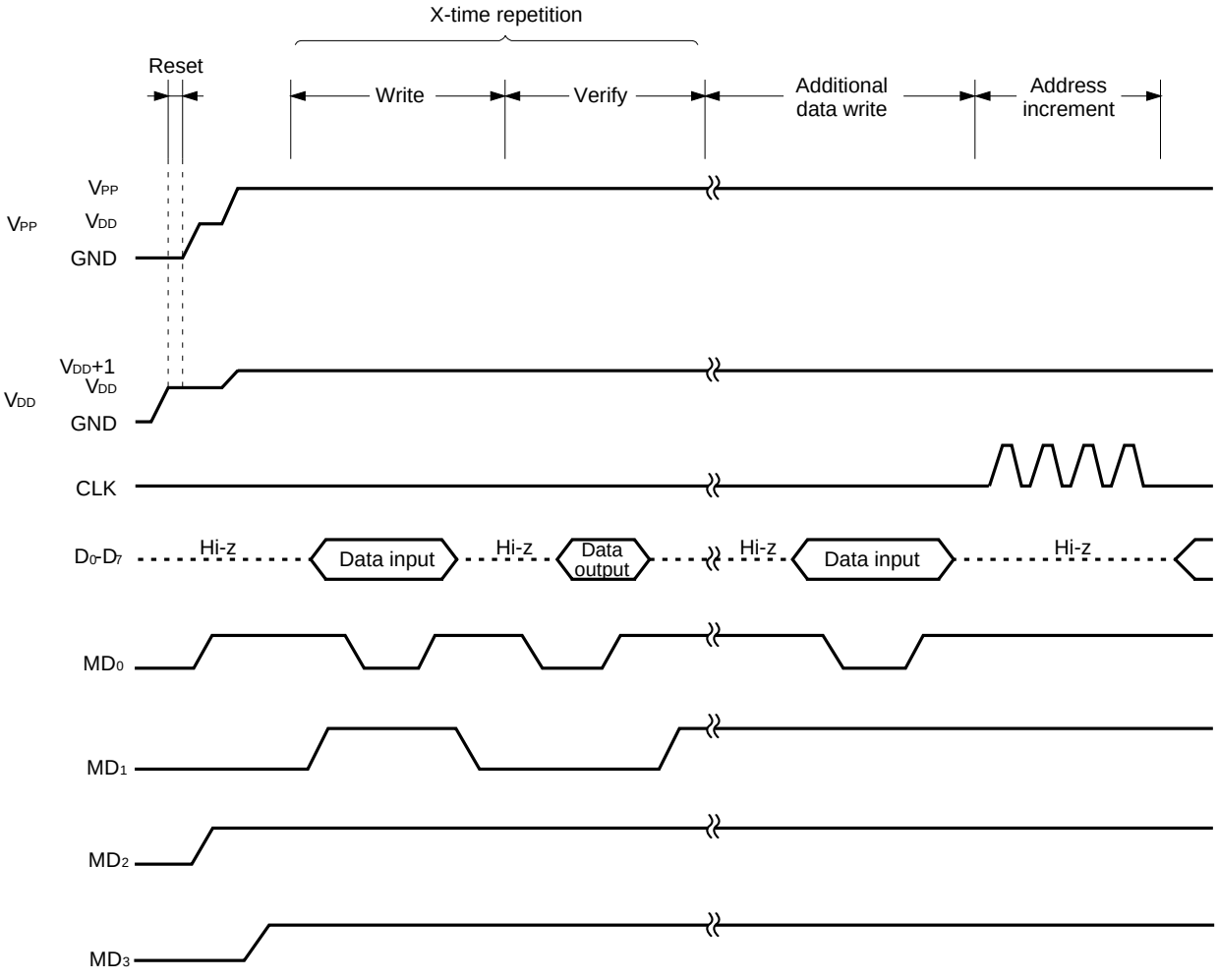
Remark x: L or H

2.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory write procedure is as follows. High-speed program memory write is possible.

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin must be low.
(3) After waiting for 10 μs, supply 5 V to the V_{PP} pin.
(4) Operate the MD0 to MD3 pins to set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Write data in 1-millisecond write mode.
(8) Set program inhibit mode.
(9) Set verify mode. If data has been written connectly, proceed to step (10). If data has not yet been written, repeat steps (7) to (9).
(10) Write additional data for (the number of times data was written (X) in steps (7) to (9)) times 1 milliseconds.
(11) Set program inhibit mode.
(12) Supply a pulse to the CLK pin four times to update the program memory address by 1.
(13) Repeat steps (7) to (12) to the last address.
(14) Set program memory address 0 clear mode.
(15) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power supply.

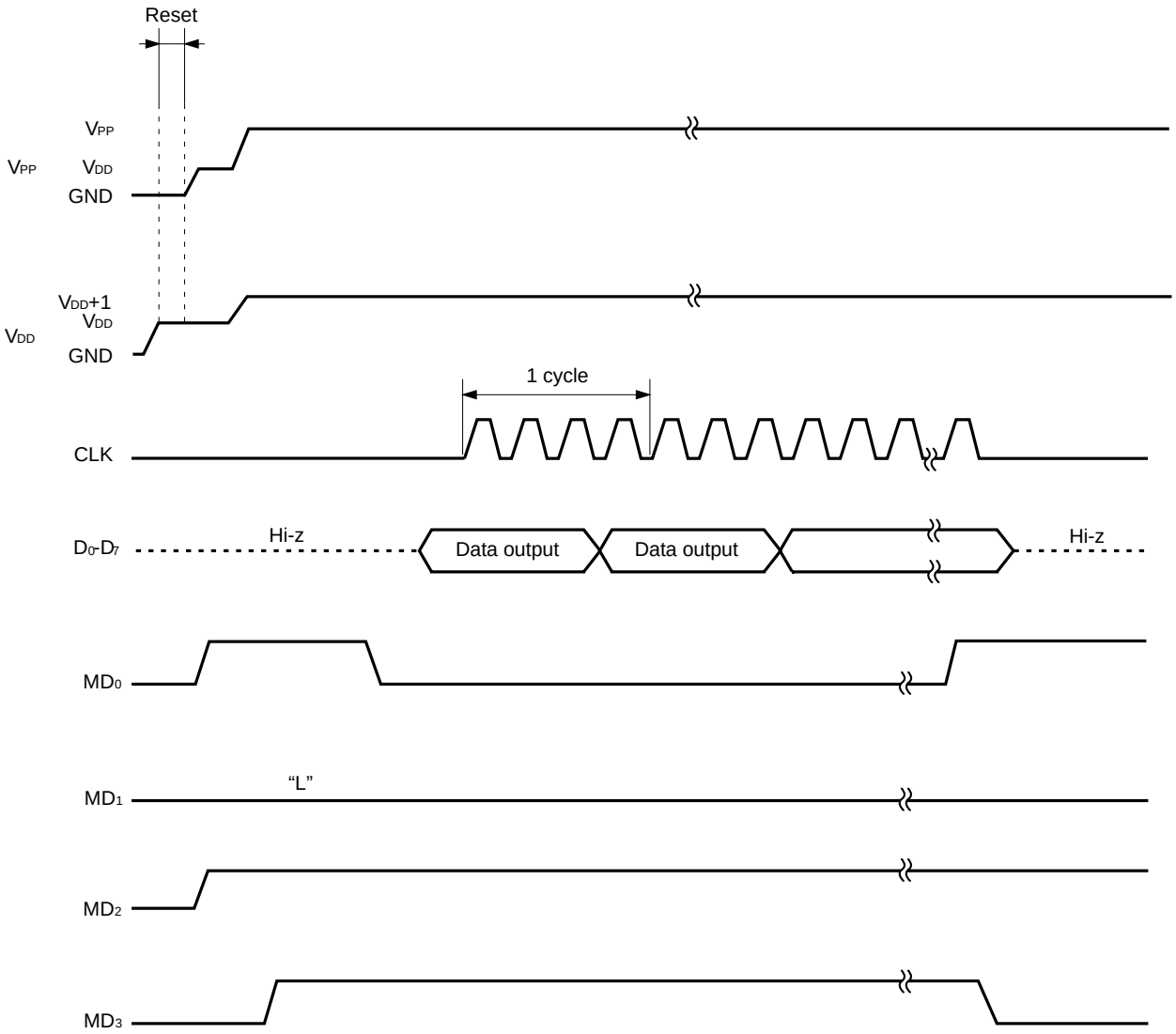
Steps (2) to (12) are illustrated below.



2.3 PROGRAM MEMORY READ PROCEDURE

(1) Ground the unused pins through pull-down resistors. The CLK pin must be low.
(2) Supply 5 V to the V_{DD} pin. The V_{PP} pin must be low.
(3) After waiting for 10 μs, supply 5 V to the V_{PP} pin.
(4) Operate the MD0 to MD3 pins to set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Set verify mode. Data of each address is sequentially output each time a clock pulse is input to the CLK pin four times.
(8) Set program inhibit mode.
(9) Set program memory address 0 clear mode.
(10) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power supply.

Steps (2) to (9) are illustrated below.



3. DIFFERENCES BETWEEN μPD17P207 AND μPD17201A/17207

The μPD17P207 has a PROM to which the user can write a program in place of the internal mask ROM (program memory) of the μPD17201A and 17207. Therefore, the μPD17P207 is identical to μPD17201A and 17207 except for the program memory and mask option. However, some of the electrical characteristics, such as supply current or V_{LCDC} voltage of the μPD17P207, are different from that of the μPD17201A and 17207.

The following table lists the differences between the μPD17P207 and μPD17201A/17207.

For the details of the CPU and hardware of the μPD17201A and 17207, refer to their Data Sheets.

<table>
<tr><th>Item / Product Name</th><th>μPD17P207
-001</th><th>μPD17P207
-002</th><th>μPD17P207
-003</th><th>μPD17201A</th><th>μPD17207</th></tr>
<tr><td>Program Memory</td><td colspan="3">One-Time PROM</td><td colspan="2">Mask ROM</td></tr>
<tr><td rowspan="2"></td><td colspan="3">0000H-0FFFH</td><td>0000H-0BFFH</td><td>0000H-0FFFH</td></tr>
<tr><td colspan="3">4096 × 16 bits</td><td>3072 × 16 bits</td><td>4096 × 16 bits</td></tr>
<tr><td>Pull-Up Resistor of $\overline{\text{RESET}}$ Pin</td><td rowspan="3">Provided</td><td>Not
provided</td><td rowspan="2">Not
provided</td><td colspan="2" rowspan="3">Any
(mask option)</td></tr>
<tr><td>Main Clock Oscillator Circuit</td><td>Provided</td></tr>
<tr><td>Subclock Oscillator Circuit</td><td>Not
provided</td><td>Provided</td></tr>
<tr><td>V_{PP} pin, PROM Programming Pin</td><td colspan="3">Provided</td><td colspan="2">Not provided</td></tr>
<tr><td>Supply Voltage
(T_A = –20 to +75°C)</td><td colspan="3">V_{DD} = 2.5 to 5.5 V (at f_X = 4 MHz, T_A = –20 to +75°C)
V_{DD} = 2.4 to 5.5 V (at f_X = 4 MHz, T_A = –20 to +60°C)</td><td colspan="2">V_{DD} = 2.2 to 5.5 V (at f_X = 4 MHz)</td></tr>
<tr><td>Package</td><td colspan="5">80-pin plastic QFP (14 × 20 mm)</td></tr>
</table>

4. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply Voltage	V_{DD}			–0.3 to +7.0	V
Analog Supply Voltage	V_{ADC}			–0.3 to +7.0	V
Input Voltage	VI			–0.3 to V_{DD}+0.3	V
Output Voltage	V_O			–0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	REM pin	Peak value	–30	mA
			rms value	–20	mA
		One pin (except REM)	Peak value	–7.5	mA
			rms value	–5	mA
		All pins (except REM)	Peak value	–22.5	mA
			rms value	–15	mA
Low-Level Output Current	I_{OL}	One pin	Peak value	7.5	mA
			rms value	5	mA
		All pins (except REM)	Peak value	22.5	mA
			rms value	15	mA
Operating Ambient Temperature	T_A			–20 to +75	°C
Storage Temperature	T_{stg}			–40 to +125	°C

Note rms value = Peak value × $\sqrt{\text{Duty}}$

Caution Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product.

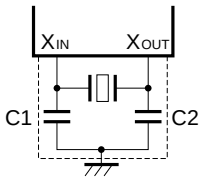
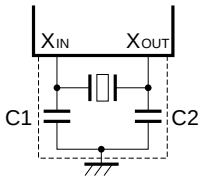
CAPACITANCE (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN1}	INT and $\overline{\text{RESET}}$ pins			10	pF
	C_{IN2}	Other than INT and $\overline{\text{RESET}}$ pins			10	pF

RECOMMENDED OPERATING RANGES (T_A = –20 to + 75°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD1}	System clock f_X = 4 MHz	2.5	3.0	5.5	V
		f_X = 4 MHz, T_A = –20 to + 60°C	2.4	3.0	5.5	V
	V_{DD2}	System clock f_X = 8 MHz	4.5	5.0	5.5	V
	V_{DD3}	System clock f_{XT} = 32.768 kHz	2.0	3.0	5.5	V
Main Clock Oscillation Frequency	f_X		1.0	4.0	8.0	MHz
Subclock Oscillation Frequency	f_{XT}			32.768		kHz

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –20 to +75°C, V_{DD} = 2.5 to 5.5 V)

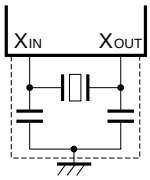
Resonator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Note 3 Ceramic Resonator		Oscillation frequency (f_X) Note 1		1.0	4	8.0	MHz
		Oscillation stabilization time Note 2	From when V_{DD} reaches the minimum oscillation voltage			4	ms
Note 3 Crystal Resonator		Oscillation frequency (f_X) Note 1		1.0	4	8.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5V			10	ms
						30	ms

Notes 1. The oscillation frequency is indicated only to express the oscillator characteristics. Refer to the AC characteristics for instruction execution time.

2. The oscillation stabilization time is the time required for stabilizing the oscillation after VDD is applied or the STOP mode is released.

3. The recommended resonators are shown in the table described later.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS

Resonator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal Resonator		Oscillation frequency (f_{XT})			32.768		kHz
		Oscillation stabilization time			5	10	s

Caution When using the main system clock and the subsystem clock generators, in order to avoid wiring capacitance effects, the following notations must be read and observed for wiring the portion inside the dotted line in the table:

- **Wiring length must be minimized.**
- **Do not cross with other signal lines. Do not wire close to a large current line.**
- **Capacitors used in the oscillators must always be grounded to GND potential level. Never ground the grounding pattern having a large current flow.**
- **Do not take the signal directly out of the oscillator.**

In order to reduce the power consumption, the subsystem clock oscillator employs a low amplification factor circuit. Because of this, the subsystem clock oscillator is more sensitive to noise than the main system clock oscillator. Therefore, when using the subsystem clock, wiring must be carefully planned.

RECOMMENDED RESONATORS

Main System Clock : Ceramic Resonator

Manufacturer	Part Name	External Capacitance (pF)		Oscillation Voltage Range (V)		Remarks
		C1	C2	MIN.	MAX.	
MURATA Mfg.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	Not required	Not required	2.0	6.0	Built-in capacitor
	CST4.00MGW	Not required	Not required	2.0	6.0	
	CST4.19MGW	Not required	Not required	2.0	6.0	
KYOCERA	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KBR4.19MS	33	33	2.0	6.0	
TOKO	CRHF4.00	18	18	2.0	6.0	
DAISHINKU	PRS0400BCSAN	39	33	2.0	6.0	

Main System Clock : Crystal Resonator

Manufacturer	Frequency (MHz)	Holder	External Capacitance (pF)		Oscillation Voltage Range (V)		Remarks
			C1	C2	MIN.	MAX.	
KINSEKI	4.0	HC-49U-S	22	22	2.0	6.0	

DC CHARACTERISTICS (T_A = –20 to +75°C, V_{DD} = V_{ADC} = 3 V)

Parameter	Symbol	Test Condition		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	$\overline{RESET}$ and INT pins		2.4		3	V
	V_{IH2}	Other than $\overline{RESET}$ and INT pins		2.1		3	V
Low-Level Input Voltage	V_{IL1}	$\overline{RESET}$ and INT pins		0		0.6	V
	V_{IL2}	Other than $\overline{RESET}$ and INT pins		0		0.9	V
High-Level Input Leakage Current	I_{LIH1}	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins				20	μA
	I_{LIH2}	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins				3	μA
Low-Level Input Leakage Current	I_{LIL1}	XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins				–20	μA
	I_{LIL2}	Other than XT_{IN}, XT_{OUT}, X_{IN}, and X_{OUT} pins				–3	μA
High-Level Output Current	I_{OH1}	REM pin	V_{OH} = 1.8 V	–7	–15		mA
	I_{OH2}	**Note 1**	V_{OH} = 2.7 V	–0.3	–0.7		mA
Low-Level Output Current	I_{OL}	**Note 2**	V_{OL} = 0.3 V	0.5	0.9		mA
Built-In Pull-Up Resistor	R_{P0A}	P0A0 to P0A3 pins		100	200	350	kΩ
	R_{RES}	$\overline{RESET}$ pins (μPD17P207-001 only)		24	47	94	kΩ
A/D Absolute Precision						±2	LSB
A/D Resolution					8		Bits
A/D Converter Current Consumption	I_{ADC}				60	120	μA
Comparator Error		In comparator mode			10	20	mV
Supply Current	I_{DD1}	X installed (f_X = 4.19 MHz) XT not installed	RUN mode		1.6	2.2	mA
	I_{DD2}		HALT mode			1.8	mA
	I_{DD3}		STOP mode		3.0	10.0	μA
	I_{DD4}	X not installed or STOP mode XT installed (f_{XT} = 32.768 kHz)	RUN mode		400	600	μA
	Note 3 I_{DD5}		HALT mode		20	40	μA

Notes 1. $P0A_0$ to $P0A_3$, $P0D_0$ to $P0D_3$, and $P1A_0$ to $P1A_2$ pins

2. $P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P0D_0$ to $P0D_3$, $P1A_0$ to $P1A_2$, $\overline{WDOUT}$, and REM pins

3. The specifications of the main STOP mode (sub-mounting) are the same as the sub-HALT mode (with the main clock oscillation stopped).

LCD CHARACTERISTICS (T_A = –20 to +75°C, V_{DD} = 3 V)

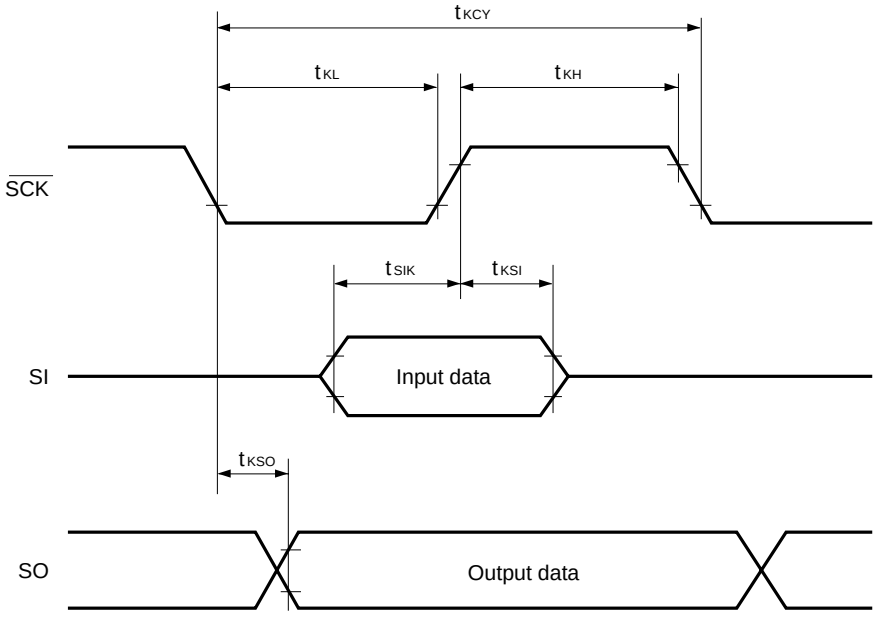
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
VLCDC Output Voltage	V_{LCDC}	T_A = 25°C, R1 = R2 = 1 MΩ	0.5	0.65	0.8	V
LCD Reference Output Voltage	V_{LCD0}	External variable resistance (0 to 2.2 MΩ)	0.8		1.8	V
Doubler Output Voltage	V_{LCD1}	C1 to C4 = 0.47 μF	1.9	2.0		V_{LCD0}
Tripler Output Voltage	V_{LCD2}	C1 to C4 = 0.47 μF	2.85	3.0		V_{LCD0}
LCD Common Output Current	I_{COM}	Output voltage deviation = 0.2 V	30			μA
LCD Segment Output Current	I_{LCD}	Output voltage deviation = 0.2 V	5			μA

AC CHARACTERISTICS (T_A = –20 to +75°C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Input Cycle Time	t_{KCY}	V_{DD} = 5 V±10 %	Data input	2.0			μs
			Data output	10			μs
			Data input	5			μs
			Data output	13			μs
$\overline{SCK}$ Input High- and Low-Level Widths	t_{KH}, t_{KL}	V_{DD} = 5 V±10 %	Data input	1.0			μs
			Data output	5.0			μs
			Data input	2.5			μs
			Data output	6.5			μs
SI Setup Time (Vs. $\overline{SCK}$↑)	t_{SIK}			100			ns
SI Hold Time (Vs. $\overline{SCK}$↑)	t_{KSI}			100			ns
$\overline{SCK}$↓→to SO Output Delay Time	t_{KSO}	C_L = 100 pF				4.5	μs
INT High-and Low-Level Width	t_{IOH}, t_{IOL}			50			μs
$\overline{RESET}$ Low-Level Width	t_{RSL}			50			μs
P0A Low-Level Width	t_{RLSL}	At standby release		10			μs ★

SERIAL TRANSFER TIMING

3-line Serial I/O Mode:



DC PROGRAMMING CHARACTERISTICS (T_A = 25°C, V_{DD} = 6.0 ±0.25V, V_{PP} = 12.5 ±0.3V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Other than CLK	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} –0.5		V_{DD}	V
Low-Level Input Voltage	V_{IL1}	Other than CLK	0		0.3 V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input Leakage Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-Level Output Voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} Supply Current	I_{DD}				30	mA
V_{PP} Supply Current	I_{PP}	MD_0 = V_{IL}, MD_1 = V_{IH}			30	mA

Cautions 1. V_{PP} must not exceed +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP} and disconnect it after V_{PP}.

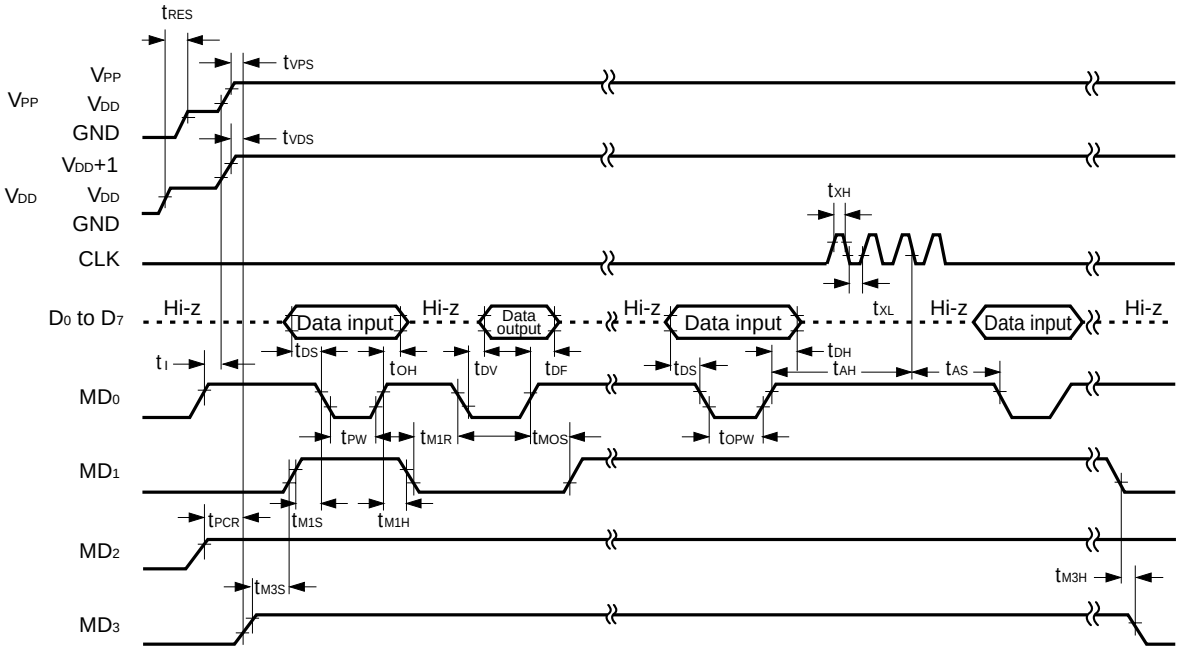
AC PROGRAMMING CHARACTERISTICS (T_A = 25°C, V_{DD} = 6.0 ±0.25V, V_{PP} = 12.5 ±0.3V)

Parameter	Symbol	**Note 1**	Conditions	MIN.	TYP.	MAX.	Unit
Address Setup Time **Note 2** (vs.MD_0↓)	t_{AS}	t_{AS}		2			μs
MD_1 Setup Time (vs. MD_0↓)	t_{M1S}	t_{OES}		2			μs
Data Setup Time (vs. MD_0↓)	t_{DS}	t_{DS}		2			μs
Address Hold Time **Note 2** (vs.MD_0↑)	t_{AH}	t_{AH}		2			μs
Data Hold Time (vs. MD_0↑)	t_{DH}	t_{DH}		2			μs
MD_0 ↑→ Data Output Float Delay Time	t_{DF}	t_{DF}		0		130	μs
V_{PP} Setup Time (vs. MD_3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} Setup Time (vs. MD_3↑)	t_{VDS}	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD_0 Setup Time (vs. MD_1↑)	t_{MOS}	t_{CES}		2			μs
MD_0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}	$MD_0 = MD_1 = V_{IL}$			1	μs
MD_1 Hold Time (vs. MD_0↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD_1 Recovery Time (vs. MD_0↓)	t_{M1R}	t_{OR}		2			μs
Program Counter Reset Time	t_{PCR}	–		10			μs
CLK Input High-/Low- Level Width	t_{XH},t_{XL}	–		0.125			μs
CLK Input Frequency	f_X	–				4	MHz
Initial Mode Set Time	t_I	–		2			μs
MD_3 Setup Time (vs. MD_1↑)	t_{M3S}	–		2			μs
MD_3 Hold Time (vs. MD_1↓)	t_{M3H}	–		2			μs
MD_3 Setup Time (vs. MD_0↓)	t_{M3SR}	–	When data is read from program memory	2			μs
Address **Note 2** → Data Output Delay Time	t_{DAD}	t_{ACC}				2	μs
Address **Note 2** → Data Output Hold Time	t_{HAD}	t_{OH}		0		130	μs
MD_3 Hold Time (vs. MD_0↑)	t_{M3HR}	–		2			μs
MD_3 ↓→ Data Output Float Delay Time	t_{DFR}	–				2	μs
Reset Setup Time	t_{RES}	–		10			μs

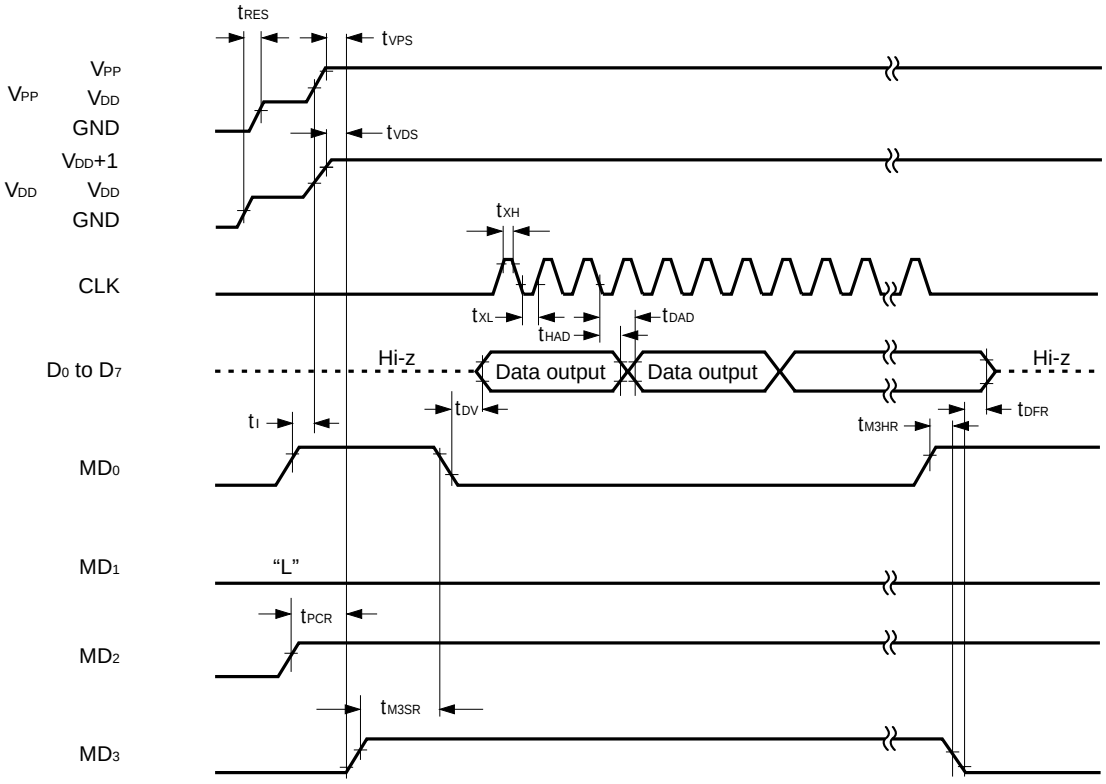
Notes 1. These symbols are the corresponding μPD27C256A (maintenance product) symbols.

2. The internal address is incremented by 1 at the third falling edge of CLK (with four clocks constituting as one cycle). The internal address is not connected to any pin.

PROGRAM MEMORY WRITE TIMING

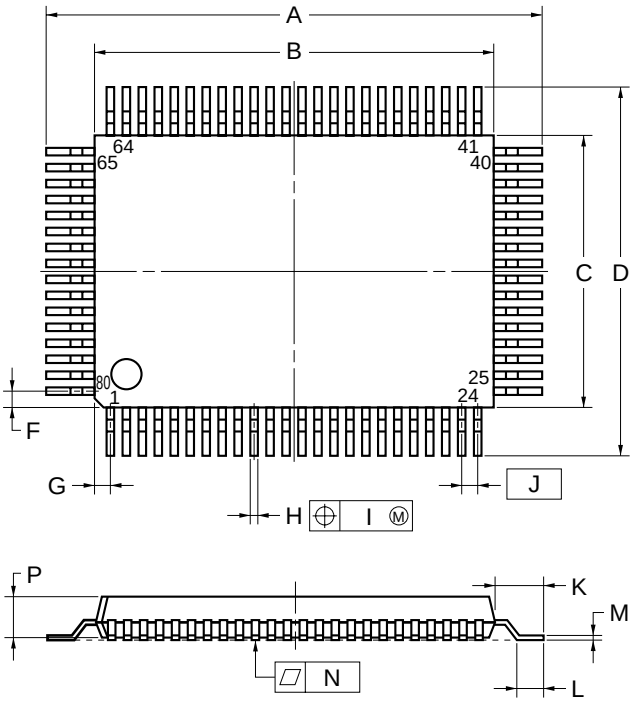


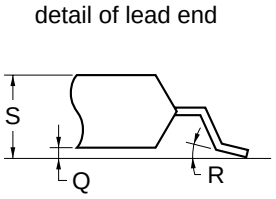
PROGRAM MEMORY READ TIMING



5. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	1.0	0.039
G	1.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GF-80-3B9-3

6. RECOMMENDED SOLDERING CONDITIONS

When mounting the μPD17P207 by soldering, soldering should be performed under the following recommended contitions.

For details on recommended soldering conditions, refer to the information document "Semconductor Device Mounting Technology Manual" (C10535E).

For other soldering methods, please cousult with NEC sales personnel.

★ **Table 6-1. Conditions for Surface Mounting**

μPD17P207GF-001-3B9 : 80-pin plastic QFP (14 × 20 mm)
μPD17P207GF-002-3B9 : 80-pin plastic QFP (14 × 20 mm)
μPD17P207GF-003-3B9 : 80-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Conditions Reference Code
Infrared Reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 20 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	IR35-207-2
VPS	Package peak temperature: 215°C Time: 40 seconds max. (200°C min.), Number of times: 2 max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 20 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	VP15-207-2
Wave Soldering	Soldering bath temperature: 260 °C max., Time: 10 seconds max., Number of times: 1 Preheating temperature: 120 °C max. (package surface temperature) Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 20 hours)	WS 60-207-1
Partial Heating	Pin temperature: 300°C max., Time: 3 seconds max. (per device)	——

Note Number of days after unpacking the dry pack. Storage conditions are 25°C and 65 %RH max.

Caution Do not use different soldering methods together (however, pin partial heating can be performed with other soldering methods).

APPENDIX A. MICROCONTROLLER FAMILY FOR HIGH-FUNCTION REMOTE CONTROLLER WITH LCD

Item / Product Name		μPD17201A	μPD17207	μPD17P207
ROM Capacity		3072 × 16 bits (Mask ROM)	4096 × 16 bits (Mask ROM)	4096 × 16 bits (One-Time PROM)
RAM Capacity		336 × 4 bits		
LCD Controller/Driver		136 segments max.		
Infrared Remote Controller Carrier Generator		LED output is high-active.		
Number of I/O Ports		19		
External Interrupt (INT)		1		
Timer		2 channels { 8-bit timer : 1; Watch timer : 1 }		
Watchdog Timer		Internal ($\overline{\text{WDOUT}}$ output)		
Serial Interface		1 channel		
Stack		5 levels (3 levels for multiplexed interrupt)		
Instruction Execution Time	Main System Clock	4 μs (4 MHz: with ceramic or crystal oscillator)		
	Subsystem Clock	488 μs (32.768 kHz: with crystal osciallator)		
Supply Voltage (T_A = –20 to +75°C)	Main System Clock	2.2 to 5.5 V		2.5 to 5.5 V 2.4 to 5.5 V **Note**
	Subsystem Clock	2.0 to 5.5 V		
Standby Function		STOP, HALT		
Pakcage		80-pin plastic QFP		

Note T_A = –20 to + 60°C

APPENDIX B. DEVELOPMENT TOOLS

To develop the programs for the μPD17P207, the following development tools are available:

Hardware

Name	Remarks
In-Circuit Emulator (IE-17K IE-17K-ET Note 1 EMU-17K Note 2)	IE-17K, IE-17K-ET, and EMU-17K are the in-circuit emulators used in common with the 17K series microcomputer. IE-17K and IE-17K-ET are connected to a PC-9800 series or IBM PC/AT™ as the host machine with RS-232C. EMU-17K is inserted into the expansion slot of a PC-9800 series. By using these in-circuit emulators with a system evaluation board corresponding to the microcomputer, the emulators can emulate the microcomputer. A higher level debugging environment can be provided by using man-machine interface *SIMPLEHOST*™. EMU-17K also has a function by which you can check the contents of data memory realtime.
SE Board (SE-17207)	This is an SE board for μPD17201A, 17207, and 17P207. It can be used alone to evaluate a system or in combination with an in-circuit emulator for debugging.
Emulation Probe (EP-17201GF)	EP-17201GF is an emulation probe for μPD17201A, 17207, and 17P207. When used with EV-9200G-80, it connects an SE board to the target system.
Conversion Socket (EV-9200G-80 Note 3)	EV-9200G-80 is a conversion socket for 80-pin QFP (14 × 20 mm) and is used to connect EP-17201GF to the target system.
★ PROM Programmer (AF-9703 Note 4, AF-9704 Note 4, AF-9705 Note 4, AF-9706 Note 4)	AF-9703, AF-9704, AF-9705, and AF-9706 are PROM programmers corresponding to μPD17P207. By connecting program adapter AF-9808A to this PROM programmer, μPD17P207 can be programmed.
Program Adapter (AF-9808 Note 4)	AF-9808A is an adapter that is used to program μPD17P207, and is used in combination with AF-9703, AF-9704, AF-9705, or AF-9706.

Notes 1. Low-cost model: External power supply type

2. This is a product from IC Corp. For details, consult IC Corp.

3. Two EV-9200G-80s are supplied with the EP-17201GF. Five EV-9200G-80s are optionally available as a set.

4. These are products from Ando Electric. For details, consult Ando Electric.

Software

Name	Outline	Host Machine	OS Media		Supply	Order Code
17K Series Assembler (AS17K)	AS17K is an assembler that can be used in common with the 17K series products. When developing the program of the μPD17P207, AS17K is used in combination with a device file (AS17201 or AS17207).	PC-9800 series	MS-DOS™		5" 2HD	μS5A10AS17K
					3.5" 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5" 2HC	μS7B10AS17K
					3.5" 2HC	μS7B13AS17K
Device File (AS17201, AS17207)	AS17201 is a device file for μPD17201A. AS17207 is a device file for μPD17207. These are used in combination with an assembler for the 17K series (AS17K).	PC-9800 series	MS-DOS		5" 2HD	μS5A10AS17201 μS5A10AS17207
					3.5" 2HD	μS5A13AS17201 μS5A13AS17207
		IBM PC/AT	PC DOS		5" 2HC	μS7B10AS17201 μS7B10AS17207
					3.5" 2HC	μS7B13AS17201 μS7B13AS17207
Support Software (*SIMPLE-HOST*)	*SIMPLEHOST* is a software package that enables man-machine interface on the Windows™ when a program is developed by using an in-circuit emulator and a personal computer.	PC-9800 series	MS-DOS	Windows	5" 2HD	μS5A10IE17K
					3.5" 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5" 2HC	μS7B10IE17K
					3.5" 2HC	μS7B13IE17K

Remark The corresponding OS versions are as follows:

OS	Version
MS-DOS	Ver. 3.30 to Ver. 5.00A **Note**
PC DOS	Ver. 3.1 to Ver. 5.0 **Note**
Windows	Ver. 3.0 to Ver. 3.1

Note Ver. 5.00/5.00A of MS-DOS and Ver. 5.0 of PC DOS have a task swap function, but this function cannot be used with this software.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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