NEC

MOS INTEGRATED CIRCUIT

μPD17P068

4-BIT SINGLE-CHIP MICROCONTROLLER WITH ON-CHIP HARDWARE FOR TV SYSTEMS

The μPD17P068 is a one-time PROM version of the μPD17068 that has on-chip mask ROM.

The μPD17P068, which can be programmed only once, is suited for testing during development of μPD17068 systems and limited production runs.

Use this data sheet together with μPD17068 documents.

The μPD17P068 does not provide a level of reliability intended for mass production of the customer's products. Use it only for functional evaluation when experimenting or doing product trial tests.

FEATURES

- Compatible with the μPD17068
- One-time PROM : 12160 × 16 bits
- Operating voltage : V_{DD} = 5 V ± 10 %

ORDERING INFORMATION

Part Number	Package
μPD17P068GF-3BA	100-pin plastic QFP (14 × 20mm)

The information in this document is subject to change without notice.

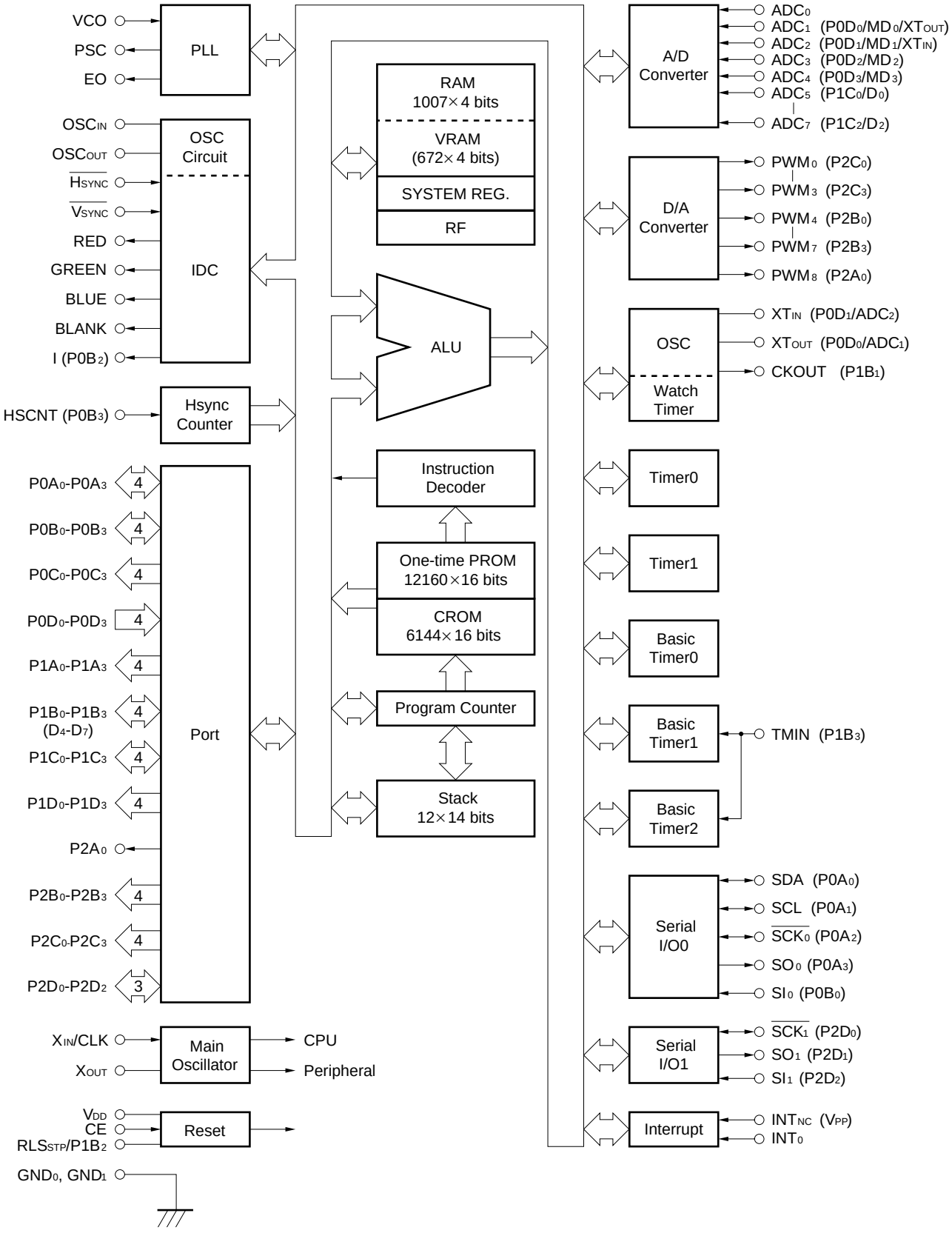
Document No. U10336EJ1V0DS00
Date Published November 1995 P
Printed in Japan

FUNCTIONAL OUTLINE

Item \ Part Number	μPD17068	μPD17P068
	Mask ROM	One-time PROM
Program memory (ROM)	• 12160 × 16 bits Table reference area: 12160 × 16 bits	
Character ROM (CROM)	• 6144 × 16 bits	
Data memory (RAM)	• 1007 × 4 bits (including area serving also as VRAM) Data buffer: 4 × 4 bits, general register: 16 × 4 bits	
Video RAM (VRAM)	• 672 × 4 bits (also used as data memory (RAM))	
System register	• 12 × 4 bits	
Register file	• 12 × 4 bits	
General port register	• 12 × 4 bits	
Instruction execution time	• 2 μs (when using 8-MHz crystal resonator)	
Stack levels	• 12 levels (stack manipulation possible)	
General ports	• I/O ports : 19 • Input ports : 4 • Output ports : 21	
IDC (Image Display Controller)	• Number of displayable characters : 192 characters max. per screen (up to 350 characters with program) • Display format : 16 × 16-dot mode 15 lines × 24 columns : 14 × 16-dot mode 17 lines × 24 columns • Character types : 255 types (user programmable) • Character format : 16 × 16 dots and 14 × 16 dots selectable (2 dots can be placed between characters) • Color : 15 colors • Character size : Vertical : 16 sizes (specifiable for each line) Horizontal : 24 sizes (specifiable for each character)	
Serial interface	• 2 systems Serial interface 0 (compatible with 2-wire system, 3-wire system and I^2C Bus) Serial interface 1 (3-wire system)	
D/A converter	• 8 bits × 9 channels (PWM output, 12.5 V max.)	
A/D converter	• 6 bits × 8 channels (successive approximation by software)	
Interrupt	• 10 channels (maskable interrupt) External interrupt : 3 channels (INT_0, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$) Internal interrupt : 7 channels (timer 0, 1, serial interface 0, 1, basic timer 2, VRAM pointer, timer 0 overflow)	

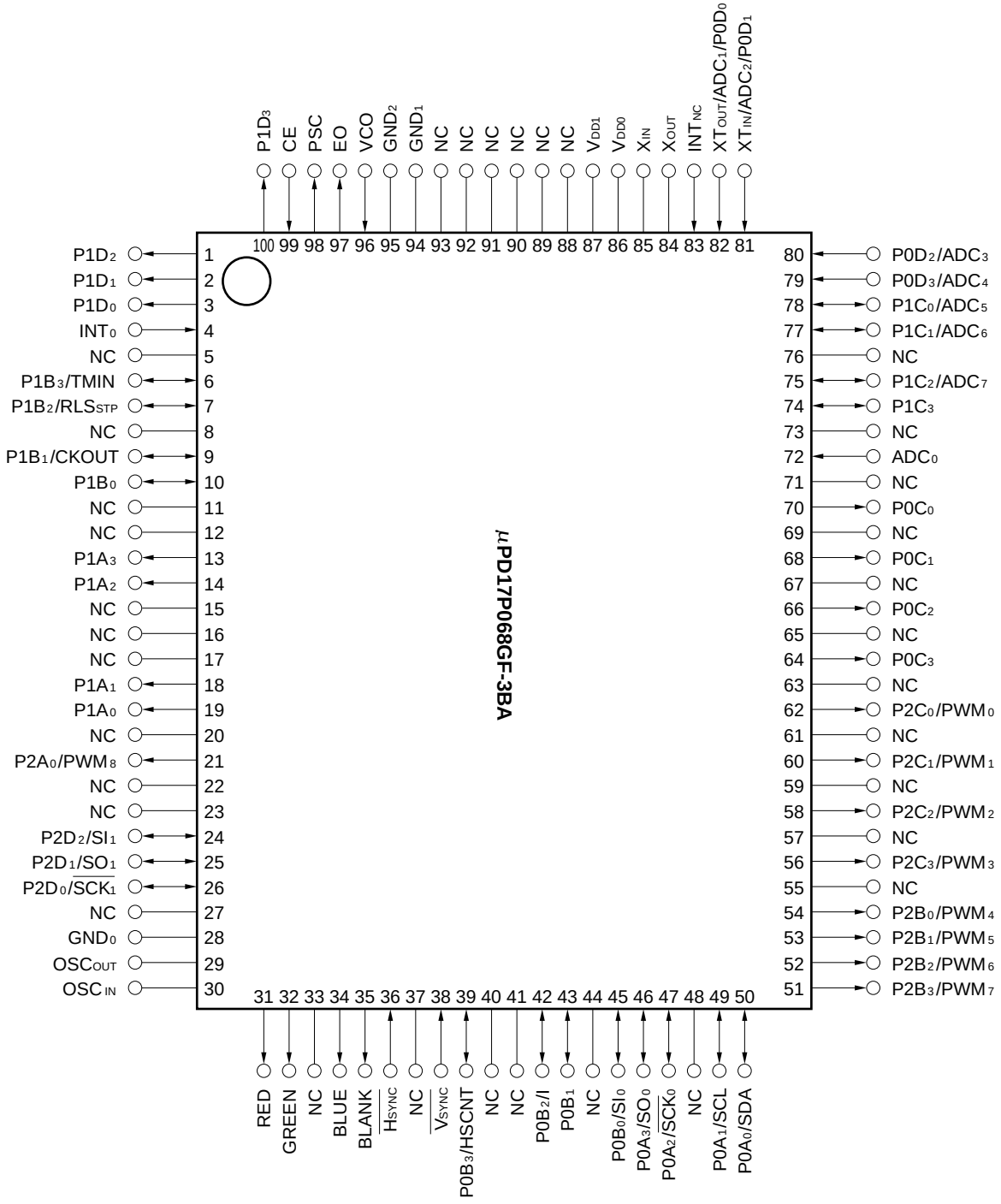
Item \ Part Number	μPD17068	μPD17P068
Timer	Timer 0 : 10 μs to 204.75 ms (interrupt) Timer 1 : 1 μs to 256 ms (interrupt) Basic timer 0 : 1, 5, 100 ms (carry) Basic timer 1 : 125 μs, 1 ms, 5 ms, 100 ms, external (carry) Basic timer 2 : 125 μs, 1 ms, 5 ms, 100 ms, external (interrupt) Watch timer : Date, Hour, Minute, Second (counter)	
Reset	• Power-on reset • Reset with CE pin (CE pin: Low level → High level) • Power interruption detection	
Supply voltage	V_{DD} = 5 V ± 10 %	
Package	100-pin plastic QFP (14 × 20 mm)	

BLOCK DIAGRAM

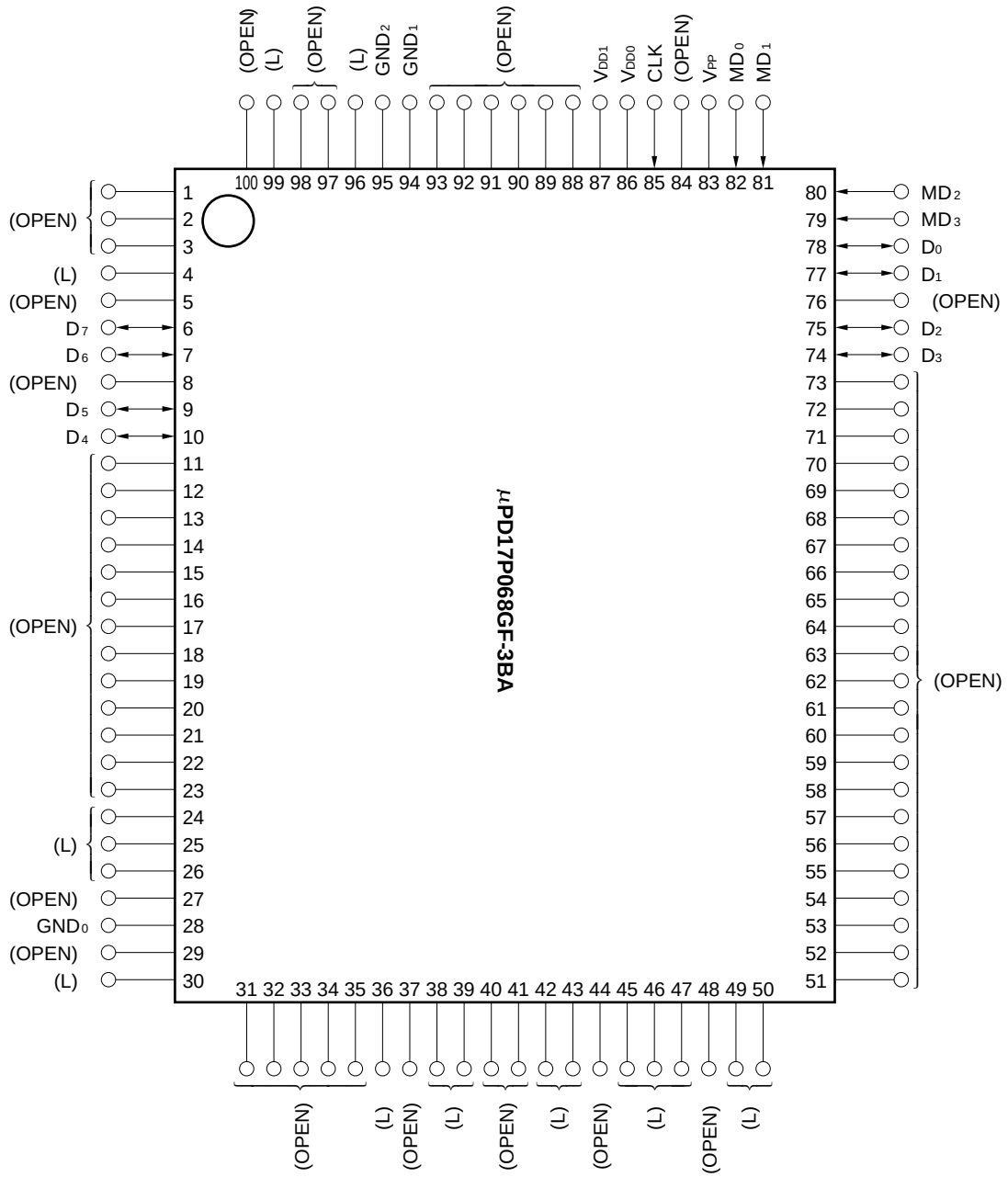


PIN CONFIGURATION (Top View)

(1) Normal operation mode



(2) PROM programming mode



Caution Contents in parentheses indicate how to handle unused pins in PROM programming mode.
L: Connect to GND via a resistor (470 Ω) separately.
OPEN: Leave unconnected.

PIN IDENTIFICATIONS

ADC_0-ADC_7 : A/D converter input
BLANK : Blanking signal output
BLUE : Character signal output
CE : Chip enable
CKOUT : Watch timer adjustment output
CLK : Address update clock input
D_0-D_7 : Data input/output
EO : Error out
GND_0-GND_2 : Ground
GREEN : Character signal output
HSCNT : Horizontal synchronizing signal counter input
$\overline{HSYNC}$: Horizontal synchronizing signal input
I : Character signal output
INT_0, INT_{NC} : External interrupt request signal input
MD_0-MD_3 : Operation mode select
NC : No connection
OSC_{IN}, OSC_{OUT} : LC oscillation for IDC
$P0A_0$-$P0A_3$: Port 0A
$P0B_0$-$P0B_3$: Port 0B
$P0C_0$-$P0C_3$: Port 0C
$P0D_0$-$P0D_3$: Port 0D
$P1A_0$-$P1A_3$: Port 1A
$P1B_0$-$P1B_3$: Port 1B
$P1C_0$-$P1C_3$: Port 1C
$P1D_0$-$P1D_3$: Port 1D
$P2A_0$: Port 2A
$P2B_0$-$P2B_3$: Port 2B
$P2C_0$-$P2C_3$: Port 2C
$P2D_0$-$P2D_2$: Port 2D
PSC : Pulse swallow control output
PWM_0-PWM_8 : Pulse-width modulation output
RED : Character signal output
RLS_{STP} : Clock stop release signal input
$\overline{SCK_0}$, $\overline{SCK_1}$: Shift clock input/output
SCL : Shift clock input/output
SDA : Serial data input/output
SI_0, SI_1 : Serial data input
SO_0, SO_1 : Serial data output
TMIN : Event input of basic timer 1 or 2
VCO : Local oscillation input
V_{DD0}, V_{DD1} : Positive power supply
V_{PP} : Program voltage application
$\overline{VSYNC}$: Vertical synchronizing signal input
X_{IN}, X_{OUT} : Main clock oscillation
XT_{IN}, XT_{OUT} : Watch timer oscillation

CONTENTS

1. PIN FUNCTIONS

1.1 Normal Operation Mode

(1) Port pins

Pin Name	Description	I/O	Output Type	When Reset	Shared by
$P0A_0$	4-bit I/O port. These pins serve as a bit-selectable 4-bit input/output port. All these pins are set to input pins when power (V_{DD}) is turned on, when clock is stopped, or when reset signal is input to the CE pin.	I/O	N-ch open drain	Input	SDA
$P0A_1$					SCL
$P0A_2$			CMOS push-pull		$\overline{SCK_0}$
$P0A_3$					SO_0
$P0B_0$	4-bit I/O port. These pins serve as a bit-selectable 4-bit input/output port. All these pins are set to input pins when power (V_{DD}) is turned on, when clock is stopped, or when reset signal is input to the CE pin.	I/O	CMOS push-pull	Input	SI_0
$P0B_1$					—
$P0B_2$					I
$P0B_3$					HSCNT
$P0C_0$ | $P0C_3$	These pins serve as a 4-bit output port. The output state of each pin is undefined after power (V_{DD}) is turned on.	O	CMOS push-pull	Undefined output	—
$P0D_0$	These pins serve as a 4-bit input port.	I	—	Input with pull-down resistor	ADC_1/XT_{OUT}
$P0D_1$					ADC_2/XT_{IN}
$P0D_2$					ADC_3
$P0D_3$					ADC_4
$P1A_0$ | $P1A_3$	These pins serve as a 4-bit output port.	O	N-ch open-drain Middle voltage, high current	Undefined output	—
$P1B_0$	4-bit I/O port. These pins serve as a bit-selectable 4-bit input/output port.	I/O	CMOS push-pull	Input	—
$P1B_1$					CKOUT
$P1B_2$					RLS_{STP}
$P1B_3$					TMIN
$P1C_0$ | $P1C_2$	4-bit I/O port. These pins serve as 4-bit-selectable 4-bit I/O port.	I/O	CMOS push-pull	Input	ADC_5 | ADC_7
$P1C_3$					—
$P1D_0$ | $P1D_3$	These pins serve as a 4-bit output port.	O	CMOS push-pull	Undefined output	—
$P2A_0$	This pin serves as a 1-bit output port.	O	N-ch open-drain Middle voltage	Undefined output	PWM_8
$P2B_0$ | $P2B_3$	These pins serve as a 4-bit output port.	O	N-ch open-drain Middle voltage	Undefined output	PWM_4 | PWM_7
$P2C_0$ | $P2C_3$	These pins serve as a 4-bit output port.	O	N-ch open-drain Middle voltage	Undefined output	PWM_0 | PWM_3
$P2D_0$	These pins serve as a bit-selectable 3-bit input/output port. All these pins are set to input pins when power (V_{DD}) is turned on, when clock is stopped, or when reset signal is input to the CE pin.	I/O	CMOS push-pull	Input	$\overline{SCK_1}$
$P2D_1$					SO_1
$P2D_2$					SI_1

(2) Non-port pins

Pin Name	Description	I/O	Output Type	When Reset	Shared by
EO	This pin outputs signals from the charge pump of the PLL frequency synthesizer. If the frequency divided from the local oscillator (VCO) frequency is higher (lower) than the reference frequency, high (low) level is output from this pin, respectively. When the two frequencies match, this pin is placed in the high-impedance state.	O	CMOS 3-state	High-impedance	—
PSC	This pin outputs pulse swallow control signal. This signal switches division ratio for the dedicated prescaler μPB595.	O	CMOS push-pull	Output	—
VCO	This pin is the input of the local oscillator. The output signal coming from the local oscillator (VCO) in the tuner and divided by the dedicated prescaler μPB595 should be input to this pin, where the μPB595 is a two-module prescaler capable of frequency division up to 1 GHz.	I	—	Internally pulled down	—
HSCNT	This pin is the input of the H sync signal counter.	I	—	Input	$P0B_3$
BLANK	This active-high pin outputs blanking signals to delete video signals.	O	CMOS push-pull	Low level output	—
RED	This active-high pin outputs character data that correspond the R signal (one of the RGB signals of IDC).	O	CMOS push-pull	Low level output	—
GREEN	This active-high pin outputs character data that correspond the G signal (one of the RGB signals of IDC).	O	CMOS push-pull	Low level output	—
BLUE	This active-high pin outputs character data that correspond the B signal (one of the RGB signals of IDC).	O	CMOS push-pull	Low level output	—
I	This pin outputs character data that correspond the I signal of IDC.	O	CMOS push-pull	Input	$P0B_2$
$\overline{HSYNC}$	The H sync signals for IDC should be input to this pin in an active-low manner.	I	—	Input	—
$\overline{VSYNC}$	The V sync signals for IDC should be input to this pin in an active-low manner.	I	—	Input	—
OSC_{IN}	These are the input and output pins of the LC oscillation circuit for IDC. Adjust the oscillation frequency to 10 MHz.	—	—	—	—
OSC_{OUT}					
ADC_0	These are the analog input pins of the 6-bit resolution A/D converter.	I	—	Input	—
ADC_1					$P0D_0/XT_{OUT}$
ADC_2	These are the analog input pins of the 6-bit resolution A/D converter.	I	—	Input	$P0D_1/XT_{IN}$
ADC_3					$P0D_2$
ADC_4					$P0D_3$
ADC_5 | ADC_7					$P1C_0$ | $P1C_2$

Pin Name	Description	I/O	Output Type	When Reset	Shared by
PWM_0 | PWM_3	These are the output pins of the 8-bit resolution D/A converter.	O	N-ch open-drain Middle-voltage	Low-level output or high impedance	$P2C_0$ | $P2C_3$
PWM_4 | PWM_7					$P2B_0$ | $P2B_3$
PWM_8					$P2A_0$
TMIN	This pin is the input of basic timer 1 or 2.	I	—	Input	$P1B_3$
XT_{IN}	A 32.768-kHz crystal resonator for watch timer operation should be connected to these pins.	—	—	—	$P0D_1/ADC_2$
XT_{OUT}					$P0D_0/ADC_1$
CKOUT	This pin outputs the signal to control the watch timer.	O	CMOS push-pull	Input	$P1B_1$
$\overline{SCK_0}$	These pins input and output shift clocks.	I/O	CMOS push-pull	Input	$P0A_2$
$\overline{SCK_1}$					$P2D_0$
SI_0	These pins input serial data.	I	—	Input	$P0B_0$
SI_1					$P2D_2$
SO_0	These pins output serial data.	O	CMOS push-pull	Input	$P0A_3$
SO_1					$P2D_1$
SCL	These pins input and output shift clocks.	I/O	N-ch open-drain	Input	$P0A_1$
SDA	These pins input and output serial data.	I/O	N-ch open-drain	Input	$P0A_0$
INT_0	This pin inputs interrupt request signal from external device. An interrupt request is issued at the rising or falling edge of the input signal applied to this pin.	I	—	Input	—
INT_{NC}	This pin inputs interrupt request signal with noise canceller. Using this pin to input signals with noise such as commands from a remote control unit simplifies programming processes. The interrupt request issuing timing is programmable to either rising or falling edge of the input signal to this pin.	I	—	Input	—

Pin Name	Description	I/O	Output Type	When Reset	Shared by
CE	This pin selects a device to be activated, or resets this device. **(1) Use as input of device selection signal** When CE=high, PLL synthesizer and IDC operate. When CE=low, their operation are disabled (stops). **(2) Use as reset input** When CE changes from low to high, this device is reset in synchronization with the carry FF operation for the internal basic interval timer 0.	I	—	Input	—
RLS_{STP}	This pin inputs the clock stop release signal.	I	—	Input	$P1B_2$
X_{IN}	An 8-MHz crystal resonator for main clock generation should be connected to these pins.	—	—	—	—
X_{OUT}					
V_{DD0}	These pins supply positive power voltage for this device. The power supply voltage of 5 V ± 10 % should be applied to these pins when all functions operate. When IDC is disabled, the voltage range from 4.0 to 5.5 V is allowed. When clock is stopped, the applied voltage to these pins may be lowered down to 2.5 V. Because this device internally has the power-on reset circuit, the voltages applied to these pins are changed from 0 to 4.0 V, system reset sequence is started and the program is implemented from address 0H. To assure normal operations of the power-on reset circuit, the rise time from 0 to 4.0 V should be shorter than 500 ms.	—	—	—	—
V_{DD1}					
GND_0 | GND_2	These pins supply the ground level for this device.	—	—	—	—
NC	This pin should be left unconnected.	—	—	—	—

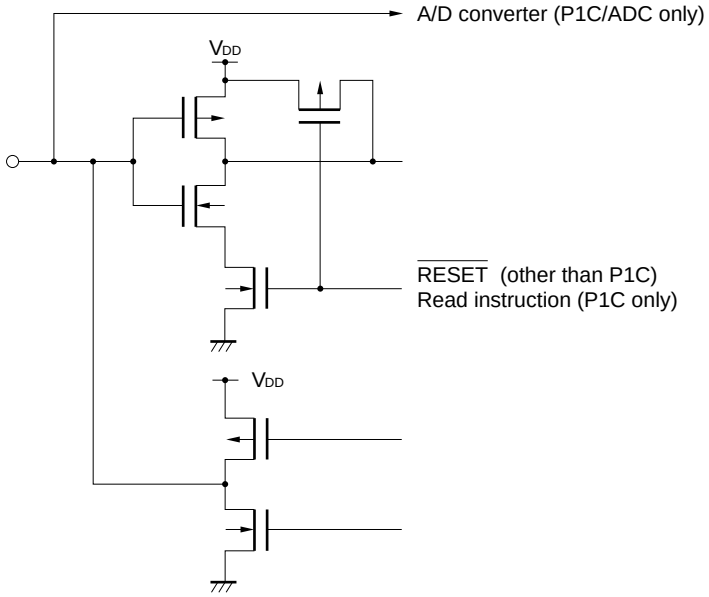
1.2 PROM Programming Mode

Pin Name	Description	I/O	Output Type
D_0 | D_7	8-bit data input/output pins used in program memory write, read, verify modes.	I/O	CMOS push-pull
MD_0 | MD_3	Input pins that select an operation mode in program memory write, read, verify modes.	I	—
CLK	Clock input for address update in program memory write, read, verify modes.	I	—
V_{PP}	Programming voltage (+12.5 V) application pin in program memory write, read, verify modes.	—	—
V_{DD0}	Positive power supply. +5 V should be applied to these pins in program memory write, read, verify modes.	—	—
V_{DD1}			
GND_0 | GND_2	Ground pin	—	—

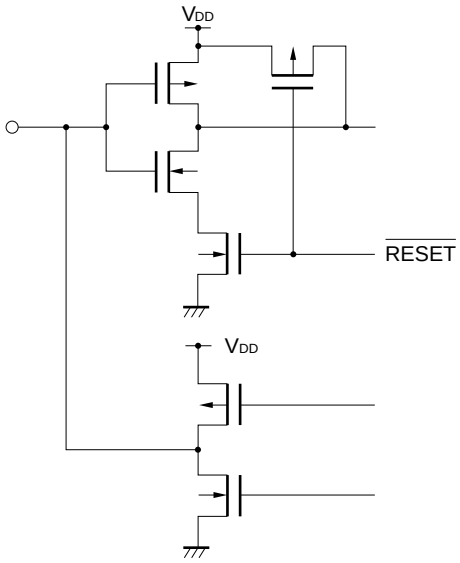
Remark The other pins are not used in the PROM programming mode. How to handle the other pins are described in the section **"PIN CONFIGURATION (2) PROM programming mode"**.

1.3 Pin Equivalent Circuits

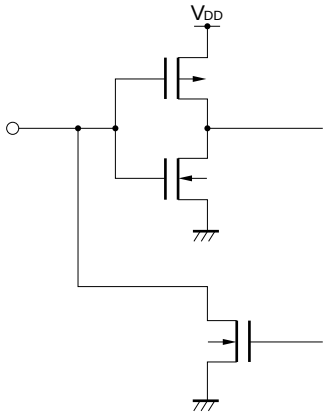
(1) P0A (P0A3/SO0, P0A2/$\overline{SCK0}$)
P0B (P0B2/I, P0B1, P0B0/SI0)
P1B (P1B2/RLSSTP, P1B1/CKOUT, P1B0)
P1C (P1C3, P1C2/ADC7, P1C1/ADC6, P1C0/ADC5)
(Input/output)



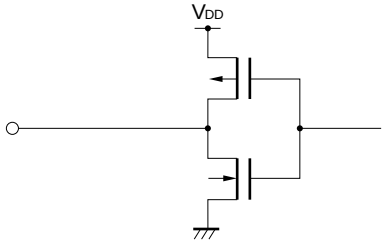
(2) P2D (P2D2/SI1, P2D1/SO1, P2D0/$\overline{SCK1}$) : (Input/output)



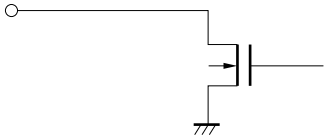
(3) P0A (P0A$_1$/SCL, P0A$_0$/SDA) : (Input/output)



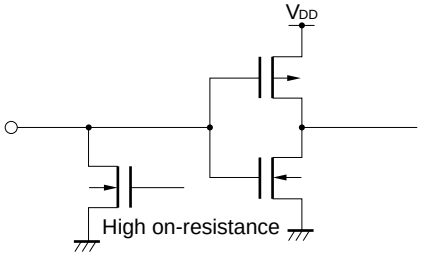
(4) P0C (P0C$_3$, P0C$_2$, P0C$_1$, P0C$_0$)
P1D (P1D$_3$, P1D$_2$, P1D$_1$, P1D$_0$)
RED, GREEN, BLUE, BLANK
PSC
(Output)



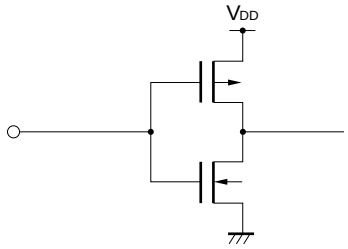
(5) P1A (P1A$_3$, P1A$_2$, P1A$_1$, P1A$_0$)
P2A (P2A$_0$/PWM$_8$)
P2B (P2B$_3$/PWM$_7$, P2B$_2$/PWM$_6$, P2B$_1$/PWM$_5$, P2B$_0$/PWM$_4$)
P2C (P2C$_3$/PWM$_3$, P2C$_2$/PWM$_2$, P2C$_1$/PWM$_1$, P2C$_0$/PWM$_0$)
(Output)



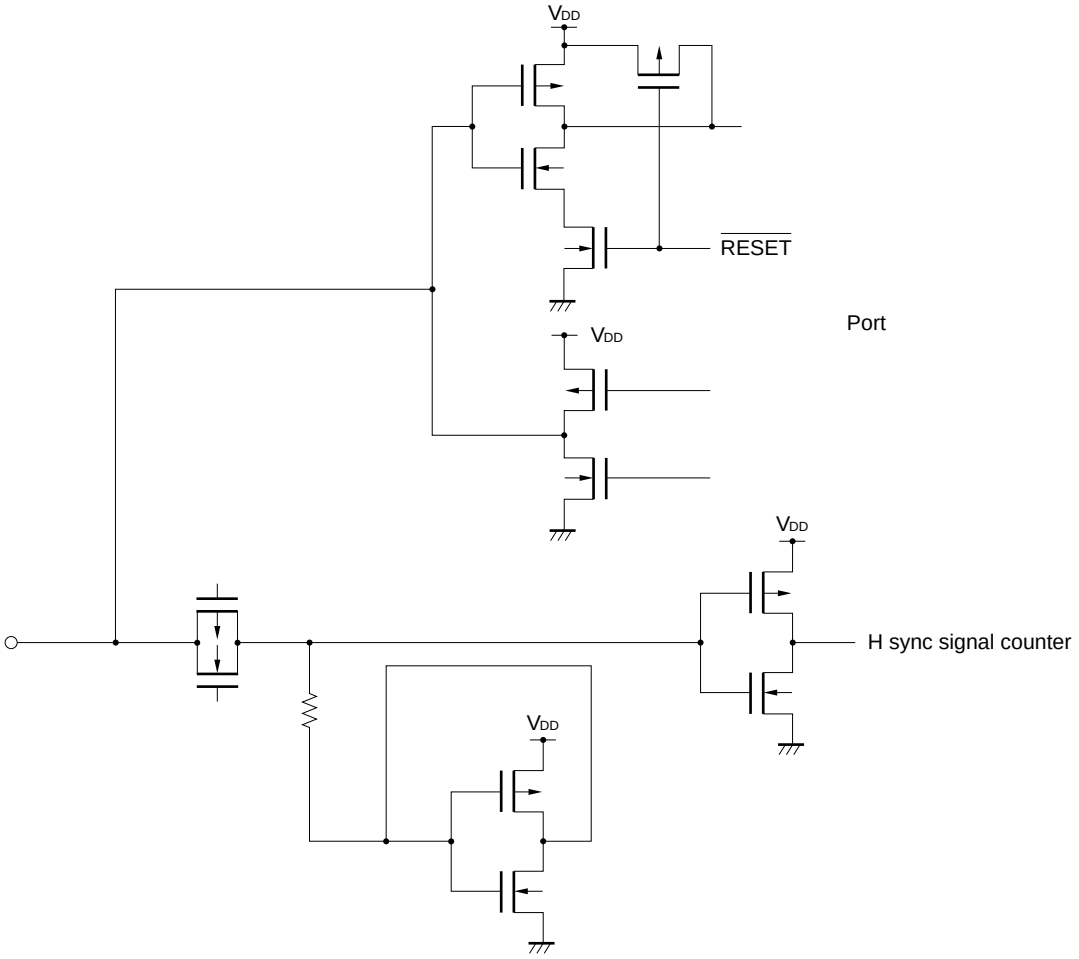
(6) P0D (P0D$_3$/ADC$_4$, P0D$_2$/ADC$_3$, P0D$_1$/ADC$_2$/XT$_{IN}$, P0D$_0$/ADC$_1$/XT$_{OUT}$) : (Input)



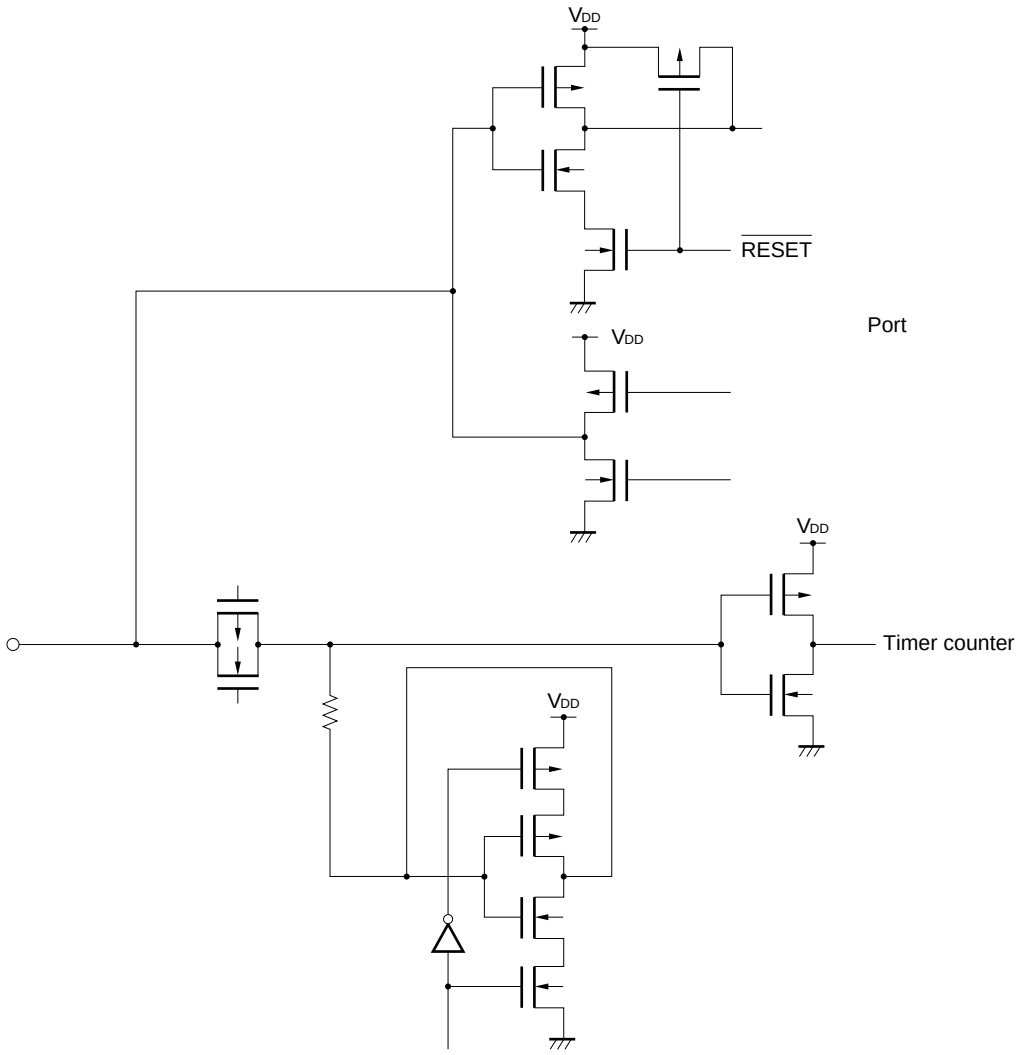
(7) ADC_0 : (Input)



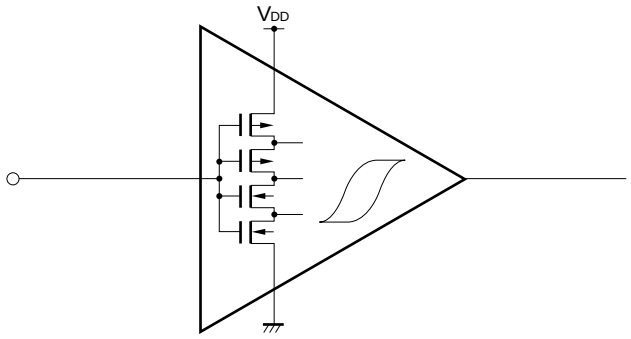
(8) $P0B_3$/HSCNT : (Input/output)



(9) P1B3/TMIN : (Input/output)

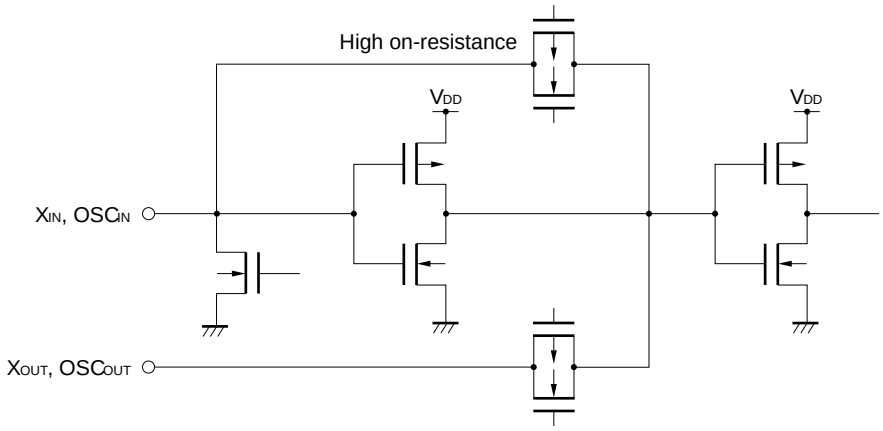


(10) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, CE, INT0, INTNC : (Schmitt triggered input)

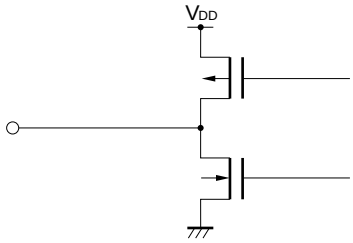


(11) X_{IN}, OSC_{IN} :

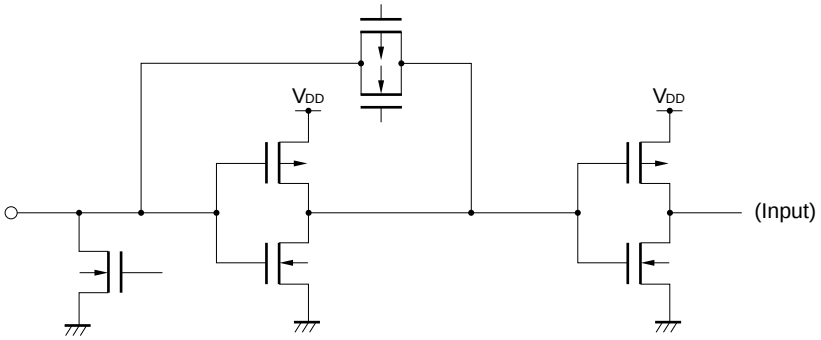
X_{OUT}, OSC_{OUT} :



(12) EO : (Output)



(13) VCO : (Input)



1.4 Handling of Unused Pins

The following are recommended for handling unused pins.

Table 1-1. Handling of Unused Pins (1/2)

(a) Port pins

Pin Name	Input/Output Circuit Type	Recommended Handling when in Unused State
$P0A_0$/SDA $P0A_1$/SCL $P0A_2/\overline{SCK_0}$ $P0A_3/SO_0$	Input/output Note 1	Specify a general-purpose input port by software and connect each pin to V_{DD} or GND through a resistor. Note 2
$P0B_0/SI_0$ $P0B_1$ $P0B_2$/I $P0B_3$/HSCNT		
$P0C_0$-$P0C_3$	CMOS push-pull output	Open
$P0D_0/ADC_1/XT_{OUT}$ $P0D_1/ADC_2/XT_{IN}$ $P0D_2/ADC_3$, $P0D_3/ADC_4$	Input	Individually connect to GND through a resistor. Note 2
$P1A_0$-$P1A_3$	N-ch open-drain output	Specify low-level output by software, then open.
$P1B_0$ $P1B_1$/CKOUT $P1B_2/RLS_{STP}$ $P1B_3$/TMIN	Input/output Note 1	Specify a general-purpose input port by software and connect each pin to V_{DD} or GND through a resistor. Note 2
$P1C_0/ADC_5$-$P1C_2/ADC_7$ $P1C_3$		
$P1D_0$-$P1D_3$	CMOS push-pull output	Open
$P2A_0/PWM_8$	N-ch open-drain output	Specify low-level output by software, then open.
$P2B_0/PWM_4$-$P2B_3/PWM_7$		
$P2C_0/PWM_0$-$P2C_3/PWM_3$		
$P2D_0/\overline{SCK_1}$ $P2D_1/SO_1$ $P2D_2/SI_1$	Input/output Note 1	Specify a general-purpose input port by software and connect each pin to V_{DD} or GND through a resistor. Note 2

Notes 1. Input ports go to input mode when the power supply rises, when the clock stops, and on CE reset.

2. Be careful of the fact that when an external pull-up (connection to V_{DD} through a resistor) or pull-down (connection GND through a resistor) is made, if the pull-up or pull-down is done through a resistor with a high value, because the pin comes near to being in high impedance, the consumed (through) current increases. This also depends on the application circuit, but a typical value for a pull-up or pull-down resistor is a few tens of kΩ.

Table 1-1. Handling of Unused Pins (2/2)

(b) Pins other than ports

Pin Name	Input/Output Circuit Type	Recommended Handling when in Unused State
ADC_0	Input	Connect to V_{DD} or GND through a resistor. **Note**
BLANK	Output	Open
BLUE	Output	Open
CE	Input	Connect to V_{DD} through a resistor. **Note**
EO	Output	Open
GREEN	Output	Open
$\overline{H_{SYNC}}$	Input	Connect to V_{DD} or GND through a resistor. **Note**
INT_0	Input	Connect to V_{DD} or GND through a resistor. **Note**
INT_{NC}	Input	Connect to V_{DD} or GND through a resistor. **Note**
OSC_{IN}	Input	Connect to V_{DD} through a resistor. **Note**
OSC_{OUT}	Output	Open
PSC	Output	Open
RED	Output	Open
VCO	Input with pull-down resistor	Open
$\overline{V_{SYNC}}$	Input	Connect to V_{DD} or GND through a resistor. **Note**

Note Be careful of the fact that when an external pull-up (connection to V_{DD} through a resistor) or pull-down (connection GND through a resistor) is made, if the pull-up or pull-down is done through a resistor with a high value, because the pin comes near to being in high impedance, the consumed (through) current increases. This also depends on the application circuit, but a typical value for a pull-up or pull-down resistor is a few tens of kΩ.

1.5 Notes on Using the CE and INT_{NC} Pins (Only in Normal Operation Mode)

In addition to the functions shown in 1.1 **Normal Operation Mode**, the CE pin also has the function of setting a test mode (for IC testing) in which the internal operations of the μPD17P068 are tested.

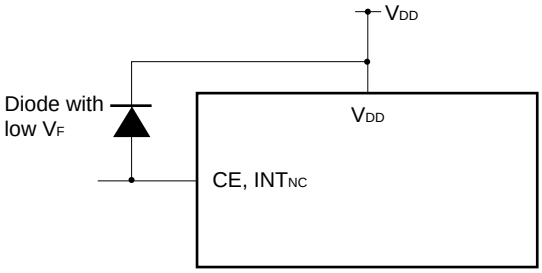
Also, the INT_{NC} pin has the function of the V_{PP} pin for program memory write/verify.

When a voltage higher than V_{DD} is applied to either of these pins, the test or program memory write/verify mode is set. This means that, even during normal operation, the μPD17P068 may be set in the test mode if noise exceeding V_{DD} is applied.

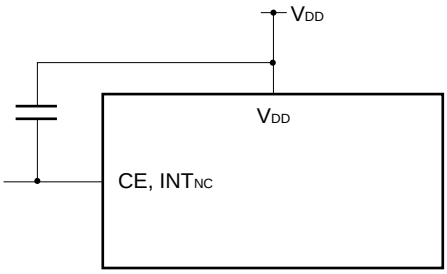
For example, if the wiring length of the CE or INT_{NC} pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- **Connect diode with low V_F between V_{DD} and CE/INT_{NC} pin**



- **Connect capacitor between V_{DD} and CE/INT_{NC} pin**



2. WRITE, READ, AND VERIFY OF ONE-TIME PROM (PROGRAM MEMORY)

The program memory contained in the μPD17P068 is the 12160 × 16-bit one-time PROM that can electrically be written one time only. This PROM is accessed in 16 bits per word in normal operation mode, and in 8 bits per word in write, read, verify modes. The 16 bits of a word in normal mode are divided into higher 8 bits and lower 8 bits which are assigned to even and odd addresses, respectively.

When the PROM is written, read, or verified, set this device into the PROM mode. In this mode, these pins are used as shown in the table below. Notice that no address input pins are provided. Addresses are automatically updated by the clock signal supplied from the CLK pin.

Table 2-1. Pins Used in Program Memory Write, Read, and Verify Modes

Pin	Function
V_{PP}	Programming voltage (+12.5 V) application
CLK	Address update clock input
MD_0-MD_3	Operation mode selection
D_0-D_7	8-bit data input/output
V_{DD0}, V_{DD1}	Power supply voltage (+5 V) application

To write the internal PROM, use the NEC-specified PROM programming equipment (PROM programmer) and program adapter as listed below.

PROM programmer	AF-9703	(Ando Electric Corporation)
	AF-9704	(Ando Electric Corporation)
	AF-9705	(Ando Electric Corporation)
	AF-9706	(Ando Electric Corporation)
Program adapter	AF-9808L	(Ando Electric Corporation)

Remark For details on these PROM programmer and program adapter, consult with Ando Electric Corporation (03-3733-1151 Tokyo, Japan).

2.1 Operation Modes in Program Memory Write/Read/Verify

When +5 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin, this device enters the program memory write/read/verify modes. Operation mode is determined by the setting of MD_0 to MD_3 pins as indicated in the table below.

All input pins irrelevant to the program memory write/read/verify operation should be left unconnected or connected to GND via a pull-down resistor of 470 Ω (Refer to the section "PIN CONFIGURATION (2) PROM programming mode). "

Table 2-2. Operation Modes in Program Memory Write/Read/Verify

Pin States						Operation Mode
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+5 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write
		L	L	H	H	Read, Verify
		H	X	H	H	Program inhibit

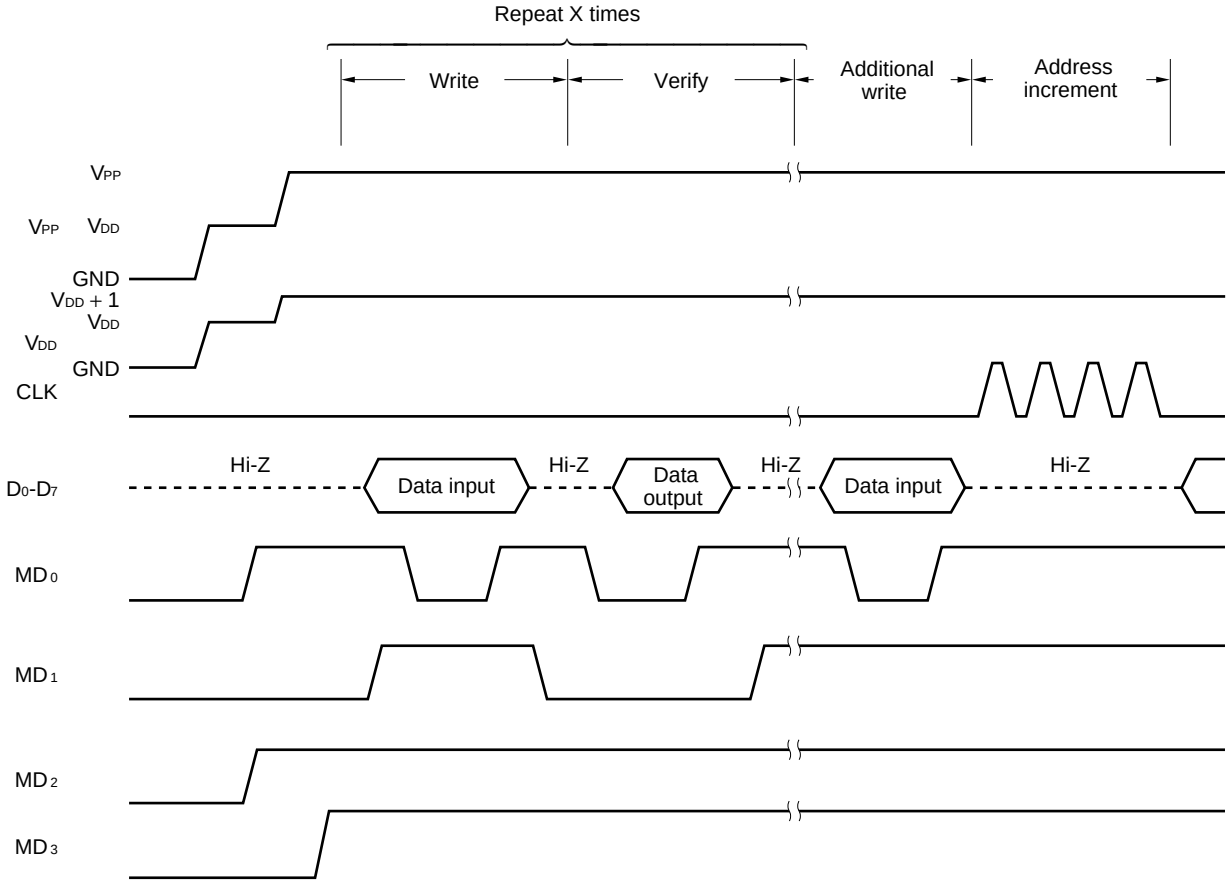
Remark X: L or H

2.2 PROM Write Procedure

Data can be written to the PROM in high speeds by using the following procedures.

(1) Set the pins not used for programming as indicated in section **"PIN CONFIGURATION (2) PROM programming mode."** Set the CLK pin to low level.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Provide a 10-μs wait state.
(4) Program memory address 0 clear mode is entered.
(5) Supply +6 V to the V_{DD} pin, and +12.5 V to the V_{PP} pin.
(6) Program inhibit mode is entered.
(7) Provide write data for 1 ms in write mode.
(8) Program inhibit mode is entered.
(9) Use the verify mode to test data. If the data has been written, proceed to (10). If not, repeat steps (7) to (9).
(10) Provide write data (for additional writing) for 1 ms times the number of repeats performed between steps (7) to (9).
(11) Program inhibit mode is entered.
(12) Provide four pulses to the CLK pin to increment the address.
(13) Repeat steps (7) to (12) until the last address is reached.
(14) Program memory address 0 clear mode.
(15) Supply +5 V to V_{DD} and V_{PP} pins.
(16) Turn off the power for this device.

The procedures from (2) to (12) are illustrated in the chart below.

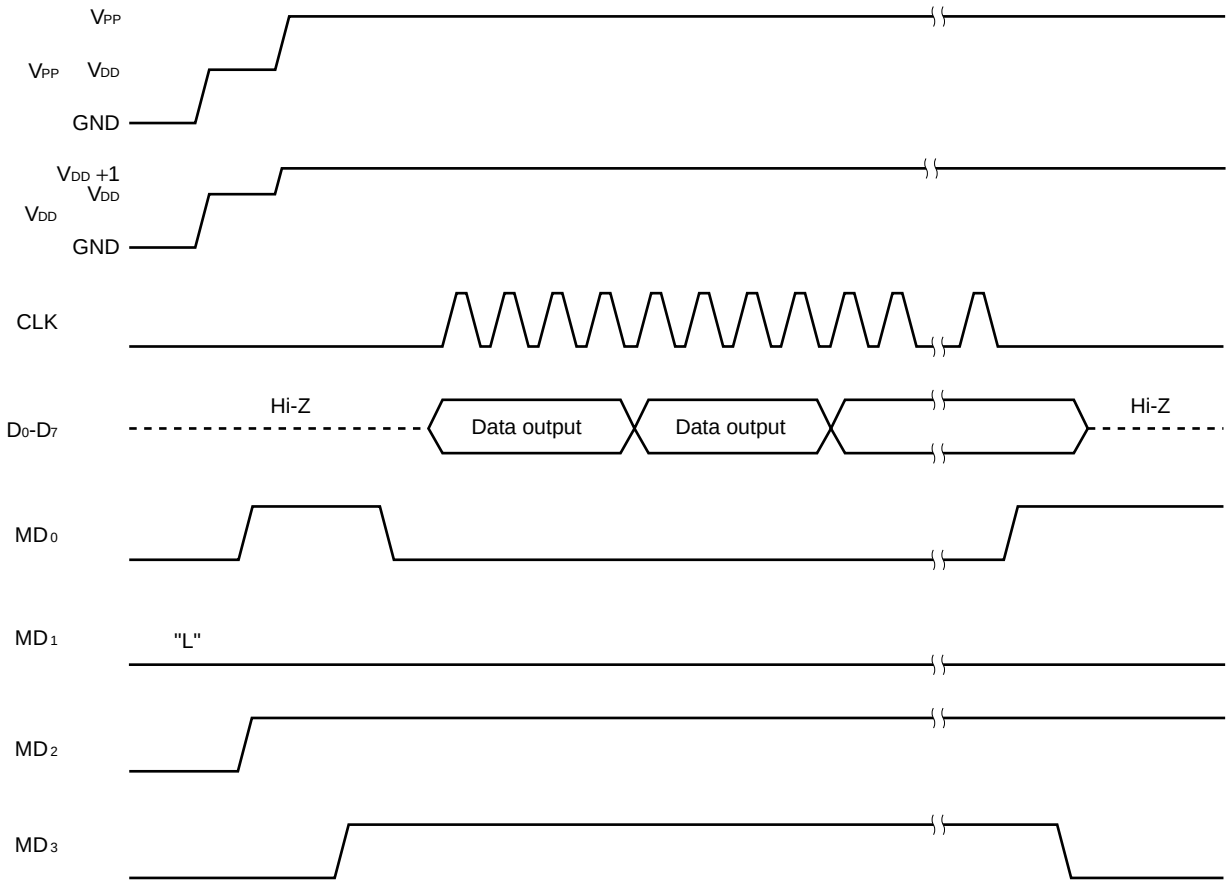


2.3 PROM Read Procedure

Data can be read from the PROM by using the following procedures.

(1) Set the pins not used for programming as indicated in section **"PIN CONFIGURATION (2) PROM programming mode."** Set the CLK pin to low level.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Provide a 10-μs wait state.
(4) Program memory address 0 clear mode is entered.
(5) Supply +6 V to the V_{DD} pin, and +12.5 V to the V_{PP} pin.
(6) Program inhibit mode is entered.
(7) Use the verify mode to output data. Provide clock pulses to the CLK pin to output the data of an address. The address is automatically incremented every four clock pulses. Repeat the four-pulse cycles until the last address is reached.
(8) Program inhibit mode is entered.
(9) Program memory address 0 clear mode.
(10) Supply +5 V to the V_{DD} and V_{PP} pins.
(11) Turn off the power for this device.

The procedures from (2) to (9) are illustrated in the chart below.



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.0	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Except for P1A, P2B, P2C	–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin	–12	mA
		All pins	–20	mA
Low-level output current	I_{OL1}	1 pin (except for P1A)	12	mA
		All pins (except for P1A)	20	mA
	I_{OL2}	1 pin (P1A only)	17	mA
		All pins (P1A only)	60	mA
Output withstand voltage	V_{BDS}	P1A, P2A, P2B, P2C	13	V
Storage temperature	T_{stg}		–55 to +125	°C

Caution Product quality may suffer if the absolute maximum ratings are exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = 25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}		4.5	5.0	5.5	V
	V_{DD2}	Only CPU operates	4.0	5.0	5.5	V
	V_{DD3}	Only watchdog timer operates (CPU stops)	2.3	5.0	5.5	V
Data retention voltage	V_{DDR}	Clock stops	2.3		5.5	V
Output withstand voltage	V_{BDS}	P1A, P2A, P2B, P2C			12.5	V
Supply voltage rise time	t_{rise}	V_{DD} = 0 → 4.5 V	3		500	ms
Input amplitude	V_{IN}	VCO	0.7		5.5	V_{P-P}

DC Characteristics (Reference characteristics: T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	Operation of all functions V_{DD} = 5 V, T_A = 25 °C, f_{VCO} = 20 MHz V_{IN} = 0.7 V_{P-P}, IDC operation OSC_{IN} = 10 MHz, X_{IN} pin square wave input (f_{IN} = 8 MHz, V_{IN} = V_{DD})		11	23	mA
	I_{DD2}	CPU and PLL operation V_{DD} = 5 V, T_A = 25 °C, f_{VCO} = 20 MHz V_{IN} = 0.7 V_{P-P}, X_{IN} pin square wave input (f_{IN} = 8 MHz, V_{IN} = V_{DD})		7	12	mA
	I_{DD3}	Only CPU operates V_{DD} = 5 V, T_A = 25 °C, X_{IN} pin square wave input (f_{IN} = 8 MHz, V_{IN} = V_{DD})		6.5	9	mA
	I_{DD4}	HALT instruction V_{DD} = 5 V, T_A = 25 °C, X_{IN} pin square wave input (f_{IN} = 8 MHz, V_{IN} = V_{DD})		2.5	4.5	mA
Data retention current	I_{DDR1}	Main clock stop, watch timer operation V_{DD} = 2.5 V, T_A = 25 °C		5	10	μA
		Main clock stop, watch timer operation V_{DD} = 5 V, T_A = 25 °C		15	25	μA
	I_{DDR2}	Main clock stop, watch timer operation V_{DD} = 5 V, T_A = 25 °C		2	15	μA
High-level input voltage	V_{IH1}	P0A, P0B, P1B, P1C, P2D	0.7V_{DD}			V
	V_{IH2}	CE, INT_0, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$	0.8V_{DD}			V
	V_{IH3}	P0D	0.7V_{DD}			V
Low-level input voltage	V_{IL1}	P0A, P0B, P0D, P1B, P1C, P2D			0.2 V_{DD}	V
	V_{IL2}	CE, INT_0, INT_{NC}, $\overline{V_{SYNC}}$, $\overline{H_{SYNC}}$			0.2 V_{DD}	V
High-level output current	I_{OH1}	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, P2D, BLANK, RED, GREEN, BLUE, PSC V_{OH} = V_{DD} – 1 V	–1	–5		mA
	I_{OH2}	EO V_{OH} = V_{DD} – 1 V	–1	–2.5		mA
Low-level output current	I_{OL1}	$P0A_2$, $P0A_3$, P0B, P0C, P1B, P1C, P1D, P2D, PSC V_{OL} = 1 V	1	10		mA
	I_{OL11}	BLANK, RED, GREEN, BLUE V_{OL} = 1 V	1	8.5		mA
	I_{OL2}	EO V_{OL} = 1 V	1	6		mA
	I_{OL3}	$P0A_0$, $P0A_1$ V_{OL} = 1 V	1	4.0		mA
	I_{OL4}	PWM (P2A, P2B, P2C) V_{OL} = 1 V	1	1.5		mA
	I_{OL5}	P1A V_{OL} = 1 V	15	30		mA
High-level input current	I_{IH}	VCO V_{IH} = V_{DD}	0.1	0.65	1.3	mA
High-level output leakage	I_{LOH}	P1A, P2A, P2B, P2C V_O = 12.5 V			0.5	μA
Output off leakage current	I_L	EO V_O = V_{DD} or 0 V		$\pm10^{-3}$	±1	μA
Internal pull-down resistor	R_{PD1}	P0D (KEY) V_{IH} = V_{DD}	19	41	85	kΩ
	R_{PD2}	P0D (KEY) V_{IH} = V_{DD} = 5 V	23	41	72	kΩ
	R_{PD3}	P0D (KEY) V_{IH} = V_{DD} = 5 V, T_A = 25 °C	29	41	47	kΩ

AC Characteristics (Reference characteristics: T_A = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency 1	f_{VCO}	VCO square wave input V_{IN} = 0.7 V_{P-P}	0.7		20	MHz
Input frequency 2	f_{TMR}	TMIN ($P1B_3$) Duty 50 %	45		65	Hz
Input frequency 3	f_{HS}	HSCNT ($P0B_3$)	10		20	kHz

A/D Converter Characteristics (Reference characteristics: T_A = –10 to +50 °C, V_{DD} = 5 V ± 10 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A/D conversion absolute accuracy		ADC_0-ADC_7		±1	±1.5	LSB
A/D conversion resolution		ADC_0-ADC_7			6	bit
A/D input impedance		ADC_0-ADC_7	1			MΩ

DC Programming Characteristics (T_A = 25 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	Except for CLK	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	CLK	V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Except for CLK	0		0.3 V_{DD}	V
	V_{IL2}	CLK	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			±10	μA
High-level output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA			1.0	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD_0 = V_{IL}, MD_1 = V_{IH}			30	mA

Cautions 1. V_{PP} must not exceed +13.5 V including overshoot.

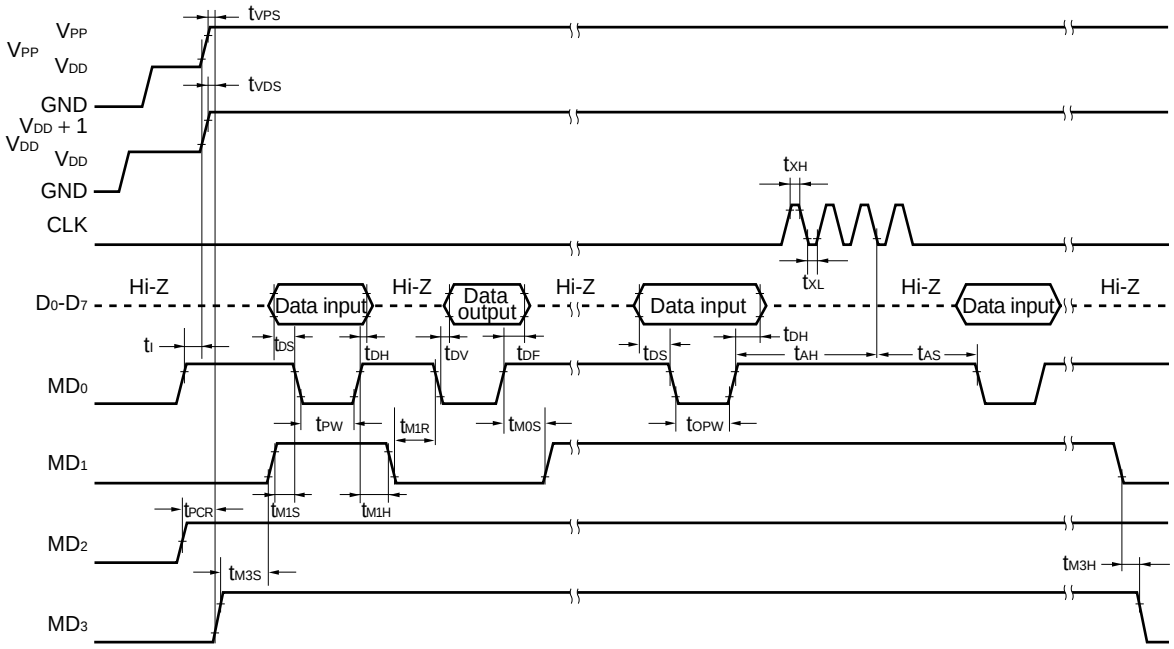
2. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

AC Programming Characteristics (T_A = 25 °C, V_{DD} = 6.0 ± 2.5 V, V_{PP} = 12.5 ± 0.5 V)

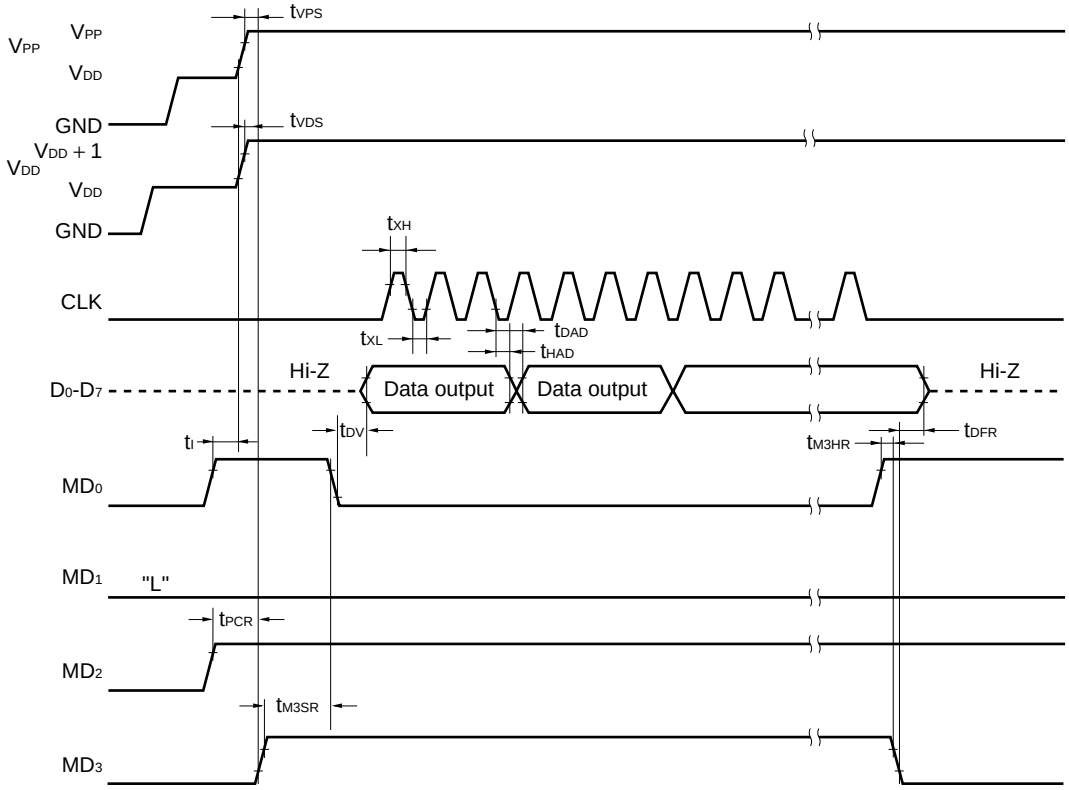
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time Note (vs. MD_0↓)	t_{AS}		2			μs
MD_1 setup time (vs. MD_0↓)	t_{M1S}		2			μs
Data setup time (vs. MD_0↓)	t_{DS}		2			μs
Address hold time Note (vs. MD_0↑)	t_{AH}		2			μs
Data hold time (vs. MD_0↑)	t_{DH}		2			μs
MD_0↑→ data output float delay time	t_{DF}		0		130	ns
V_{PP} setup time (vs. MD_3↑)	t_{VPS}		2			μs
V_{DD} setup time (vs. MD_3↑)	t_{VDS}		2			μs
Initial program pulse width	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}		0.95		21.0	ms
MD_0 setup time (vs. MD_1↑)	t_{M0S}		2			μs
MD_0↓→ data output delay time	t_{DV}	$MD_0 = MD_1 = V_{IL}$			1	μs
MD_1 hold time (vs. MD_0↑)	t_{M1H}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD_1 recovery time (vs. MD_0↓)	t_{M1R}		2			μs
Program counter reset time	t_{PCR}		10			μs
CLK input high-/low-level width	t_{XH}, t_{XL}		0.125			μs
CLK input frequency	f_X				4.19	MHz
Initial mode setting time	t_I		2			μs
MD_3 setup time (vs. MD_1↑)	t_{M3S}		2			μs
MD_3 hold time (vs. MD_1↓)	t_{M3H}		2			μs
MD_3 setup time (vs. MD_0↓)	t_{M3SR}	When program memory is read	2			μs
Address Note → data output delay time	t_{DAD}				2	μs
Address Note → data output hold time	t_{HAD}		0		130	ns
MD_3 hold time (vs. MD_0↑)	t_{M3HR}		2			μs
MD_3↓→ data output float delay time	t_{DFR}				2	μs

Note The internal address increment (+1) is performed on the fall of the 3rd clock, where 4 clocks comprise one cycle. The internal clock is not connected to a pin.

Program Memory Write Timing

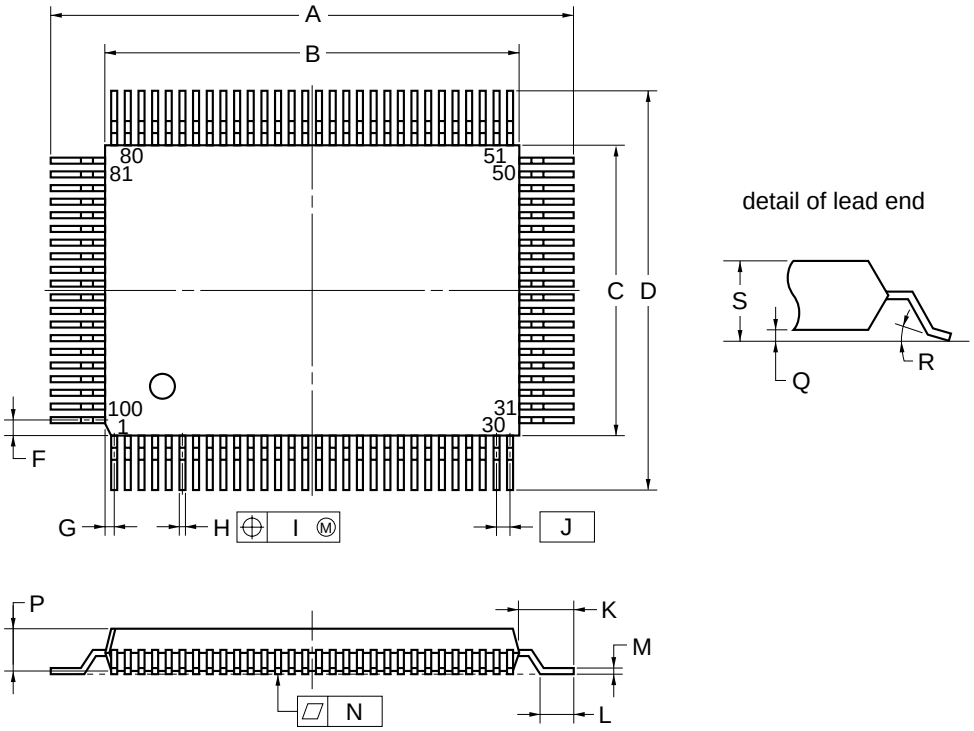


Program Memory Read Timing



4. PACKAGE DRAWING

100 PIN PLASTIC QFP (14×20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S100GF-65-3BA-3

APPENDIX DEVELOPMENT TOOLS

The following tools are available to provide μPD17P068's program development environment.

Hardware

Product	Description
In-circuit emulator (IE-17K IE-17K-ET Note 1 EMU-17K Note 2)	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators common to the 17K series. The IE-17K and IE-17K-ET should be connected with the host computer (PC-9800 series or IBM PC/AT™) through an RS-232-C cable. The EMU-17K should be installed to an extension slot in the host computer (PC-9800 series). Each of the three products function as a dedicated emulator for each device by connecting it with an individual system evaluation board (SE board). Using *SIMPLEHOST*® which features an excellent user-machine interface, makes user's debugging environment more powerful. If the EMU-17K is used, user can monitor the contents of the data memory in real time.
SE board (SE-17008)	This SE board is for the μPD17068, 17P068, and 17008. This board can perform evaluations of user's system. To debug user's programs, use it together with an in-circuit emulator.
Emulation probe (EP-17068GF)	This probe is used when emulating the μPD17P068GF.
Conversion socket (EV-9200GF-100 Note 3)	This socket converts pin arrangement for the 100-pin plastic QFP (14 × 20 mm) to connect the emulation probe EP-17068GF to the target system.
PROM programmer (AF-9703 Note 4 AF-9704 Note 4 AF-9705 Note 4 AF-9706 Note 4)	These products write programs to the internal PROM of the μPD17P068. To perform programming, the program adapter AF-9808L is required to connect to the PROM programmer.
Program adapter (AF-9808L Note 4)	This adapter is used together with the PROM programmer to program the PROM in the μPD17P068.

Notes 1. Inexpensive type: Power supply is required to connect externally.

2. Manufactured by IC Corporation. For details, call 03-3447-3793 Tokyo, Japan.

3. If the EP-17068GF is purchased, one EV-9200GF-100 is attached as a companion product. EV-9200GF-100s can separately be purchased in 5-piece units.

4. Manufactured by Ando Electric Corporation. For details, call 03-3733-1151 Tokyo, Japan.

Software

Product	Description	Host Computer	OS		Media	Ordering Code
17K series assembler (AS17K)	This assembler can be used for all 17K series devices. To develop program of the μPD17P068, the device file (AS17068) are also required.	PC-9800 Series	MS-DOS™		5 inch 2HD	μS5A10AS17K
					3.5 inch 2HD	μS5A13AS17K
		IBM PC/AT DOS™	PC		5 inch 2HC	μS7B10AS17K
					3.5 inch 2HC	μS7B13AS17K
Device file (AS17068)	This product is the device file for the μPD17P068. This device file is used together with the assembler AS17K.	PC-9800 series	MS-DOS		5 inch 2HD	μS5A10AS17068
					3.5 inch 2HD	μS5A13AS17068
		IBM PC/AT	PC DOS		5 inch 2HC	μS7B10AS17068
					3.5 inch 2HC	μS7B13AS17068
Support software (*SIMPLEHOST*)	This software is used to develop programs using an in-circuit emulator and the host computer. This product runs under Windows™ system and provides users with an excellent user-machine interface.	PC-9800 Series	MS-DOS	Windows	5 inch 2HD	μS5A10lE17K
					3.5 inch 2HD	μS5A13lE17K
		IBM PC/AT	PC DOS		5 inch 2HC	μS7B10lE17K
					3.5 inch 2HC	μS7B13lE17K

Remark These products run with the versions of the operation systems shown below.

OS	Version
MS-DOS	Ver.3.30 to Ver.5.00A **Note**
PC DOS	Ver.3.1 to Ver.5.0 **Note**
Windows	Ver.3.0 to Ver.3.1

Note With these products, the task swap function is disabled though the Ver.5.00/5.00A of MS-DOS and Ver.5.0 of the PC DOS support the task swap function.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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