M6759 : 8 Bit MTP Micro-controller

Features

- **8051 instruction set compatible 8 bit micro-controller**
- **8051/8052 compatible pin out**
- **Complete static design, wide range of operation frequency from 1 ~ 40 MHz**
- **Large on-chip memory**
  - ✧ 64K bytes build-in Multiple Times Programming ROM (MTP-ROM) program memory
  - ✧ 512 bytes on-chip SRAM, expandable external 64K bytes address space
- **Four 8-bit bi-directional I/O ports**
- **13 interrupts including 6 external source**
- **One full-duplex serial UART ports compatible with standard 8052**
- **Two 16 bit timer/counter**
- **One 16 bit timer**
- **On chip oscillator for crystal**
- **Software power-down mode, support IDLE mode and STOP mode for less power consumption**
- **ROM Code Protection**
- **4.5V~5.5V operation voltage, 12V programming**
- **44 pin PLCC or QFP package**

General Description

The M6759 is an 8032/8052 instruction compatible 8-bit micro-controller with MTP Flash ROM for firmware updating. By combining a versatile 8-bit CPU with MTP-Flash, this device provides whole micro-controller system on one chip and still remains the feasibility for general control systems in a variety of applications. Further more, the firmware can be protected by user-defined security registers after the code is ready.

ALi M6759 contains the following: a) a non-volatile 64K bytes Multiple Times Programmable ROM program memory. b) a volatile 512 bytes read/write data memory c) four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51). d) a 16-bit timer (identical to the Timer 2 of the 8052). e) a multi-source two-priority-level nested interrupt structure. f) one serial interface (UART) and g) an on-chip oscillator.

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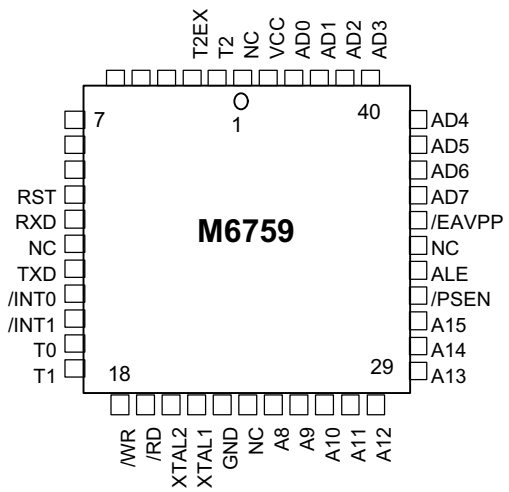
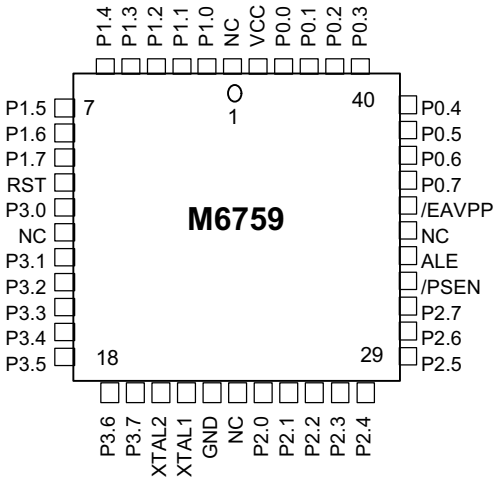
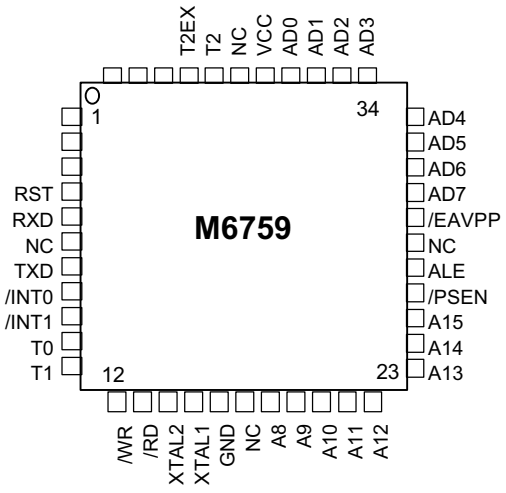
Pin Configuration

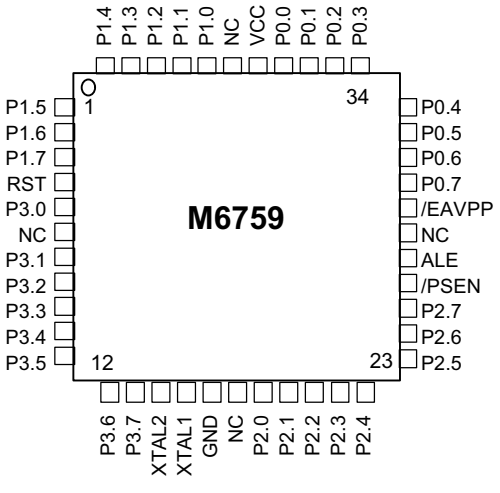
44-pin PLCC Package





44-pin QFP Package





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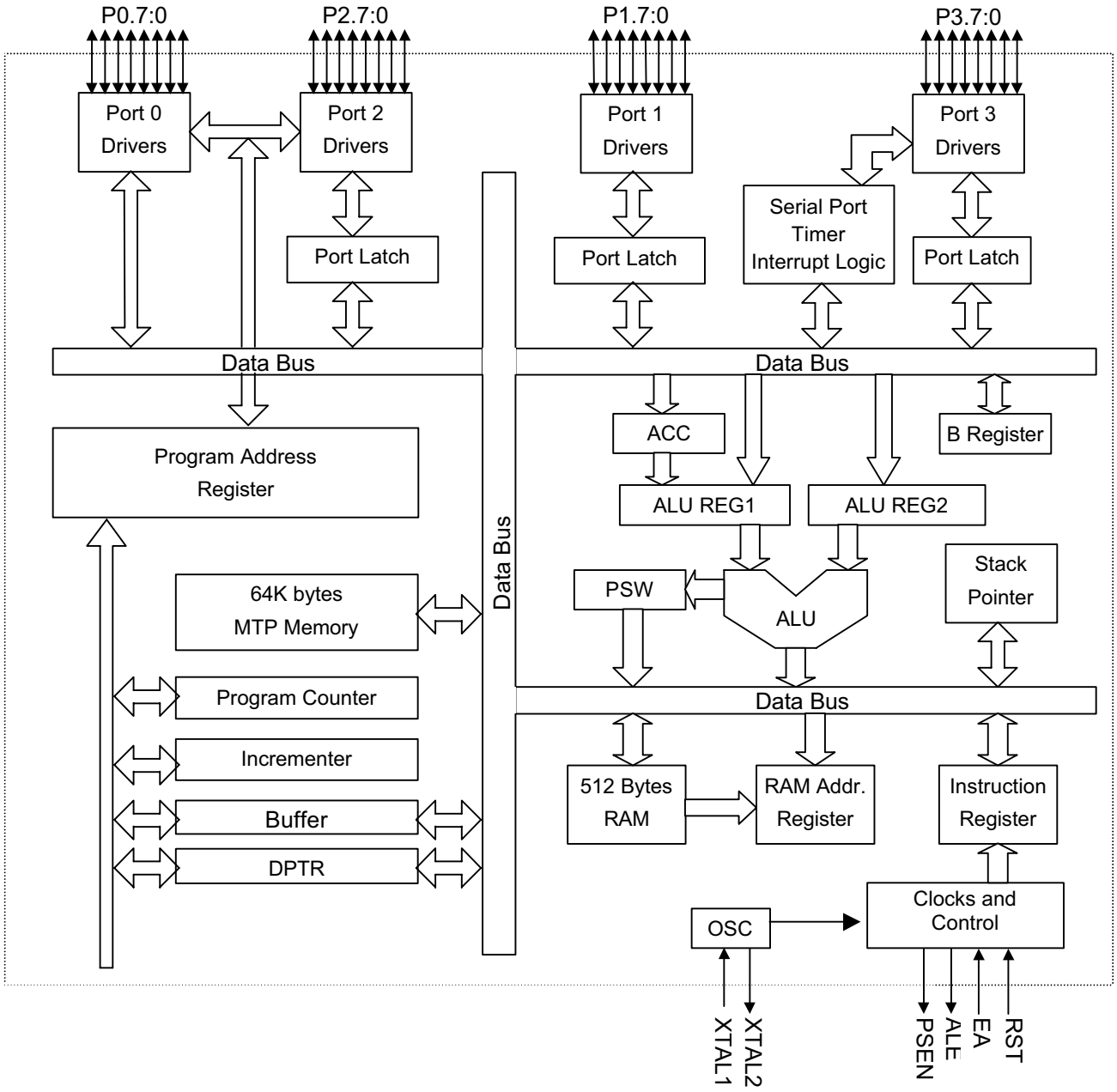
Pin Description

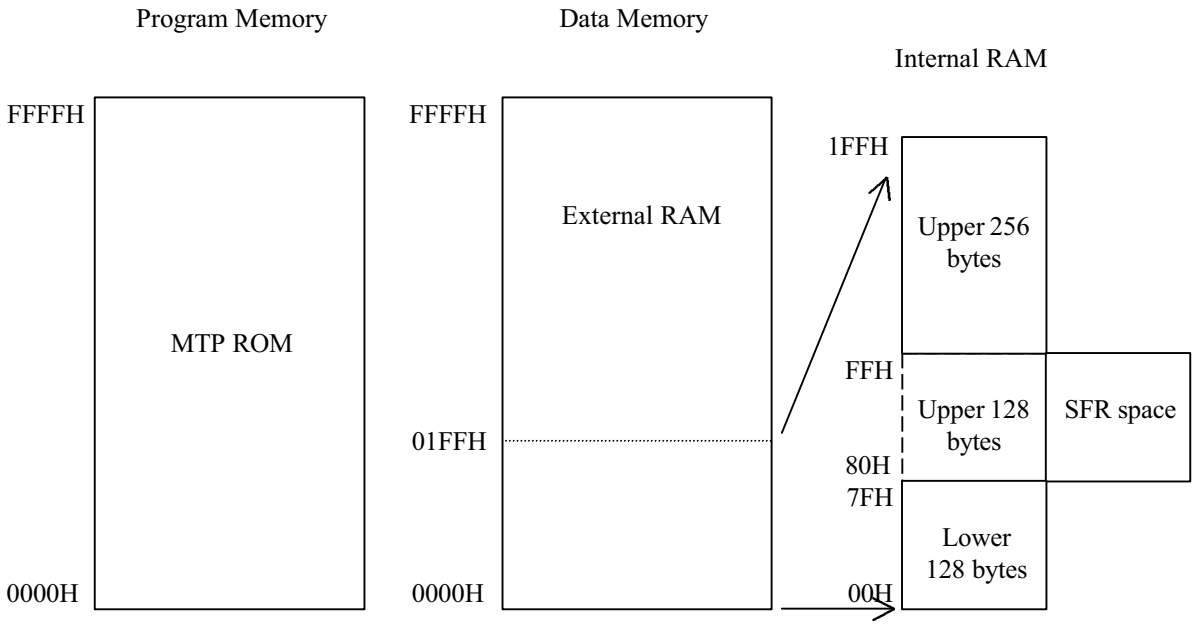
Pin assignments shown below are listed based on 44-pin PLCC package. And if not additionally specified, further pin number reference throughout this document is, by default, referred to 44-pin PLCC package. As for QFP package, the pin number assignment should be shifted accordingly, as shown in Pinout Configuration.

Pin Name	No. (PLCC)	Type	Description
VDD	44	IN	Power supply for internal operation, 5V input.
GND	22	IN	Ground.
P0.7-P0.0	36,37,38,39, 40,41,42, 43	I/O	Port 0 is 8 bits bi-directional I/O port with internal pull high.
AD7-0			Multiplexed address/data bus. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls, the port transitions to a bi-directional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals.
RST	10	IN	Reset signal of internal circuit, it must be kept 4 clocks to ensure being recognized by internal circuit. This signal will not affect internal SRAM.
XTAL1	21	IN	Crystal In, can be used as external clock input.
XTAL2	20	OUT	Crystal out, feedback of XTAL1.
/PSEN	32	OUT	Program Store Enable Output, commonly connected to external ROM memory as a chip enable during fetching and MOVC operation. /PSEN goes high during a reset condition.
ALE	33	OUT	Address Latch Enable, used to latch external LSB 8 bit address bus from multiplexed address/data bus, commonly connect to the latch enable of 373 family. This signal will be forced high when the device is in a reset condition.
P1.7-P1.0	9,8,7,6,5,4,3, 2	I/O	Port 1 is 8 bits bi-directional I/O port with internal pull high. All pins have an alternate function shown as below.
T2EX (P1.1)		IN	External timer/counter 2 trigger.
T2 (P1.0)		IN	External timer/counter 2.
P2.7-P2.0	31,30,29,28, 27,26,25, 24	I/O	Port 2 is 8 bits bi-directional I/O port with internal pull high. The alternate function is MSB 8 bit address bus
A15-A8		OUT	This bus emits the high-order address byte during fetches from external Program Memory or during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.
P3.7-P3.0	19,18,17,16, 15,14,13, 11	I/O	Port 3 is an 8-bit bi-directional I/O port with internal pull high. The reset condition of this port is with all bits at a logic 1. Port 3 also have alternate function list below
/RD (P3.7)		OUT	External data memory read strobe.
/WR (P3.6)		OUT	External data memory write strobe.
T1 (P3.5)		IN	External timer/counter 1.
T0 (P3.4)		IN	External timer/counter 0.
/INT1 (P3.3)		IN	External interrupt 1 (Negative Edge Detect).
/INT0 (P3.2)		IN	External interrupt 0 (Negative Edge Detect).
TXD (P3.1)		OUT	Serial port output.
RXD (P3.0)		IN	Serial port input.
/EAVPP	35	IN	The pin must be externally held low to enable the device to fetch code from external program memory. If /EAVPP is held high, the device executes from internal program memory. /EAVPP is internal latched on reset. This pin also receives the 12V programming voltage (V_{PP}) during FLASH programming.
NC	1,12,23,34	NC	These pins should not be connected for any purpose

Block Diagram

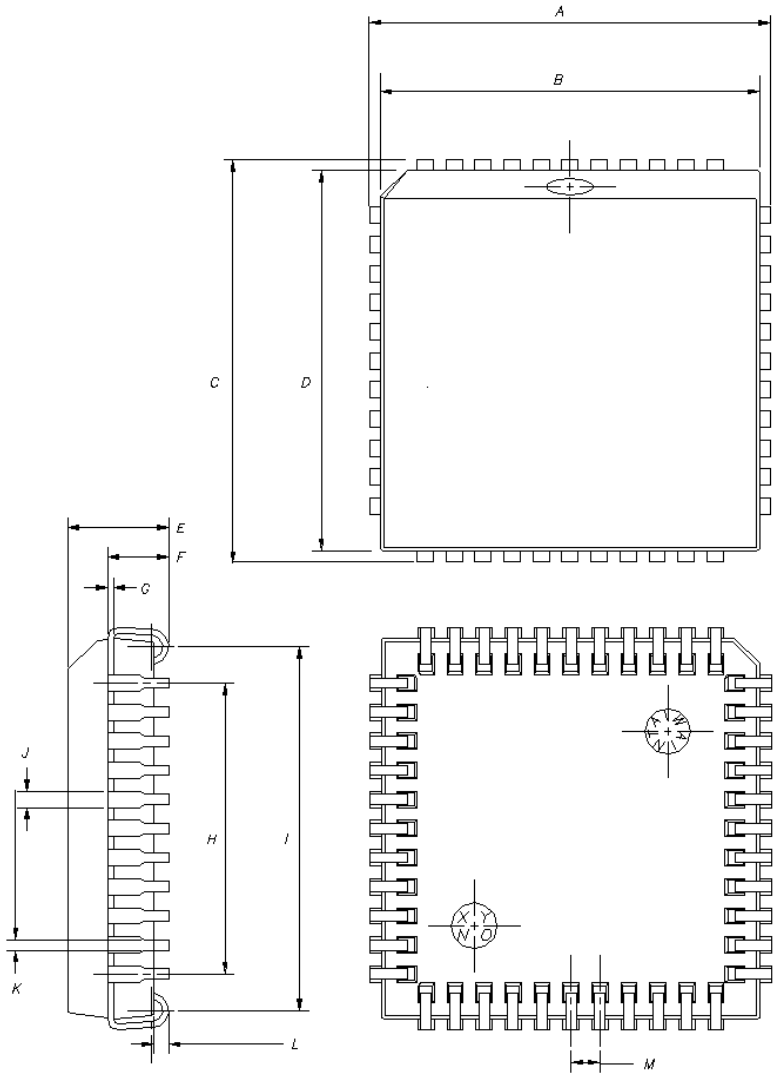


Memory Map


Program Memory
Data Memory
Internal RAM
FFFFH
MTP ROM
0000H
FFFFH
External RAM
01FFH
0000H
1FFH
Upper 256 bytes
FFH
Upper 128 bytes
80H
7FH
Lower 128 bytes
00H
SFR space

Package Information

44-pin PLCC Package



SYMBOL	Dimension in Inches			SYMBOL	Dimension in Inches		
	Min	Typ	Max		Min	Typ	Max
A	0.685	0.690	0.695	**H**	-	0.5	-
B	0.650	0.653	0.656	**I**	0.595	0.610	0.625
C	0.685	0.690	0.695	**J**	0.026	-	0.032
D	0.650	0.653	0.656	**K**	0.013	-	0.021
E	0.168	0.174	0.180	**L**	0.02	-	0.04
F	0.102	0.105	0.108	**M**	0.045	0.05	0.055
G	-	0.010	-				

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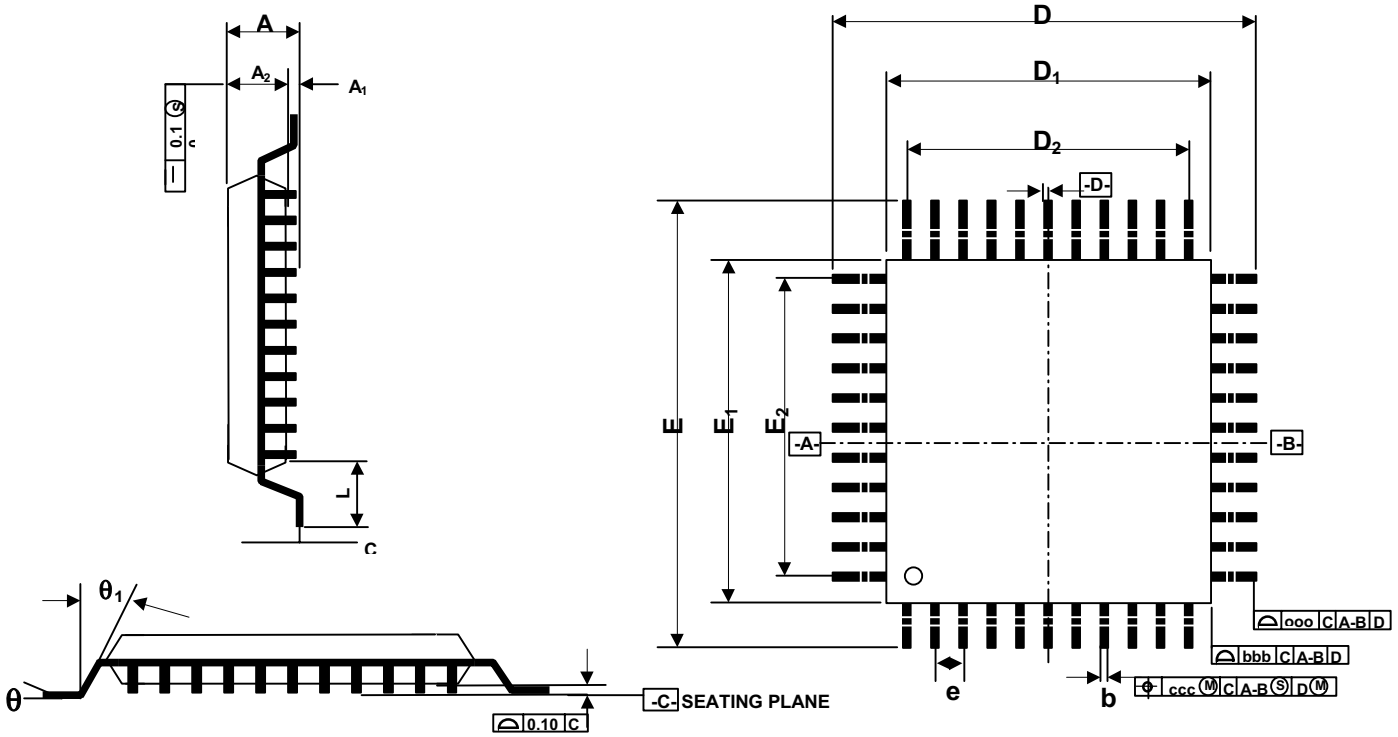
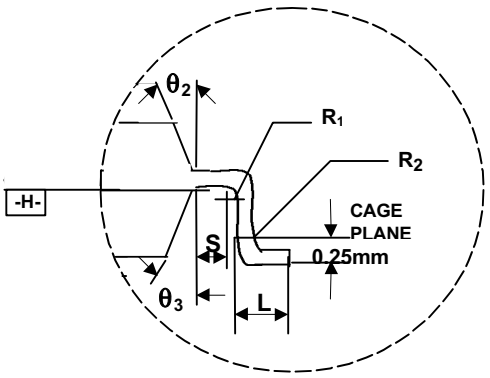
44-pin QFP Package



CONTROL DIMENSIONS ARE IN MILLIMETERS

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.55	-	-	0.100
A_1	0.15	0.25	0.35	0.006	0.010	0.014
A_2	1.90	2.05	2.20	0.075	0.081	0.087
D	13.20 BASIC			0.520 BASIC		
D_1	10.00 BASIC			0.394 BASIC		
E	13.20 BASIC			0.520 BASIC		
E_1	10.00 BASIC			0.394 BASIC		
R_2	0.13	-	0.30	0.005	-	0.012
R_1	0.13	-	-	0.005	-	-
θ	0°	-	7°	0°	-	7°
θ_1	0°	-	-	0°	-	-
θ_2	10° REF			10° REF		
θ_3	7° REF			7° REF		
c	0.10	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.80			0.063		
c	0.10	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L_1	1.80			0.063		
S	0.20	-	-	0.008	-	-



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	8.0			0.315		
E2	8.0			0.315		
ooo	0.25			0.010		
bbb	0.20			0.008		
ccc	-	0.20	-	-	0.008	-

NOTES : 1, DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE (-H-). 2, DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL. IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

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