



# STU/D3055L2

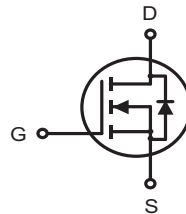
## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### PRODUCT SUMMARY

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
20V	18A	40 @ V <sub>GS</sub> = 10V
		45 @ V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-252 and TO-251 Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Drain Current-Continuous @T <sub>C</sub> =25°C -Pulsed <sup>a</sup>	I <sub>D</sub>	18	A
	I <sub>DM</sub>	30	A
Drain-Source Diode Forward Current	I <sub>S</sub>	15	A
Maximum Power Dissipation @T <sub>C</sub> =25°C	P <sub>D</sub>	50	W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 175	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	3	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	50	°C/W

# STU/D3055L2

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> =25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V			1	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250uA	0.7	1.2	1.8	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =6.0A		25	40	m-ohm
		V <sub>GS</sub> =4.5V, I <sub>D</sub> = 5.2A		30	45	m-ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 4.5V	15			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> =6.0A		7		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =8V, V <sub>GS</sub> = 0V f =1.0MHz		614		pF
Output Capacitance	C <sub>OSS</sub>			151		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			116		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 10V, I <sub>D</sub> = 1A, V <sub>GEN</sub> = 4.5V, R <sub>L</sub> = 10 ohm R <sub>GEN</sub> = 6 ohm		14.3		ns
Rise Time	t <sub>r</sub>			11.9		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			22.1		ns
Fall Time	t <sub>f</sub>			16.7		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =6A, V <sub>GS</sub> =10V		18.9		nC
		V <sub>DS</sub> =10V, I <sub>D</sub> =6A, V <sub>GS</sub> =4.5V		8.9		nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> = 6A, V <sub>GS</sub> =10V		2.1		nC
Gate-Drain Charge	Q <sub>gd</sub>			2.4		nC

# STU/D3055L2

## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 10A$		1	1.3	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

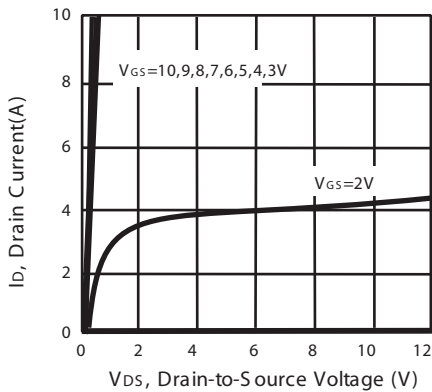


Figure 1. Output Characteristics

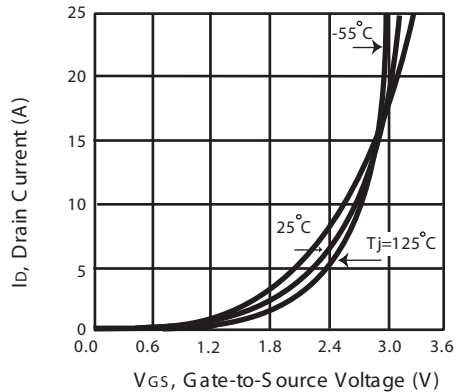


Figure 2. Transfer Characteristics

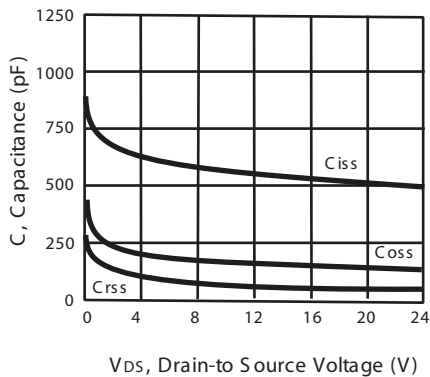


Figure 3. Capacitance

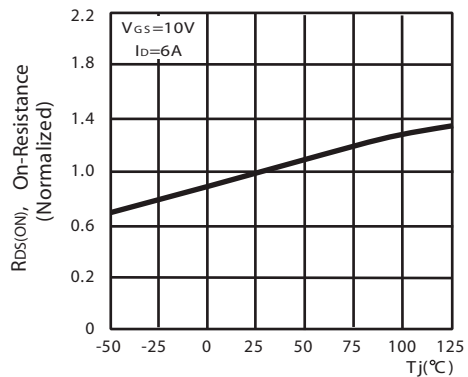


Figure 4. On-Resistance Variation with Temperature

# STU/D3055L2

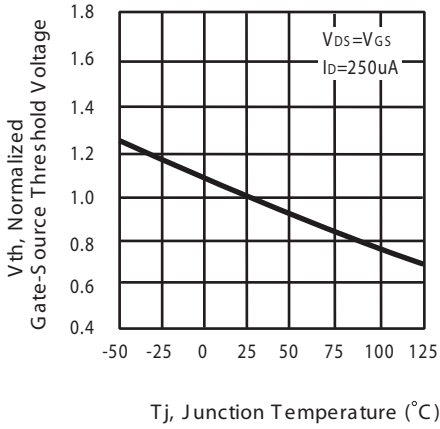


Figure 5. Gate Threshold Variation with Temperature

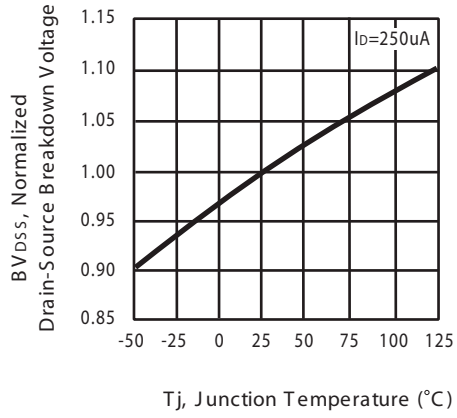


Figure 6. Breakdown Voltage Variation with Temperature

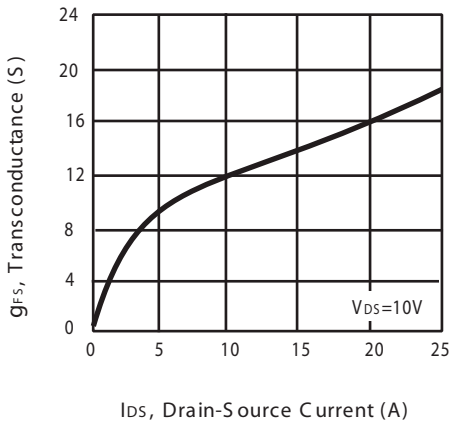


Figure 7. Transconductance Variation with Drain Current

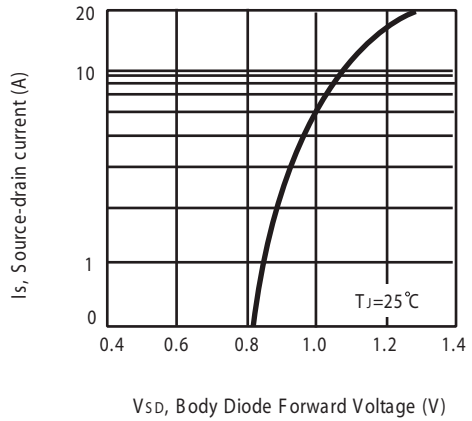


Figure 8. Body Diode Forward Voltage Variation with Source Current

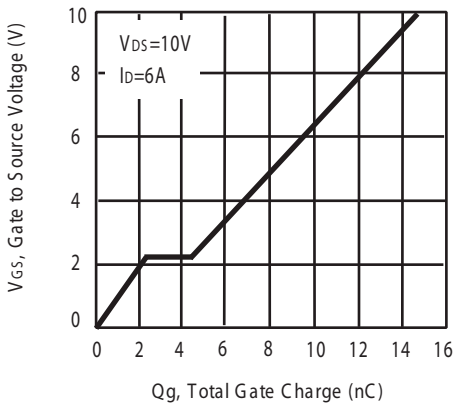


Figure 9. Gate Charge

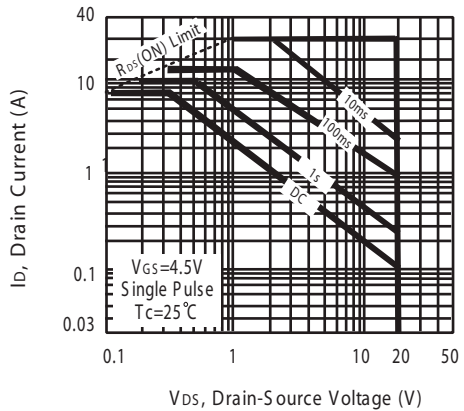


Figure 10. Maximum Safe Operating Area

# STU/D3055L2

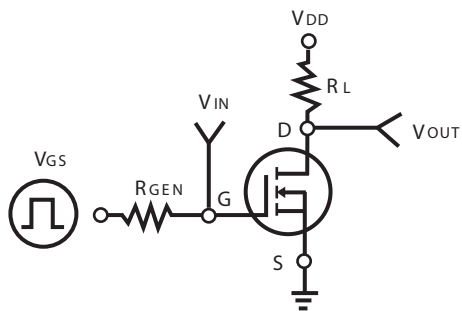


Figure 11. Switching Test Circuit

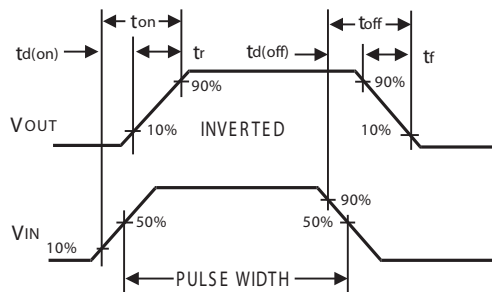


Figure 12. S Switching Waveforms

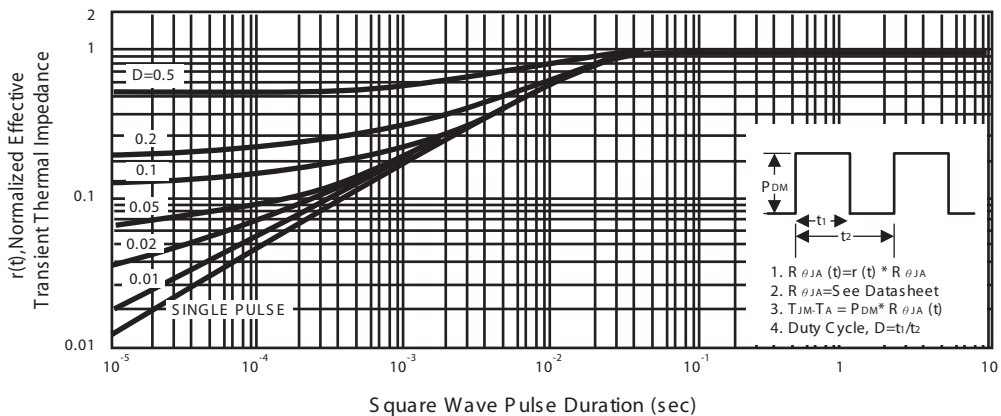
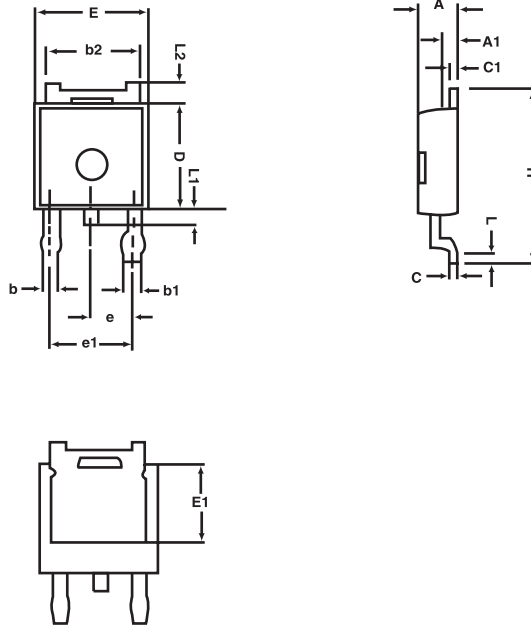


Figure 13. Normalized Thermal Transient Impedance Curve

# STU/D3055L2

## PACKAGE OUTLINE DIMENSIONS

### TO-252

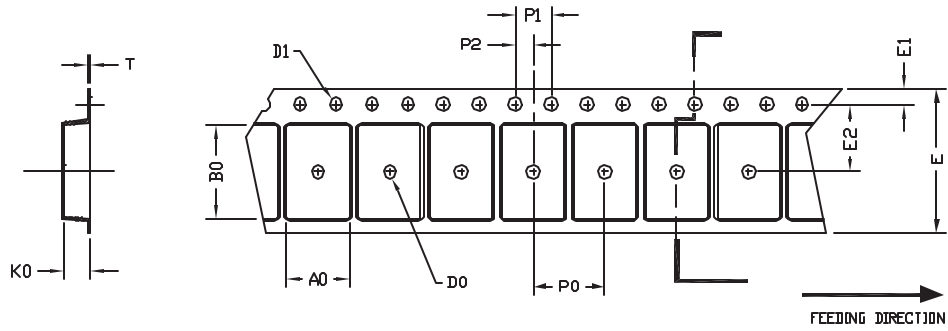


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.25	2.35	0.089	0.093
A1	0.95	1.05	0.037	0.041
b	0.77	0.85	0.030	0.033
b1	0.84	0.94	0.033	0.037
b2	5.30	5.45	0.209	0.215
C	0.49	0.53	0.019	0.021
D	6.00	6.20	0.236	0.244
E	6.40	6.60	0.252	0.260
E1	3.18	3.67	0.125	0.145
e	2.29	BSC	0.090	BSC
H	9.70	10.10	0.382	0.398
L	1.425	1.625	0.056	0.064
L1	0.650	0.850	0.026	0.033
L2	0.600	REF.	0.024	REF.

# STU/D3055L2

## TO-252 Tape and Reel Data

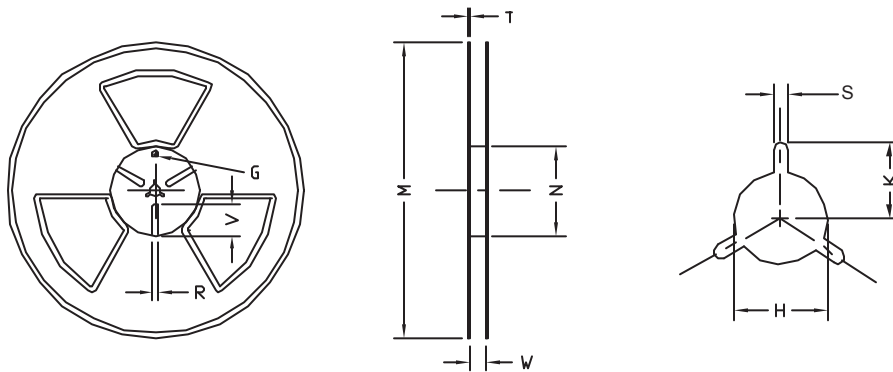
### TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.80 ±0.1	10.3 ±0.1	2.50 ±0.1	φ 2	φ 1.5 + 0.1 - 0	16.0 0.3±	1.75 0.1±	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

### TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---