



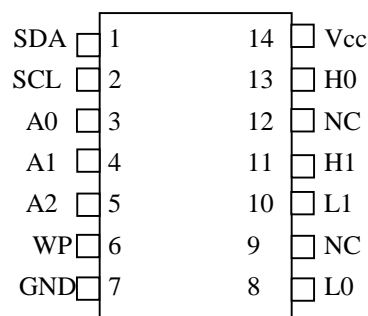
DS1848

Dual Temperature-Controlled NV Variable Resistor & Memory

www.dalsemi.com

FEATURES

- Two linear taper, temperature-controlled variable resistors
 - One 50 k Ω , 256 position
 - One 10 k Ω , 256 position
- Resistor settings changeable every 2°C
- Access to temperature data and device control via a 2-wire interface
- Operates from 3V or 5V supplies
- Packaging: 14-pin TSSOP, 16-ball STPBGA
- Operating temperature: -40°C to +95°C
- Programming temperature: 0°C to +70°C
- 128 bytes of user EEPROM



14-Pin TSSOP (173 mil)

16-BALL STPBGA (4x4 mm)

See Mech. Drawing Section

PIN DESCRIPTION

V _{CC}	-	3V or 5V Power Supply Input
GND	-	Ground
SDA	-	2-wire Serial Data Input/Output
SCL	-	2-wire Serial Clock Input
H0, H1	-	High-End of Resistor
L0, L1	-	Low-End of Resistor
WP	-	Write Protect
A0, A1, A2	-	Address Lines

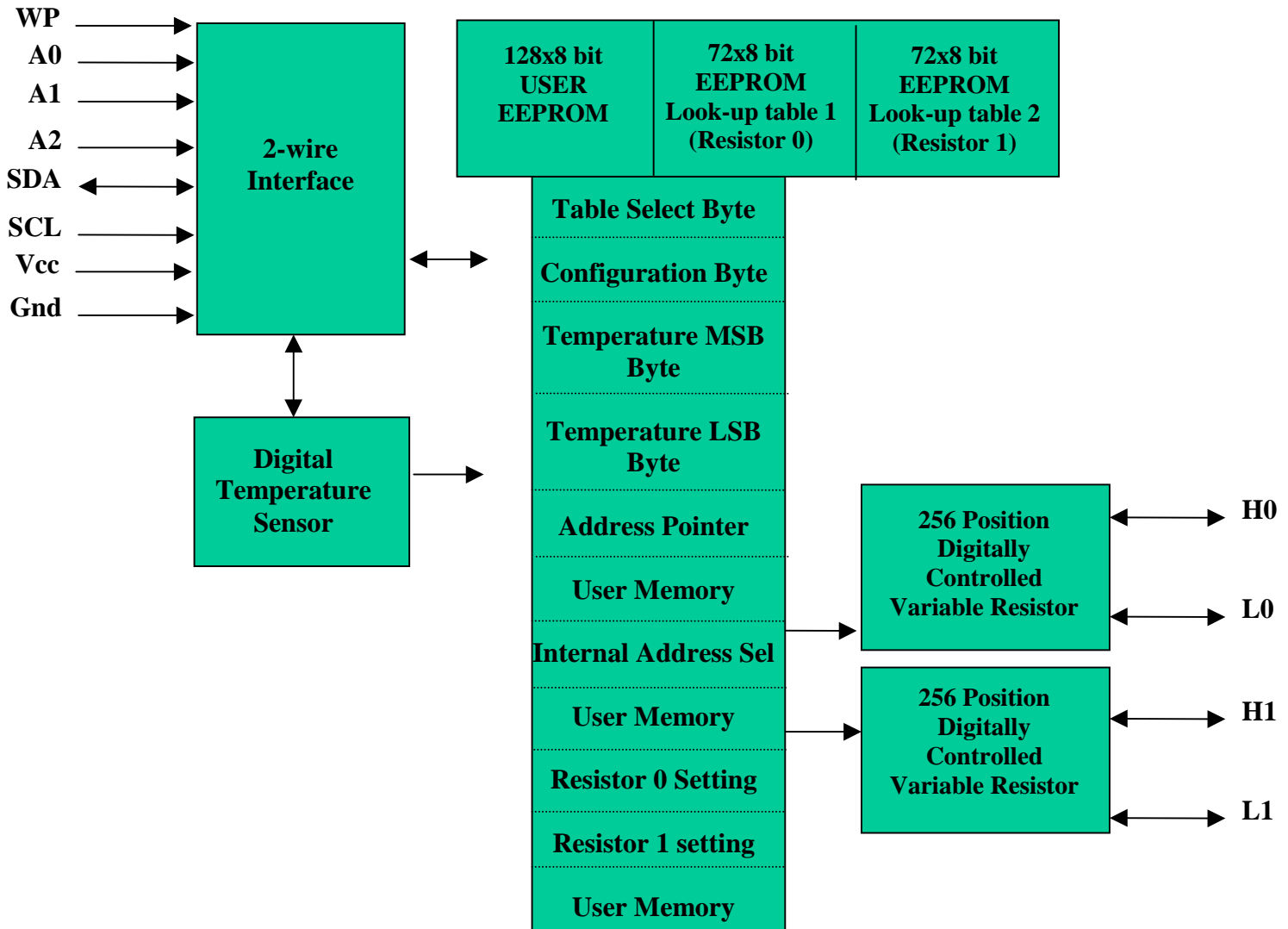
OVERVIEW

The DS1848 Dual Temperature-Controlled NV Variable Resistor consists of one 50 k Ω , 256-position linear, variable resistor, one 10 k Ω , 256-position linear, variable resistor, and a Direct-to-Digital Temperature Sensor. The device provides an ideal method for setting and temperature-compensating bias voltages and currents in control applications using a minimum of circuitry.

The variable resistors settings are stored in EEPROM memory and can be accessed over the industry standard 2-wire serial bus. The value of each variable resistor is determined by a temperature-addressed look-up table, which can assign a unique value to each resistor for every 2°C increment over the -40°C to +95°C range. The output of the digital temperature sensor is also available as a 13-bit, 2's complement value over the serial bus. The interface I/O pins consist of SDA and SCL.

DS1848 BLOCK DIAGRAM

Figure 1



PIN DESCRIPTIONS

V_{CC} - Power Supply Terminal. The DS1848 will support supply voltages ranging from +2.7 to +5.5 volts.

GND - Ground Terminal.

SDA - 2-wire serial data interface. The serial data pin is for serial data transfer to and from the DS1848. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces.

SCL - 2-wire serial clock interface. The serial clock input is used to clock data into the DS1848 on rising edges and clock data out on falling edges.

H0, H1 – These are the high-end terminals of the variable resistors. For both resistors, it is not required that these terminals be connected to a potential greater than the low-end terminal of the corresponding resistor. Voltage applied to the high-end of the resistors cannot exceed the power supply voltage, V_{CC} , or go below ground.

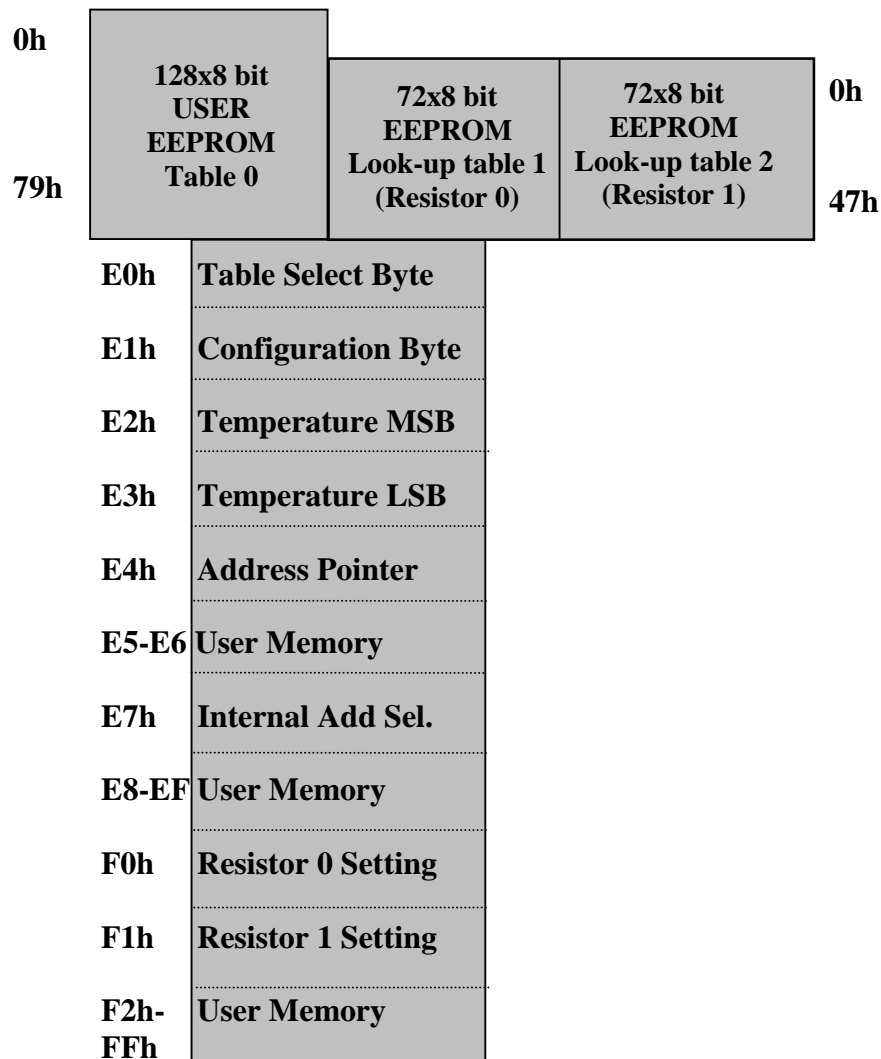
L0, L1 – These are the low-end terminals of the variable resistors. For both resistors, it is not required that these terminals be connected to a potential less than the high-end terminal of the corresponding resistor. Voltage applied to the low-end of the resistors cannot exceed the power supply voltage, V_{CC} , or go below ground.

WP - Write Protect. Write Protect must be connected to GND before either the data in memory or potentiometer wiper settings may be changed. Write Protect is pulled high internally and must be either left open or connected to V_{CC} if write protection is desired.

A0, A1, A2 - Address Inputs. These input pins specify the address of the device when used in a multi-dropped configuration. Up to eight individual DS1848s may be addressed on a single 2-wire bus.

NC - No Connect.

Memory Organization



Memory Location	Name of Location	Function of Location				
00h to 47h	User Defined Look-up Table	This block contains the user defined temperature settings of the resistors. Values between 00h and FFh can be written to either table to set the 256 position variable resistors. The first address location, 00h, is used to set the resistor at -40°C . Each successive memory location will contain the resistor setting for the previous temperature $+2^{\circ}\text{C}$. For example, memory address 01h is the address that will set the resistor in a -38°C environment.				
00h to 79h	User Memory	This block is for general purpose user memory.				
E0h	Table Select Byte	Writing to this byte determines if one of the two 72x8 EEPROM look-up tables or the user EEPROM memory is selected for reading or writing. 00h (User EEPROM selected) 01h (Table 1 selected) 02h (Table 2 selected)				
E1h	Configuration Byte	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="width: 40px; height: 20px;"></td> <td style="width: 30px; text-align: center;">TAU</td> <td style="width: 30px; text-align: center;">TEN</td> <td style="width: 30px; text-align: center;">AEN</td> </tr> </table> <p>TAU – Temperature/Address Update TEN – Temperature Update Enable AEN – Address Update Enable</p> <p>DEFAULT setting is 03h, TAU = 1, TEN = 1 and AEN = 1.</p> <p>TAU becomes a 1 after a temperature and address update has occurred as a result of a temperature conversion. The user can write this bit to 0 and check for a transition from 0 to 1 in order to verify that a conversion has occurred.</p> <p>If TEN = 0, the temperature conversion feature is disabled. The user sets the resistor in “manual mode” by writing to addresses F0h and F1h to control resistors 0 and 1 respectively.</p> <p>With AEN = 0 the user can operate in a test mode. Address updates made from the temperature sensor will cease. The user can load a memory location into E4h and verify that the values in locations F0h and F1h are the expected user defined values.</p>		TAU	TEN	AEN
	TAU	TEN	AEN			

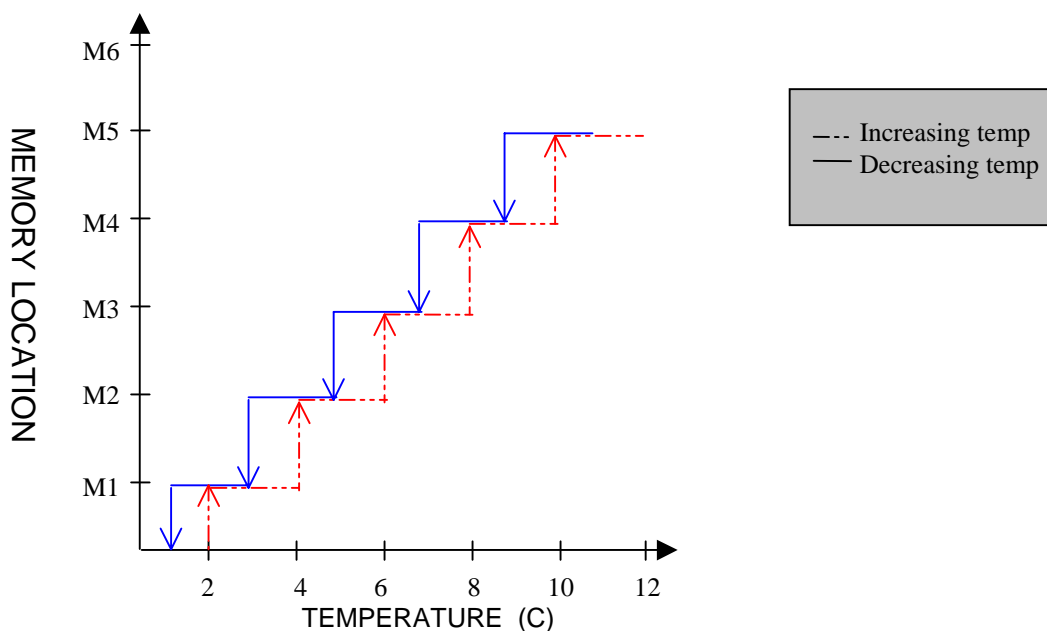
Memory Location	Name of Location	Function of Location								
E2h	Temperature MSB	This byte contains the MSB of the 13-bit 2's complement temperature output from the temperature sensor. <div style="border: 1px solid black; padding: 2px; display: inline-block;"> <table style="border-collapse: collapse;"> <tr> <td style="padding: 0 5px;">S</td> <td style="padding: 0 5px;">2⁷</td> <td style="padding: 0 5px;">2⁶</td> <td style="padding: 0 5px;">2⁵</td> <td style="padding: 0 5px;">2⁴</td> <td style="padding: 0 5px;">2³</td> <td style="padding: 0 5px;">2²</td> <td style="padding: 0 5px;">2¹</td> </tr> </table> </div>	S	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹
S	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹			
E3h	Temperature LSB	This byte contains the LSB of the 13-bit 2's complement temperature output from the temperature sensor. <div style="border: 1px solid black; padding: 2px; display: inline-block;"> <table style="border-collapse: collapse;"> <tr> <td style="padding: 0 5px;">2⁰</td> <td style="padding: 0 5px;">2⁻¹</td> <td style="padding: 0 5px;">2⁻²</td> <td style="padding: 0 5px;">2⁻³</td> <td style="padding: 0 5px;">2⁻⁴</td> <td style="padding: 0 5px;">X</td> <td style="padding: 0 5px;">X</td> <td style="padding: 0 5px;">X</td> </tr> </table> </div>	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	X	X	X
2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	X	X	X			
E4h	Address Pointer	Calculated, current resistor address (0h – 47h). The user-defined resistor setting at this location in the respective look-up table will be loaded into F0h and F1h to set the two resistors.								
E5h to E6h	User Memory	General purpose user memory								
E7h	Address Select	Internal or External device address select. This byte allows the user to use the external address pins or an internal register location to determine the device address. <div style="border: 1px solid black; padding: 2px; display: inline-block; margin: 10px 0;"> <table style="border-collapse: collapse;"> <tr> <td style="width: 100px; height: 20px;"></td> <td style="padding: 0 5px;">A2</td> <td style="padding: 0 5px;">A1</td> <td style="padding: 0 5px;">A0</td> <td style="padding: 0 5px;">$\overline{\text{ENB}}$</td> </tr> </table> </div> <p>ENB = 0 and external A2, A1, A0 grounded, device will use internal address bits (A2, A1, A0) in this register</p> <p>ENB = 1, external A2, A1, A0 = any setting, device will use external address pins</p> <p>DEFAULT setting is 01h. The device uses external pins to determine its address.</p>		A2	A1	A0	$\overline{\text{ENB}}$			
	A2	A1	A0	$\overline{\text{ENB}}$						
E8h to EFh	User Memory	General purpose user memory								
F0h	Resistor 0 Setting	In the user-controlled setting mode, this block contains the resistor 0 setting.								
F1h	Resistor 1 Setting	In the user-controlled setting mode, this block contains the resistor 1 setting.								
F2h to FFh	User memory	General purpose user memory								

Temperature Conversion

The direct-to-digital temperature sensor measures temperature through the use of an on-chip temperature measurement technique with an operating range from -40°C to $+95^{\circ}\text{C}$. Temperature conversions are initiated upon power-up, and the most recent result is stored in address locations E2h and E3h, which are updated every 10 milliseconds. Temperature conversion will not occur during an active read or write to memory.

The value of each resistor is determined by the temperature-addressed look-up table that assigns a unique value to each resistor for every 2°C increment with a 1°C hysteresis at a temperature transition over the operating temperature range. This can be seen in Figure 2.

Figure 2



Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL low time periods. Data changes during SCL high periods will indicate a start or stop conditions depending on the conditions discussed below. Refer to the timing diagram Figure 2 for further details.

Start Condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command. Refer to the timing diagram Figure 2 for further details.

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command places the DS1848 into a low-power mode. Refer to the timing diagram Figure 2 for further details.

Acknowledge: All address and data byte are transmitted via a serial protocol. The DS1848 pulls the SDA line low during the ninth clock pulse to acknowledge that it has received each word.

Standby Mode: The DS1848 features a low-power mode that is automatically enabled after power-on, after a stop command, and after the completion of all internal operations.

2-Wire Interface Reset: After any interruption in protocol, power loss, or system reset, the following steps reset the DS1848.

1. Clock up to nine cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition while SDA is high.

Device Addressing: The DS1848 must receive an 8-bit device address word following a start condition to enable a specific device for a read or write operation. The address word is clocked into the DS1848 MSB to LSB. The address word consists of Ah (1010) followed by A2, A1, and A0 then the R/W (READ/WRITE) bit. If the R/W bit is high, a read operation is initiated. If the R/W bit is low, a write operation is initiated. For a device to become active, the values of A2, A1 and A0 must be the same as the hard-wired address pins on the DS1848. Upon a match of written and hard-wired addresses, the DS1848 will output a zero for one clock cycle as an acknowledge. If the address does not match the DS1848 returns to a low-power mode.

Write Operations: After receiving a matching address byte with the R/W bit set low, the device goes into the write mode of operation. The master must transmit an 8-bit EEPROM memory address to the device to define the address where the data is to be written. After the reception of this byte, the DS1848 will transmit a zero for one clock cycle to acknowledge the receipt of the address. The master must then transmit an 8-bit data word to be written into this address. The DS1848 will again transmit a zero for one clock cycle to acknowledge the receipt of the data. At this point the master must terminate the write operation with a stop condition. The DS1848 then enters an internally timed write process T_w to the EEPROM memory. All inputs are disabled during this byte write cycle.

The DS1848 is capable of an 8-byte page write. A page write is initiated the same way as a byte write, but the master does not send a stop condition after the first byte. Instead, after the slave acknowledges receipt of the data byte, the master can send up to seven more bytes using the same nine-clock sequence. The master must terminate the write cycle with a stop condition or the data clocked into the DS1848 will not be latched into permanent memory.

Acknowledge Polling: Once the internally-timed write has started and the DS1848 inputs are disabled, acknowledge polling can be initiated. The process involves transmitting a start condition followed by the device address. The R/W bit signifies the type of operation that is desired. The read or write sequence will only be allowed to proceed if the internal write cycle has completed and the DS1848 responds with a zero.

Read Operations: After receiving a matching address byte with the R/W bit set high, the device goes into the read mode of operation. There are three read operations: current address read, random read and sequential address read.

CURRENT ADDRESS READ

The DS1848 has an internal address register that maintains the address used during the last read or write operation, incremented by one. This data is maintained as long as V_{CC} is valid. If the most recent address was the last byte in memory, then the register resets to the first address. This address stays valid between operations as long as power is available.

Once the device address is clocked in and acknowledged by the DS1848 with the R/W bit set to high, the current address data word is clocked out. The master does not respond with a zero, but does generate a stop condition afterwards.

RANDOM READ

A random read requires a dummy byte write sequence to load in the data word address. Once the device and data address bytes are clocked in by the master, and acknowledged by the DS1848, the master must generate another start condition. The master now initiates a current address read by sending the device address with the read/write bit set high. The DS1848 will acknowledge the device address and serially clocks out the data byte.

SEQUENTIAL ADDRESS READ

Sequential reads are initiated by either a current address read or a random address read. After the master receives the first data byte, the master responds with an acknowledge. As long as the DS1848 receives this acknowledge after a byte is read, the master may clock out additional data words from the DS1848. After reaching address FFh, it resets to address 00h.

The sequential read operation is terminated when the master initiates a stop condition. The master does not respond with a zero.

For a more detailed description of 2-wire theory of operation, refer to the following section.

2-WIRE SERIAL PORT OPERATION

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1848 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The following I/O terminals control the 2-wire serial port: SDA, SCL, A0, A1, A2. Timing diagrams for the 2-wire serial port can be found in Figures 2 and 3. Timing information for the 2-wire serial port is provided in the AC Electrical Characteristics table for 2-wire serial communications.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 2 and 3 detail how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9th bit.

Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1848 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The master transmits the 1st byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1848 may operate in the following two modes:

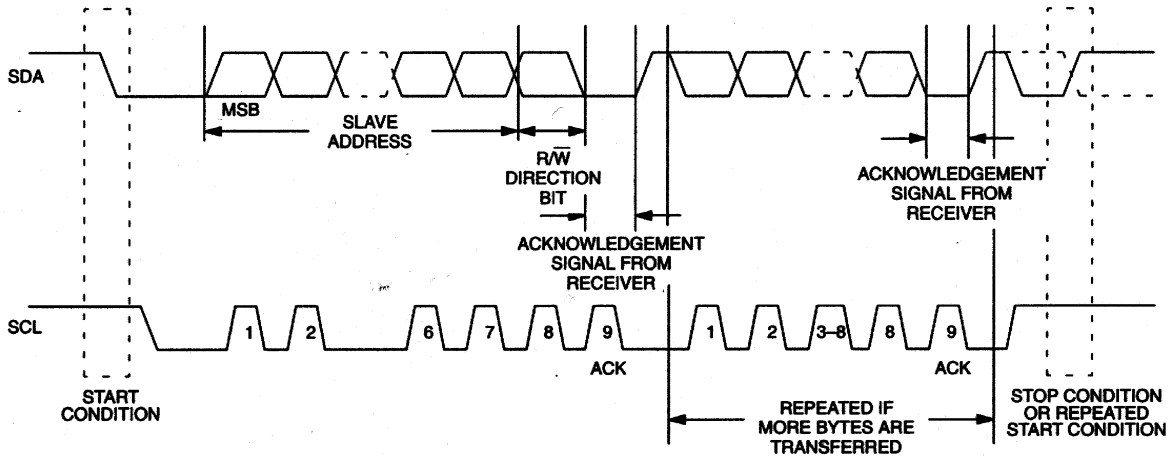
1. Slave receiver mode: Serial data and clock are received through SDA and SCL respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.
2. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1848 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.
3. Slave Address: command/control byte is the 1st byte received following the START condition from the master device. The command/control byte consists of a 4-bit control code. For the DS1848, this is set as **1010** binary for read/write operations. The next 3 bits of the command/ control byte are the device select bits or slave address (A2, A1, A0). They are used by the master device to select which of eight devices is to be accessed. When reading or writing the DS1848, the device-select bits must match the device-select pins (A2, A1, A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1 a read operation is selected, and when set to a 0 a write operation is selected.

Following the START condition, the DS1848 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the **1010** control code, the appropriate device address bits, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

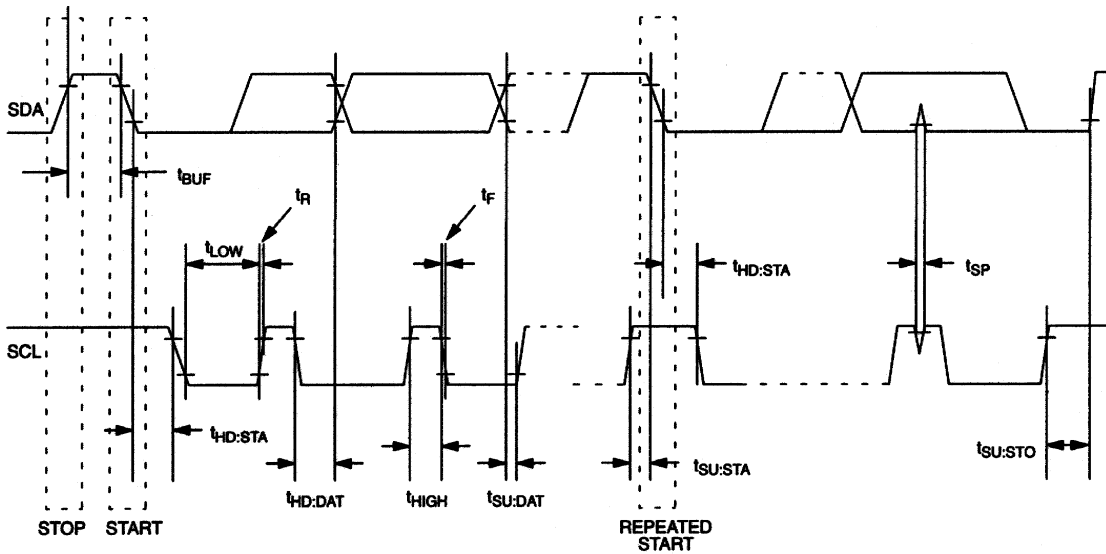
WRITE PROTECT

An external pin WP (write protect) protects EEPROM data and potentiometer position from alteration in an application. This pin must be open or tied high to protect data from alteration.

2- Wire Protocol Data Transfer Protocol Figure 2



2-Wire AC CHARACTERISTICS Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +6.0V
Operating Temperature	-40°C to +95°C
Programming Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +95°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	+2.7		5.5	V	1
Input Logic 1	V _{IH}	.7 V _{CC}		V _{CC} +0.5	V	1
Input Logic 0	V _{IL}	GND-0.5		.3 V _{CC}	V	1
Resistor Inputs	L,H	GND-0.5		V _{CC} +0.5	V	1

DIGITAL THERMOMETER

PARAMETER	SYMBOL	CONDITION	TYP	MAX	UNITS	NOTES
Thermometer Error	T _{ERR}	-40°C to 95°C		± 3.0	°C	
Conversion Time	t _{CONVT}	12-bit conversion		10	ms	

DC ELECTRICAL CHARACTERISTICS (-40°C to +95°C; $V_{CC} = 2.7V$ to $5.5V$)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CC}			0.5	2	mA	2
Input Leakage	I_{LI}		-1		+1	μA	
Input Logic 1	V_{IH}		$0.7 V_{CC}$		$V_{CC}+0.5$	V	1
Input Logic 0	V_{IL}		GND-0.5		$0.3 V_{CC}$	V	1
Input Logic levels A0, A1, A2		Input Logic 1 Input Logic 0	$0.7 V_{CC}$ GND-0.5		$V_{CC}+0.5$ $0.3 V_{CC}$	V	1
Input Current each I/O pin		$0.4 < V_{IO} < 0.9 V_{DD}$	-10		+10	μA	
Low Level Output Voltage (SDA)	V_{OL1}	3 mA sink current	0.0		0.4	V	1
	V_{OL2}	6 mA sink current	0.0		0.6	V	1
I/O Capacitance	C_{IO}				10	pF	
WP Internal Pull Up Resistance, R_{wp}	R_{wp}		40	65	100	k Ω	

ANALOG RESISTOR CHARACTERISTICS (-40°C to +95°C; $V_{CC}=2.7V$ to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Resistance		1k – 50k	-20		+20	%	3
Absolute Linearity			-1		+1	LSB	4
Relative Linearity			-1		+1	LSB	5
-3 dB Cutoff frequency	f_{cutoff}			125		kHz	
Temperature Coefficient				850		PPM/°C	12

AC ELECTRICAL CHARACTERISTICS (-40°C to +95°C, $V_{CC}=2.7V$ to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL clock frequency	f_{SCL}		0 0		400 100	kHz	*,6 **
Bus free time between STOP and START condition	t_{BUF}		1.3 4.7			μs	*,6 **
Hold time (repeated) START condition	$t_{HD:STA}$		0.6 4.0			μs	*,7,6 **
Low period of SCL clock	t_{LOW}		1.3 4.7			μs	*,6 **
High period of SCL clock	t_{HIGH}		0.6 4.0			μs	*,6 **
Data hold time	$t_{HD:DAT}$		0 0		0.9	μs	*,6,8,9 **
Data set-up time	$t_{SU:DAT}$		100 250			ns	*,6 **
Start set-up time	$t_{SU:STA}$		0.6 4.7			μs	*,6 **
Rise time of both SDA and SCL signals	t_R		$20+0.1C_B$		300 1000	ns	*,10 **
Fall time of both SDA and SCL signals	t_F		$20+0.1C_B$		300 300	ns	*,10 **
Set-up time for STOP condition	$t_{SU:STO}$		0.6 4.0			μs	* **
Capacitive load for each bus line	C_B				400	pF	10
EEPROM write time	T_w			5		ms	11

* fast mode

** standard mode

NOTES:

- 1) All voltages are referenced to ground.
- 2) Max Icc is dependent on clock rates.
- 3) Valid at 25°C only.
- 4) Absolute linearity is used to measure expected resistance value as determined by resistor position.
- 5) Relative linearity is used to determine the change of resistance value between two adjacent resistor positions.
- 6) A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.
- 7) After this period, the first clock pulse is generated.
- 8) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
- 9) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
- 10) C_B - total capacitance of one bus line in picofarads, timing referenced to $(0.9)(V_{CC})$ and $(0.1)(V_{CC})$.
- 11) EEPROM write begins after a stop condition occurs.
- 12) An equation for temperature coefficients over resistor settings can be supplied

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	OPERATING TEMPERATURE	VERSION Resistor 0 /Resistor 1
DS1848E-050	14 PIN TSSOP (173 MIL)	-40°C TO +95°C	50 kΩ/10 kΩ
DS1848E-050/T&R	14 PIN TSSOP/TAPE & REEL	-40°C TO +95°C	50 kΩ/10 kΩ
DS1848B-050	16 BALL STPBGA	-40°C TO +95°C	50 kΩ/10 kΩ