

SIEMENS

**HYB 514100BJ/BJL -50/-60/-70
4 194 304 x 1 - Bit Dynamic RAM**

**HYB 514400BJ/BJL -50/-60/-70
1 048 576 x 4 - Bit Dynamic RAM**

INFORMATION NOTE

Fourth Generation 4M-DRAM (Ultrashrink-Version)

General Information

Products

Design and technology highlights

Package outline dimension

Packing

10.95

Info4M20.doc

This information note is intended to provide technical information on the SIEMENS 4M x 1 and 1M x 4 bit generation ("Ultrashrink-Version") DYNAMIC ACCESS MEMORIES HYB 514100BJ and HYB 514400BJ .

GENERAL INFORMATION

The SIEMENS HYB514100BJ and HYB514400BJ are latest generation dynamic RAMs organized 4,194,304 words by 1 bit and 1,048,576 words by 4 bits respectively, assembled in 300 mil wide SOJ26/20 packages. The design features fast page mode operations. Low Power versions with low standby current and high data retention time especially selected for battery backup operations are also available. (fig.1)

The HYB 514100BJ and HYB 514400BJ utilises the SIEMENS submicron twin-well CMOS silicon gate 4M-process technology with depletion type trench capacitors with ONO dielectric as well as advanced circuit techniques to provide wide operation margins, both internally and to the system user.

Figs. 2 - 4 highlight the process, design and assembly related data.

PACKAGE OUTLINE DRAWINGS

The SIEMENS 4M x 1/1M x 4 bit DRAMs are available in an industrial standard 26/20 pin plastic SOJ packages with 300 mil body width, appropriate for surface-mounting techniques. The 4M x 1 or 1M x 4 organisation are implemented by different bonding options. The package outline dimensions of the package meet JEDEC standards.

CODES FOR MARKING

The marking on the top side of every 4M x 1 or 1M x 4 device gives information to the device type, which access-time specification is met, and the country of origin "Germany". In addition, a weekcode indicates in which week of the year this part was tested. (fig.7)

A SIEMENS internal part number is printed on the bottom side which represents the wafer production lot number, the date of final assembly and a code for the assembly line. Laser equipment is used for top and bottom side marking.

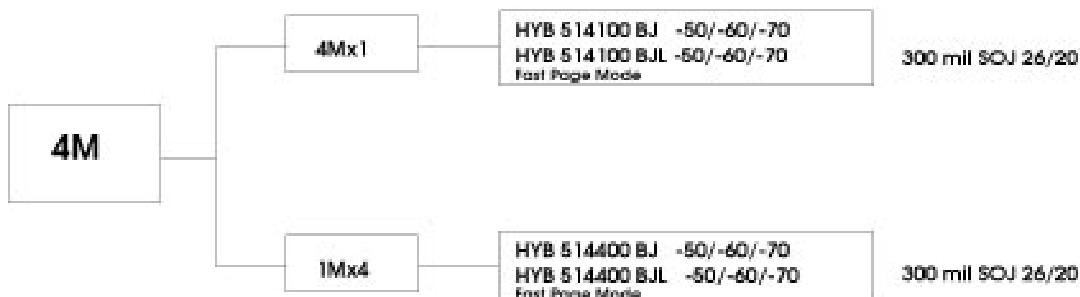
PACKING

Volume conductive polystyrol tubes ,especially designed for 300 mil SOJ packages with a surface resistance in the range between 10^5 to 10^7 Ohm/sq. are used. Each tube contains 25 SOJ DRAMs.

Before packing, all SOJ 4M-DRAMs are baked in metal tubes at 125°C in ovens with circulating hot air for 12 hours. Within 24 hours the devices are seal packed. One sealed dry pack contains 40 tubes along with a pouch of desiccant and a humidity indicator.

SIEMENS 4M-DRAMs in SOJ packages are also available dry-packed on tape & reel . In this case each reel contains 1500 SOJ 4M-devices.

SIEMENS recommends for SOJ packaged devices not to exceed a 168 hours time span between unpacking and vapour-phase or reflow-soldering.



-- fig. 1 --

**4Mx1 / 1M x 4 DRAM
PROCESS RELATED DATA**

| | | |
|--------------------------------------|--|--------|
| PROCESS | 0,6 µm twin well CMOS on a p-type substrate 2 Polysilicon layers 1 Molybdenum silicide layer 1 Aluminium layer | |
| SIEMENS PROCESS NAME | C5DH | |
| MINIMAL DESIGN RULES | | |
| Line | 0,6 µm | |
| Space | 0,7 µm | |
| LITHOGRAPHY | g-line Stepper / i-line Stepper | |
| CONTACT DIMENSIONS | | |
| final | 0,8 µm x 1,0 µm AlSiCu/TiN-barrier metalization | |
| CHANNEL LENGTH | | |
| gate final | n-Channel 0,75 µm LDD p-Channel 0,75 µm | |
| OXIDE THICKNESS | 18 nm | |
| JUNCTION DEPTH | n-Channel 0,25 µm p-Channel 0,35 µm | |
| THRESHOLD VOLTAGE | n-Channel 0,7 V p-Channel -1,1 V | |
| CELL-TYPE | Trench-Capacitor with Fully Overlapping Bitline Contact (FOBIC) 13 nm eff ONO 4,5 µm depth p-well depth 6 µm | |
| CELL-CAPACITANCE | > 40 fF | |
| BITLINE TO CELL CAPACITANCE RATIO | 10 : 1 | |
| METAL (AlSiCu) | Thickness | 800 nm |

--- fig 2 ---

**4Mx1/1Mx4 DRAM
DESIGN RELATED DATA**

| | | | | | | | |
|-------------------|--|-------------|-----------------|-------------------|-----------------|-----------------|-----------------|
| ORGANIZATION | 4M x 1 / 1M x 4 (bonding option) | | | | | | |
| OPERATION MODES | FAST PAGE MODE LOW POWER VERSIONS | | | | | | |
| REFRESH | 1024 CYCLES / 16 ms 1024 CYCLES / 128 ms for LOW POWER VERSIONS | | | | | | |
| TESTMODE | 8 bit | | | | | | |
| SPECIFICATIONS | <table><tr><td>trac</td><td>50 / 60 / 70 ns</td></tr><tr><td>t_{cac}</td><td>13 / 15 / 20 ns</td></tr><tr><td>t_{aa}</td><td>25 / 30 / 35 ns</td></tr></table> | trac | 50 / 60 / 70 ns | t _{cac} | 13 / 15 / 20 ns | t _{aa} | 25 / 30 / 35 ns |
| trac | 50 / 60 / 70 ns | | | | | | |
| t _{cac} | 13 / 15 / 20 ns | | | | | | |
| t _{aa} | 25 / 30 / 35 ns | | | | | | |
| CHIP SIZE | 4.72 mm x 10.46 mm = 49.37 mm ² | | | | | | |
| CELL SIZE | 1.63 μm x 3.27 μm = 5.33 μm ² | | | | | | |
| SENSE LINE | FOLDED BITLINE CONCEPT with 16 blocks of 256k cells | | | | | | |
| WORDLINE PITCH | 1.63 μm | | | | | | |
| BITLINE PITCH | 1.63 μm | | | | | | |
| PARTITIONING | <table><tr><td>cells</td><td>43%</td></tr><tr><td>pitched circuits</td><td>28%</td></tr><tr><td>periphery</td><td>29%</td></tr></table> | cells | 43% | pitched circuits | 28% | periphery | 29% |
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| pitched circuits | 28% | | | | | | |
| periphery | 29% | | | | | | |
| REDUNDANCY | <table><tr><td>ROWS</td><td>16</td></tr><tr><td>COLUMNS</td><td>64</td></tr><tr><td>METHOD</td><td>LASER</td></tr></table> | ROWS | 16 | COLUMNS | 64 | METHOD | LASER |
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| COLUMNS | 64 | | | | | | |
| METHOD | LASER | | | | | | |
| NUMBER OF DEVICES | <table><tr><td>transistors</td><td>4.7 Mio</td></tr><tr><td>trench capacitors</td><td>4.2 Mio</td></tr><tr><td>contact holes</td><td>3.0 Mio</td></tr></table> | transistors | 4.7 Mio | trench capacitors | 4.2 Mio | contact holes | 3.0 Mio |
| transistors | 4.7 Mio | | | | | | |
| trench capacitors | 4.2 Mio | | | | | | |
| contact holes | 3.0 Mio | | | | | | |

-- fig.3 --

**4Mx1/1Mx4 DRAM
ASSEMBLY RELATED DATA****Surface mount package:**

| | |
|------------------|--|
| PACKAGE | 300 mil SOJ 26/20 JEDEC-standard |
| LEAD FRAME | Material Cu Ni(3.2%) Finish 80% Pb / 20% Sn solder (electroplated) |
| DIE ATTACH | silver filled epoxy |
| WIRE BOND | 24 um Au wires,thermosonic |
| CHIP PROTECTION | Polyimid layer |
| MOLDING COMPOUND | ARATRONIK 2180VA (Ciba Geigy) |

-- fig.4 --

CODES FOR MARKING

The following codes are marked on the top of all SIEMENS
4M x 1 / 1Mx 4 DRAMS:

Example: HYB 514100 BJL - 70

- 1.Dash Number
2. Special Selection
- 3.Package
- 4.Die revision
- 5.Device number
- 6.SIEMENS prefix

1.Dash number

Two numerical characters defining specific device performance

- 50 part meets 50 ns tRAC access time specification
- 60 part meets 60 ns tRAC access time specification
- 70 part meets 70 ns tRAC access time specification

2.Special selection

The additional marking shown below indicates that the device is a special selection out of the standard product.

- L Low Power Version for battery backup operations
- T extended temperature range (-40°C to +85°C)

3.Package

- J SOJ26/20 300 mil wide surface mount package
- T TSOPII - 26/20 package

4.Die revision

- B Design revision

5.Device number

- 514100 4Mx1 with fast page mode operation
- 514400 1Mx4 with fast page mode operation

6.SIEMENS prefix

HYB standard prefix for SIEMENS memories

FOUR DIGIT WEEKCODE:

Example : 9601 is the first week of year 1996

Note The top side marking is done after the lot has been through
 a 100 % dynamic burn-in

fig.7