PM5346

S/UNI-LITE

SATURN USER NETWORK INTERFACE (LITE)

DATA SHEET ERRATA

ISSUE 9: MARCH 1999

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
9	Sept., 1998	Revised test mode 0 register settings and clarified the register bits that set INTB. LOOPT bit description modified.

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1 RDOOLV BIT OPERATION:

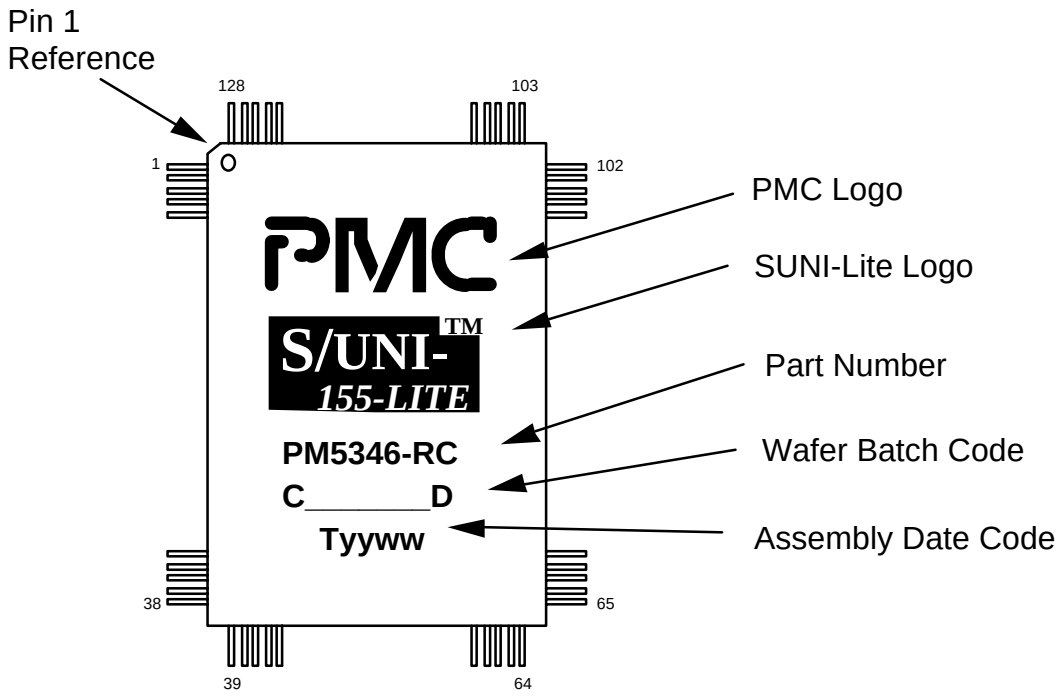
Anomolous operation of the RDOOLV bit (Register 0x07, bit 3 on page 50 of the Issue 6 datasheet) has been noticed. Under certain circumstances, the RDOOLV bit may falsely indicate data out of lock.

It is recommended that spurious RDOOLV indications be ignored, and that the RDOOLE bit (Register 0x07, bit 1 on page 50 of the Issue 6 datasheet) be programmed to '0' in order to permanently disable RDOOLV interrupts.

The RDOOLV bit should only be examined as a diagnostic aid in situations where other major on-chip alarms are indicated.

Note: The anomolous RDOOLV only occurs in revisions prior to 'Revision D' of the PM5346 S/UNI-155 LITE. Subsequent revisions, starting with 'Revision D' have this problem corrected. Software work-arounds as indicated above will work with all revisions. For details on identifying the device revision, please refer to the Branding Diagram.

2 BRANDING DIAGRAM



SCALE = 3.2 : 1 (Approx.)

Wafer Batch Code has three components:
• One character for wafer fab source (**P or C**)
• Up to 7 characters and/or digits for wafer manufacturer's batch code (_____)
• One character for mask set revision (**A, C or D**). Note: There is no rev. '**B'.**

For example "CA123456D" is for source "C" wafers, batch A12345.6, device rev "D"

Assembly Date Code has three components:

1 character for assembly source (**T**)
2 digits for year (**yy**)
2 digits for week (**ww**)

For example "T9524" is for parts packaged by source "T" in the 24th week of 1995.

3 LOOP FILTER RECOMMENDATIONS

An extensive analysis of loop filter requirements on the S/UNI-LITE was performed. As a result of this analysis, the following changes are required to the Issue 6 datasheet:

3.1 Page 111

On Page 111 of the Issue 6 datasheet, make the following changes:

Clock Recovery

Figure~~s~~ 14a) ~~and 14b) are~~ is an abstraction~~s~~ of the clock recovery phase lock loop illustrating the connections to external components.

Figure 14a illustrates the asymmetrical loop filter application where the external passive components (R1, R2, C1, C2) are set to different values to account for the finite output impedance of the integral op-amp in the S/UNI-LITE. The asymmetrical loop filter circuit provides maximum jitter tolerance without jitter peaking and is recommended for all designs. ~~does not have good jitter transfer properties and is not recommended for new designs.~~

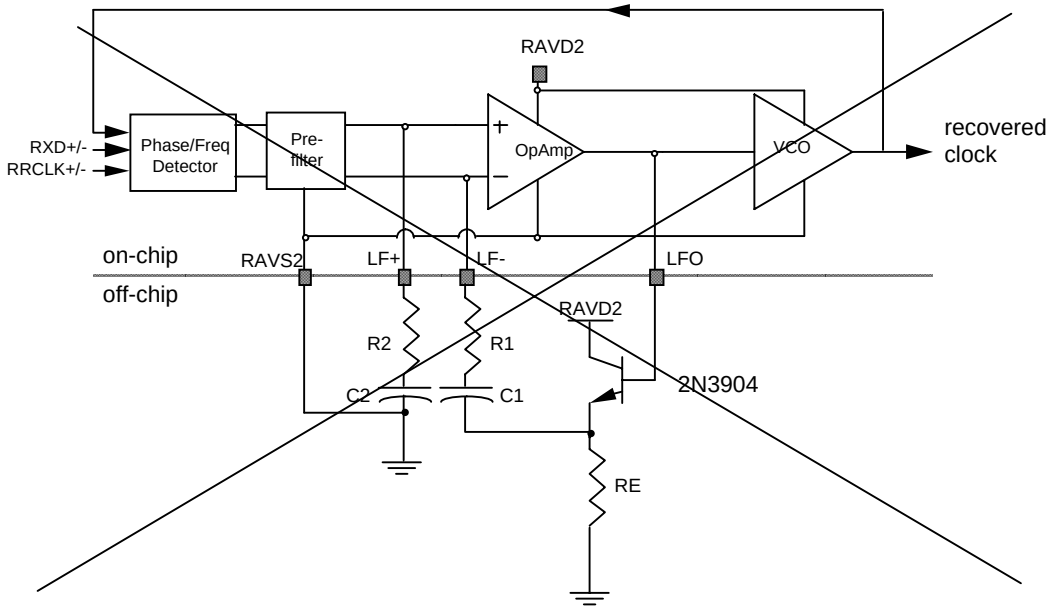
~~Figure 14b illustrates the unity gain buffer loop filter application where the integral op-amp output is buffered through a unity gain amplifier to minimize the effect of its finite output impedance on the transfer function of the PLL. The unity gain buffer loop filter circuit exceeds SONET/SDH jitter tolerance and jitter transfer specifications and is recommended for new designs.~~

~~Additional analysis of jitter transfer and jitter tolerance issues for the S/UNI-LITE can be found in PMC's ATM Design Notes "Meeting SONET/SDH WAN Interface Jitter Transfer Requirements with the S/UNI-LITE", PMC-950139~~

3.2 Page 113

On Page 113 of the Issue 6 datasheet, make the following changes (delete entire page):

~~**Fig. 14b Clock Recovery Circuit - Unity Gain Buffer Loop Filter (recommended for designs requiring BISDN-UNI jitter transfer)**~~



~~Line Rate (Mbit/s)~~	~~R1 (•±1%)~~	~~R2 (•±1%)~~	~~C1, C2 min (µF)~~	~~RE (•±1%)~~
~~155.52~~	~~68.1~~	~~90.9~~	~~4.7~~	~~100~~
~~51.84~~	~~68.1~~	~~90.9~~	~~15~~	~~100~~

~~The capacitors (C1, C2) determine the amount of "peaking" in the jitter transfer curve. The capacitor values can be ±10%. The capacitors should be non-polarized because when the S/UNI-LITE is held in reset, the capacitors are reverse-biased at approximately 2.0V. Also, for some process extremes, the capacitors may operate with a D.C. reverse-bias of up to 1.0V.~~

The recommended values for the capacitors are not readily available in non-polarized versions. Therefore, two polarized capacitors can be connected "back-to-back" (in series, anode-to-anode) to implement each capacitance in Figure

14b. Since these back-to-back capacitors will be in series, they should be of twice the value of the desired capacitance. This back-to-back configuration effectively creates a "bi-polar" capacitor.

4 TEST MODE 0

In order to correctly test in Test Mode 0 the following registers must be written with all zeros: 0x9A, 0xB2 and 0xE0.

As well, register 0x96 bit 6 and register 0xD0 bit 0 control the INTB, if either bit is set to a one the output pin is asserted low.

The INTB pin is the NOR of both these register bits.

5 PAGE 47

On Page 47 of the Issue 6 datasheet, make the following changes (under LOOPT bit description):

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the S/UNI-LITE. When LOOPT is a logic zero, the transmitter timing is derived from inputs TRCLK+ and TRCLK-.

When LOOPT is a logic one, the transmitter timing is derived form the receiver inputs RXD+ and RXD- ~~when clock recovery is enabled and from RRCLK+ and RRCLK- when clock recover is disabled~~.

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PMC-941215 (R9) ref PMC-931110(R6) Issue date: March 1999