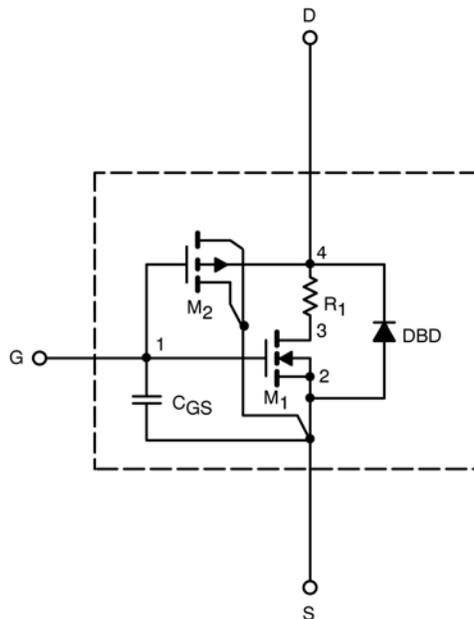# Dual N-Channel 2.5-V (G-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0 to 5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

SPICE Device Model Si9926BDY
Vishay Siliconix

| Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.96		V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5\ V$, $V_{GS} = 4.5\ V$	394		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 4.5\ V$, $I_D = 8.2\ A$	0.015	0.016	Ω
		$V_{GS} = 2.5\ V$, $I_D = 3.3\ A$	0.022	0.024	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15\ V$, $I_D = 8.2\ A$	26	29	S
Forward Voltage[a]	V_{SD}	$I_S = 1.7\ A$, $V_{GS} = 0\ V$	0.80	0.80	V
Dynamic[b]					
Total Gate Charge	Q_g	$V_{DS} = 10\ V$, $V_{GS} = 4.5\ V$, $I_D = 8.2\ A$	10	11	nC
Gate-Source Charge	Q_{gs}		2.5	2.5	
Gate-Drain Charge	Q_{gd}		3.2	3.2	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ V$, $R_L = 10\ \Omega$ $I_D \cong 1\ A$, $V_{GEN} = 10\ V$, $R_G = 6\ \Omega$	50	35	ns
Rise Time	t_r		32	50	
Turn-Off Delay Time	$t_{d(off)}$		24	31	
Fall Time	t_f		14	15	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)
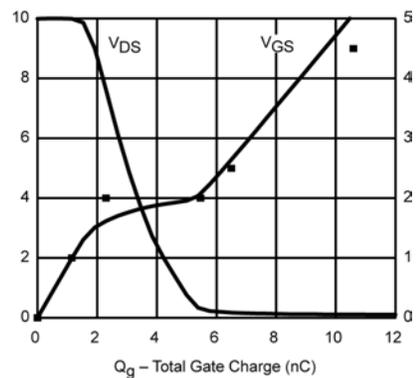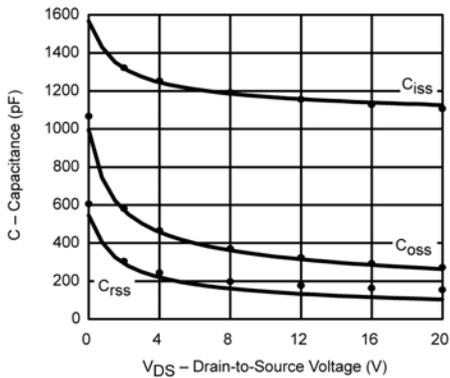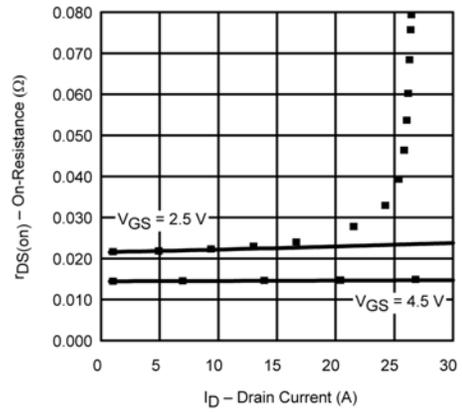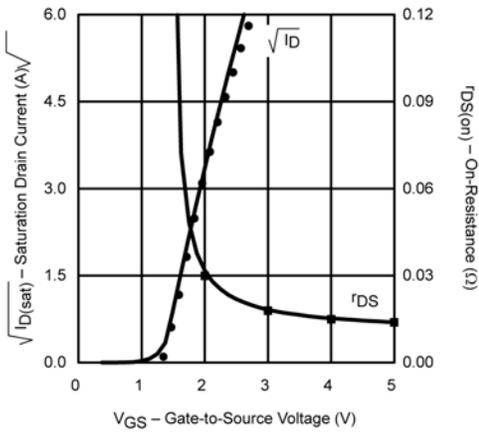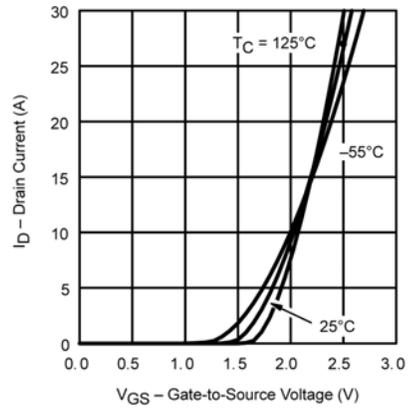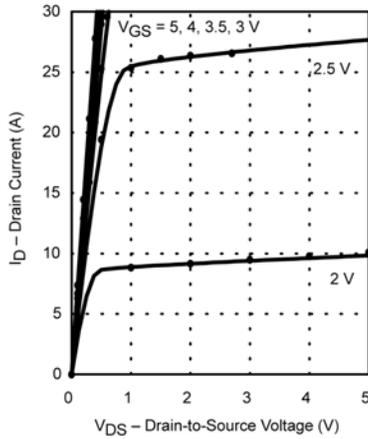
Note: Dots and squares represent measured data.