

March 1997

Features

- **Fast Access Time**
 - $V_{DD} = 5V$ 450ns
 - $V_{DD} = 10V$ 250ns
- **Common Data Inputs and Outputs**
- **Multiple Chip Select Inputs to Simplify Memory System Expansion**

Ordering Information

5V	10V	PACKAGE	TEMP. RANGE	PKG. NO.
CDP1823CE	CDP1823E	PDIP	-40°C to +85°C	E24.6
CDP1823CD	CDP1823D	SBDIP	-40°C to +85°C	D24.6
CDP1823CDX	-	Burn-In		D24.6

Description

The CDP1823 and CDP1823C are 128-word by 8-bit CMOS SOS static random-access memories. These memories are compatible with general-purpose microprocessors. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4V to 10.5V, and the CDP1823C has a recommended operating voltage range of 4V to 6.5V.

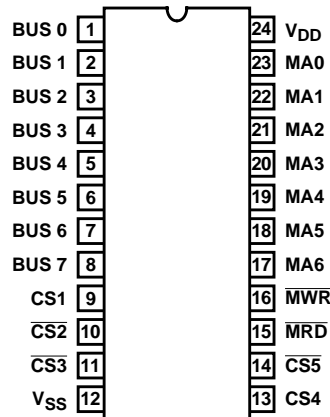
The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs CS2, CS3 and CS5 require a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The MRD signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the MRD signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

Pinout

CDP1823, CDP1823C
(PDIP, SBDIP)
TOP VIEW



CDP1823, CDP1823C

OPERATIONAL MODES

FUNCTION	MRD	MWR	CS1	CS2	CS3	CS4	CS5	BUS TERMINAL STATE
Read	0	X	1	0	0	1	0	Storage State of Addressed Word
Write	1	0	1	0	0	1	0	Input High-Impedance
Stand-By (Active)	1	1	1	0	0	1	0	High Impedance
Not Selected	X	X	0	X	X	X	X	High Impedance
	X	X	X	1	X	X	X	High Impedance
	X	X	X	X	1	X	X	High Impedance
	X	X	X	X	X	0	X	High Impedance
	X	X	X	X	X	X	1	High Impedance

Logic 1 = High, Logic 0 = Low, X = Don't Care

CDP1823, CDP1823C

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) (All Voltages Referenced to V_{SS} Terminal)	
CDP1823	-0.5V to +11V
CDP1823C	-0.5V to +7V
Input Voltage Range, All Inputs	-0.5V to $V_{DD} + 0.5V$
DC Input Current, Any One Input	$\pm 10mA$
Operating Temperature Range (T_A)	
Package Type D	-55°C to +125°C
Package Type E	-40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	60	N/A
SBDIP Package	60	17
Maximum Storage Temperature Range (T_{STG})	-65°C to +150°C	
Maximum Junction Temperature		
Plastic Package	+150°C	
Maximum Lead Temperature (During Soldering)	300°C	

Recommended Operating Conditions At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	MIN	MAX	MIN	MAX	
Supply Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications At T_A = -40°C to +85°C, Except as Noted:

PARAMETER	SYMBOL	CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1823			CDP1823C			
					MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	-	500	-	-	500	μA
		-	0, 10	10	-	-	1000	-	-	-	μA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	2	4	-	2	4	-	mA
		0.5	0, 10	10	4.5	9	-	-	-	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-1	-2	-	-1	-2	-	mA
		9.5	0, 10	10	-2.2	-4.4	-	-	-	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	± 5	-	-	± 5	μA
			0, 10	10	-	-	± 10	-	-	-	μA
Operating Current (Note 2)	I_{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	± 5	-	-	± 5	μA
		0, 10	0, 10	10	-	-	± 10	-	-	-	μA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:

1. Typical values are for T_A = +25°C and nominal V_{DD} .
2. Outputs open circuited; Cycle time = 1 μs .

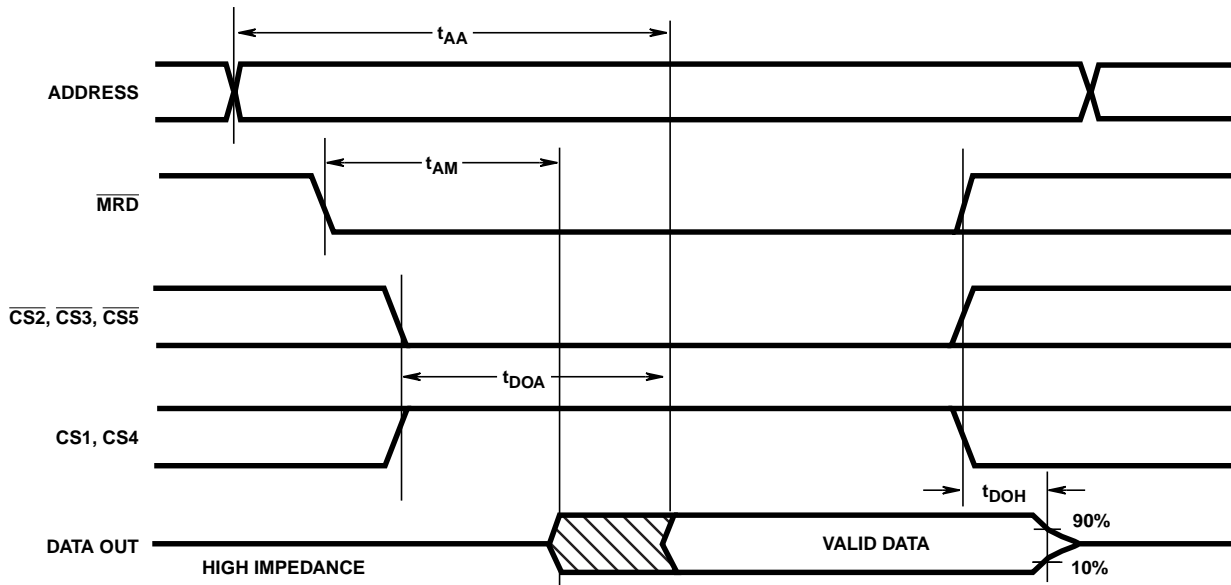
CDP1823, CDP1823C

Dynamic Electrical Specifications At $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_R, t_F = 20\text{ns}$, $C_L = 100\text{pF}$

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS						UNITS
			CDP1823			CDP1823C			
			(NOTE 2) MIN	(NOTE 1) TYP	MAX	(NOTE 2) MIN	(NOTE 1) TYP	MAX	
Read Cycle (See Figure 1)									
Access Time From Address Change	t_{AA}	5	-	275	450	-	275	450	ns
		10	-	150	250	-	-	-	ns
Access Time From Chip Select	t_{DOA}	5	-	150	250	-	150	250	ns
		10	-	100	150	-	-	-	ns
$\overline{\text{MRD}}$ to Output Active	t_{AM}	5	-	150	250	-	150	250	ns
		10	-	100	150	-	-	-	ns
Data Hold Time After Read	t_{DOH}	5	25	50	75	25	50	75	ns
		10	15	25	40	-	-	-	ns

NOTES:

1. Typical values are at $T_A = 25^\circ\text{C}$ and nominal voltage.
2. Time required by a limit device to allow for the indicated function.



NOTE:

1. $\overline{\text{MWR}}$ is high during read operation. Timing measurement reference is $0.5 V_{DD}$.

FIGURE 1. READ CYCLE TIMING DIAGRAM

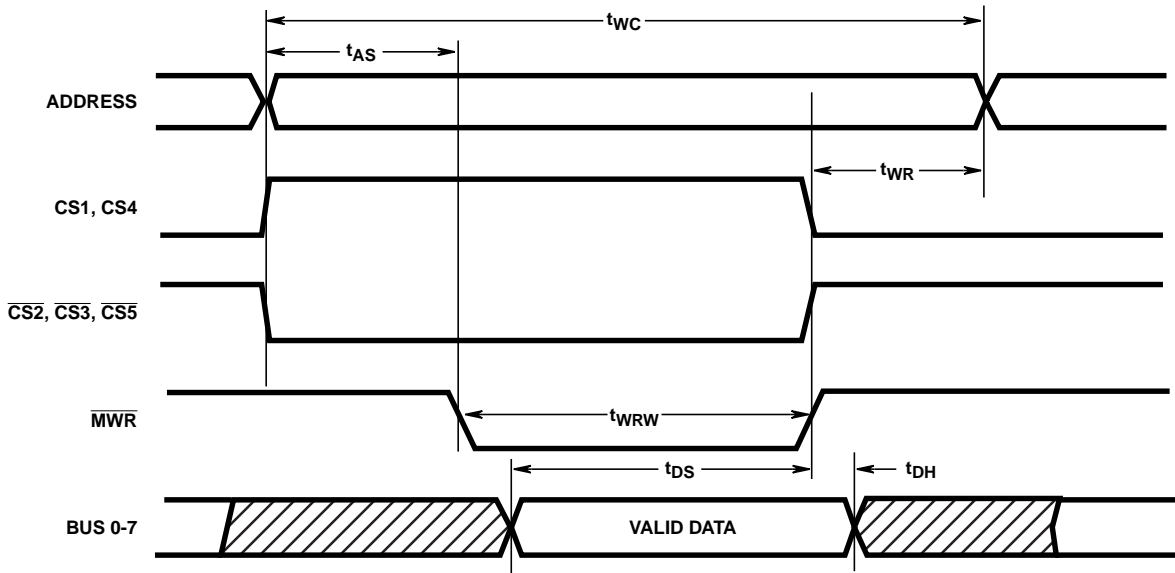
CDP1823, CDP1823C

Dynamic Electrical Specifications At $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $t_R, t_F = 20\text{ns}$, $C_L = 100\text{pF}$

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS						UNITS
			CDP1823			CDP1823C			
			(NOTE 2) MIN	(NOTE 1) TYP	MAX	(NOTE 2) MIN	(NOTE 1) TYP	MAX	
Write Cycle (See Figure 2)									
Write Recovery	t_{WR}	5	75	-	-	75	-	-	ns
		10	50	-	-	-	-	-	ns
Write Cycle	t_{WC}	5	400	-	-	400	-	-	ns
		10	225	-	-	-	-	-	ns
Write Pulse Width	t_{WRW}	5	200	-	-	200	-	-	ns
		10	100	-	-	-	-	-	ns
Address Setup Time	t_{AS}	5	125	-	-	125	-	-	ns
		10	75	-	-	-	-	-	ns
Data Setup Time	t_{DS}	5	100	-	-	100	-	-	ns
		10	75	-	-	-	-	-	ns
Data Hold Time From \overline{MWR}	t_{DH}	5	75	-	-	75	-	-	ns
		10	50	-	-	-	-	-	ns

NOTES:

1. Typical values are at $T_A = 25^\circ\text{C}$ and nominal voltage.
2. Time required by a limit device to allow for the indicated function.



NOTE:

1. \overline{MRD} must be high during write operation.

FIGURE 2. WRITE CYCLE TIMING DIAGRAM

CDP1823, CDP1823C

Data Retention Specifications At $T_A = -40$ to $+85^\circ\text{C}$, see Figure 3

PARAMETER	TEST CONDITIONS		LIMITS						UNITS
	V_{DR} (V)	V_{DD} (V)	CDP1823			CDP1823C			
			MIN	(NOTE 1) TYP	MAX	MIN	(NOTE 1) TYP	MAX	
Minimum Data Retention Voltage, V_{DR}	-	-	-	1.5	2	-	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	-	-	30	100	-	30	100	μA
Chip Deselect to Data Retention Time t_{CDR}	-	5	600	-	-	600	-	-	ns
	-	10	300	-	-	-	-	-	ns
Recovery to Normal Operation Time t_{RC}	-	5	600	-	-	600	-	-	ns
	-	10	300	-	-	-	-	-	ns
V_{DD} to V_{DR} Rise and Fall Time t_R, t_F	2	5	1	-	-	1	-	-	μs

NOTE:

Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

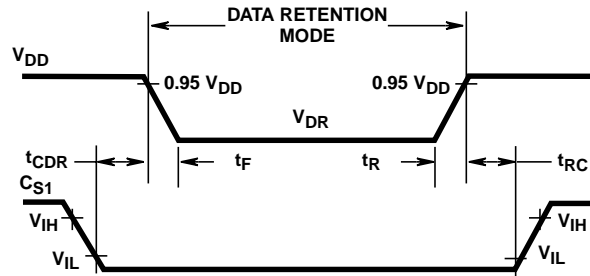


FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

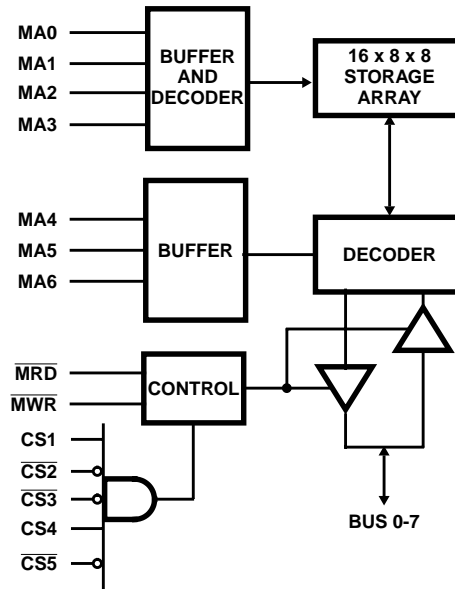


FIGURE 4. FUNCTIONAL DIAGRAM

CDP1823, CDP1823C

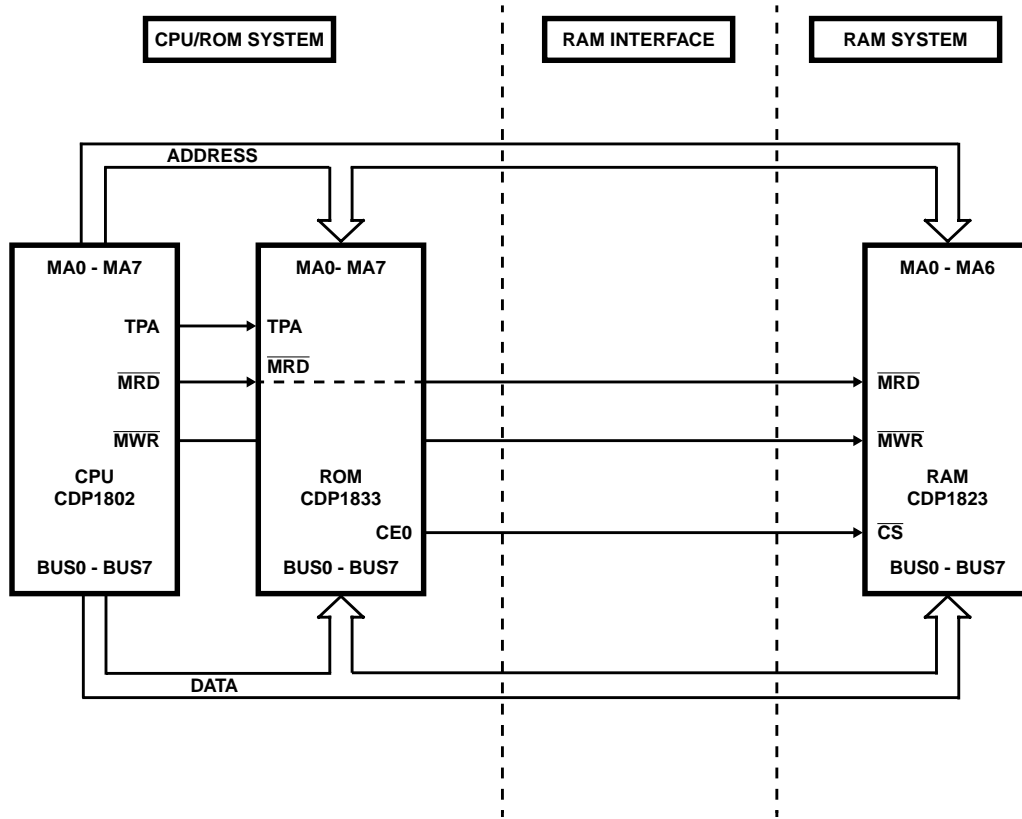


FIGURE 5. CDP1823 (128 x 8) MINIMUM SYSTEM (128 x 8)

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029