

**TC74VHC132F, TC74VHC132FN, TC74VHC132FT**

**QUAD 2-INPUT SCHMITT NAND GATE**

The TC74VHC132 is an advanced high speed CMOS 2-INPUT SCHMITT NAND GATE fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74VHC00 but the inputs have hysteresis and with its schmitt trigger function, the TC74VHC132 can be used as a line receivers which will receive slow input signals.

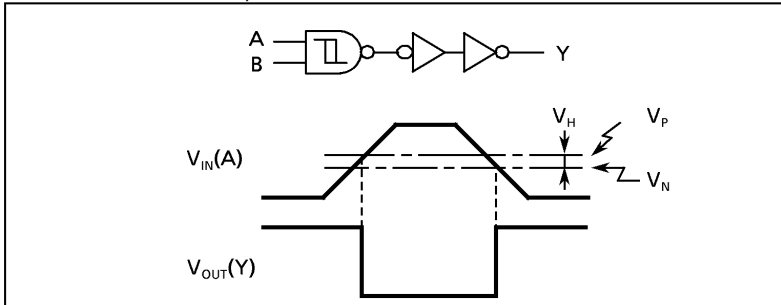
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

This circuit prevents device destruction due to mismatched supply and input voltages.

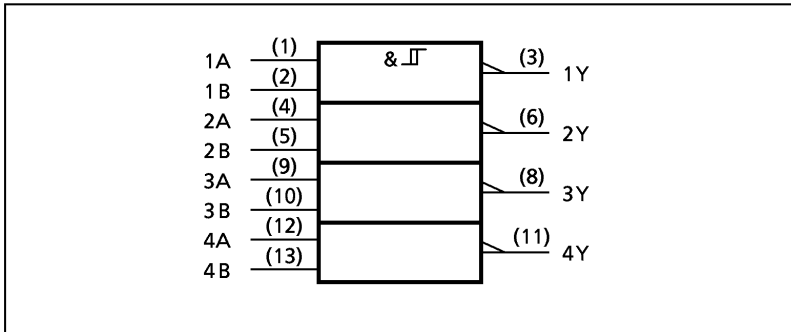
**FEATURES :**

- High Speed..... $t_{pd} = 4.9ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 2\mu A$ (Max.) at  $T_a = 25^{\circ}C$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (opr) = 2V \sim 5.5V$
- Low Noise..... $V_{OLP} = 0.8V$  (Max.)
- Pin and Function Compatible with 74ALS132

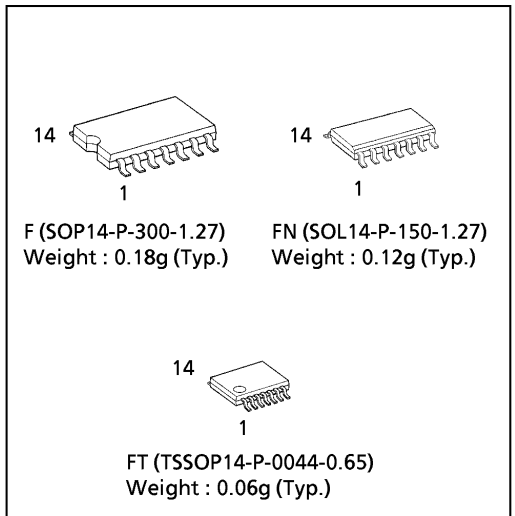
**SYSTEM DIAGRAM, WAVEFORM**



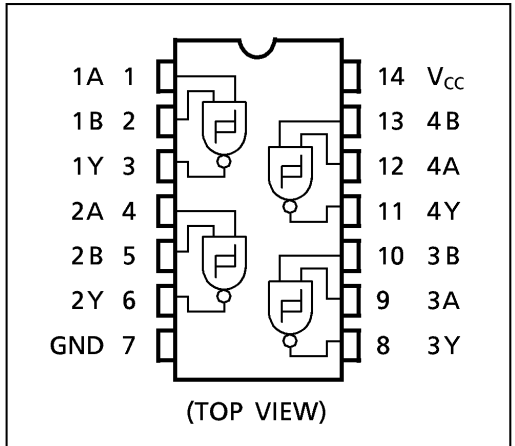
**IEC LOGIC SYMBOL**



(Note) The JEDEC SOP (FN) is not available in Japan.



**PIN ASSIGNMENT**



**TRUTH TABLE**

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
Positive Threshold Voltage	$V_P$		3.0	—	—	2.20	—	2.20	V	
			4.5	—	—	3.15	—	3.15		
			5.5	—	—	3.85	—	3.85		
Negative Threshold Voltage	$V_N$		3.0	0.90	—	—	0.90	—	V	
			4.5	1.35	—	—	1.35	—		
			5.5	1.65	—	—	1.65	—		
Hysteresis Output Voltage	$V_H$		3.0	0.30	—	1.20	0.30	1.20	V	
			4.5	0.40	—	1.40	0.40	1.40		
			5.5	0.50	—	1.60	0.50	1.60		
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu A$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0	2.58	—	—	2.48	—	V
				4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu A$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0	—	—	0.36	—	0.44	V
				4.5	—	—	0.36	—	0.44	
Input Leakage Current	$I_{IN}$	$V_{IN} = 5.5V$ or GND	0~5.5	—	—	±0.1	—	±1.0	$\mu A$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0		

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**AC ELECTRICAL CHARACTERISTICS ( Input  $t_r = t_f = 3ns$  )**

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V <sub>CC</sub> (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	$t_{pLH}$ $t_{pHL}$	3.3 ± 0.3	15	—	7.6	11.9	1.0	14.0	ns
			50	—	10.1	15.4	1.0	17.5	
		5.0 ± 0.5	15	—	4.9	7.7	1.0	9.0	
			50	—	6.4	9.7	1.0	11.0	
Input Capacitance	C <sub>IN</sub>			—	4	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 1)		—	16	—	—	—	

Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

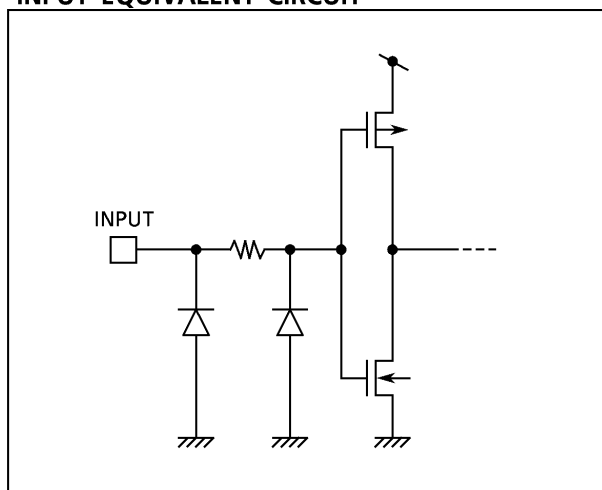
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ ( per Gate. )}$$

**NOISE CHARACTERISTICS ( Input  $t_r = t_f = 3ns$  )**

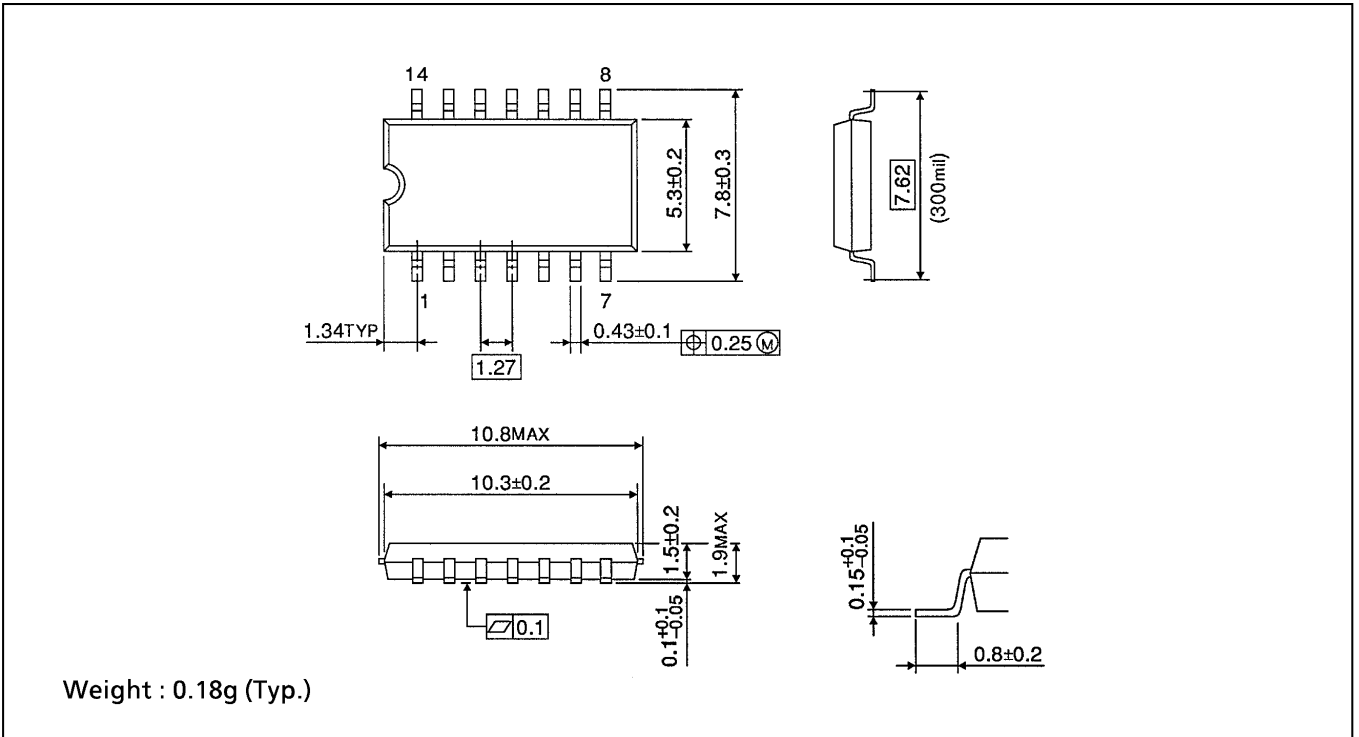
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V <sub>CC</sub> (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50pF	5.0	0.3	0.8	V
Quiet Output Minimum Dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50pF	5.0	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50pF	5.0	—	1.5	V

**INPUT EQUIVALENT CIRCUIT**



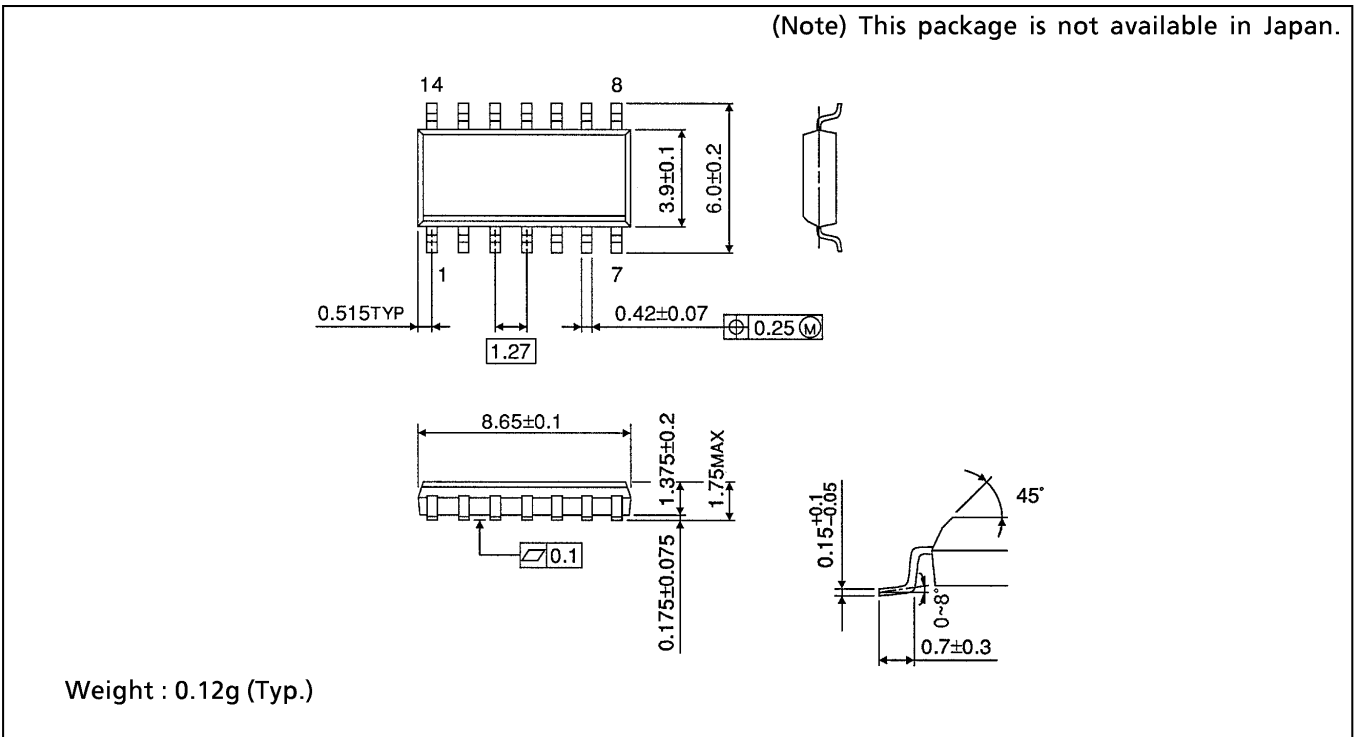
**SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)**

Unit in mm



**SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOP14-P-150-1.27)**

Unit in mm



**TSSOP 14PIN PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)**

Unit in mm

